Self Healing MIMO Transreceiver Module On-Chip

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ABSTRACT
In this study channel estimation and error recovery schemes to support self-healing Multi Input Multi Output transmitter and receiver architecture is proposed. The paper can coexist with existing Automatic modulation Identification hardware module. This technique is used for interference identification and source identification of received signal. The Decision theoretic approach uses the likelihood function where probabilistic and hypothesis-testing arguments to formulate the recognition problem at the output of the channel and accordingly classification are performed. The merits of the proposed approach are its lesser computational complexity, ease in implementation and robustness to model mismatch.

Keywords
Self healing, MIMO, Module on-chip,

1. INTRODUCTION
MIMOC is a dynamic and flexible network architecture that protects existing investments while future proofing the network. With MIMOC, today's static network can evolve into an extensible service delivery platform capable of responding rapidly to changing business, end-user, and market needs.

2. MIMO NETWORKING ARCHITECTURE
Traditional network architectures are ill suited to meet the requirements of today's enterprises, carriers, and end users. MIMO-on-Chip (MIMOC) is transforming networking architecture. MIMOC is currently being rolled out in a variety of networking devices and software, delivering substantial benefits to both enterprises and carriers, including,

(i) centralized management and control of networking devices from multiple vendors, improved automation and management by using common APIs to abstract the underlying networking details from the orchestration and provisioning systems and applications,
(ii) rapid innovation through the ability to deliver new network capabilities and services without the need to configure individual devices or wait for vendor releases,
(iii) programmability by operators, enterprises, independent software vendors, and users (not just equipment manufacturers) using common programming environments, which gives all parties new opportunities to drive revenue and differentiation,
(iv) increased network reliability and security as a result of centralized and automated management of network devices, uniform policy enforcement, and fewer configuration errors,
(v) more granular network control with the ability to apply comprehensive and wide-ranging policies at the session, user, device, and application levels and
(vi) better end-user experience as applications exploit centralized network state information to seamlessly adapt network behavior to user needs.

In the MIMOC architecture, the control and data planes are decoupled, network intelligence and state are logically centralized, and the underlying network infrastructure was abstract from the applications. As a result, enterprises and carriers gain unprecedented programmability, automation, and network control, enabling them to build highly scalable, flexible networks that readily adapt to changing business needs. An example of an Ideal MIMOC block diagram is shown in Figure 1.

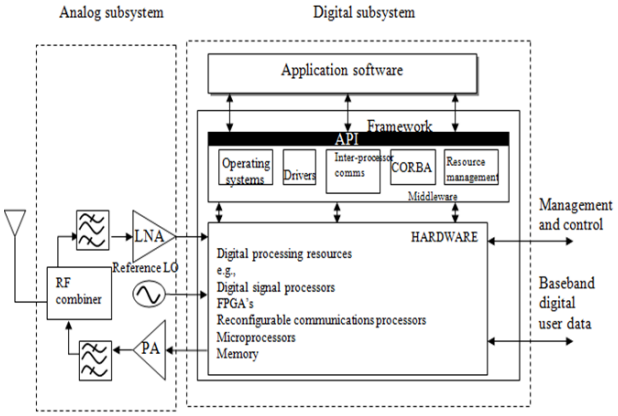

Fig 1: Ideal MIMOC

3. MODULE FOR MIMOC EXPERIMENT
The module for MIMOC experiment is developed using STM32 family. The STM32 family of 32-bit Flash microcontrollers based on the ARM Cortex™-M processor is designed to offer new degrees of freedom to MCU users. It offers 32-bit product range that combines high performance, real-time capabilities, digital signal processing, and low-power, low-voltage operation, while maintaining full integration and ease of development. The unparalleled and large range of STM32 devices, based on an industry-standard core and accompanied by a vast choice of tools and software, makes this family of products the ideal choice, both for small projects and for entire platform decisions. The STM32F103xx (Figure 2) medium-density performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general-purpose 16-bit timers

and one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN. The devices operate from a 2.0 to 3.6 V power supply. They are available in both the –40 to +85°C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

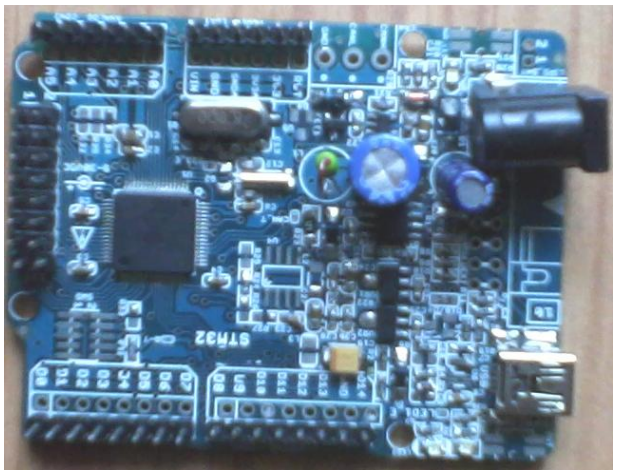

Fig 2: Circuit module of STM32F103RB

4. DESIGN OF TRANSMITTER AND RECEIVER

The transmitter acts under the physical layer of OSI model. It enhances the error detection and control mechanisms using LRC. It reads the input frames given by the user and converts into a framing sequence. The Arm processor is configured to act as a error detection and correction unit for the physical layer [6]. The hardware (Figure 3) functions as a self-healing physical layer implementation in future embedded web server. The Receiver receives the information, detects and corrects errors and retransmits it to the side-by-side configured server system. The hardware implementation of the error recovery block on the ARM processor along with the data recovered output is shown in appendix -1.

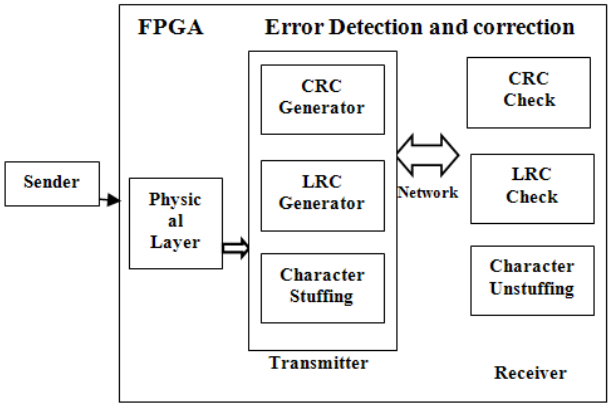

Fig3: Architecture of error detection using FPGA in Physical layer

The receiver takes the input and gives an acknowledgement to the received data before the next sequence is transmitted. During any error, an out of sequence error message is displayed.

5. PERFORMANCE OF LONGITUDINAL REDUNDANCY CHECK

A longitudinal redundancy check (LRC) is a form of redundancy check that is applied independently to each of a parallel group of bit streams. The data is divided into transmission blocks, to which the additional check data is added [10]. While simple longitudinal parity can only detect errors, it can be combined with additional error control coding schemes, such as a transverse redundancy check, to correct the errors [13]. The architecture in Figure 4 represents the LRC generation method for the binary data using both 1's and two's complement.

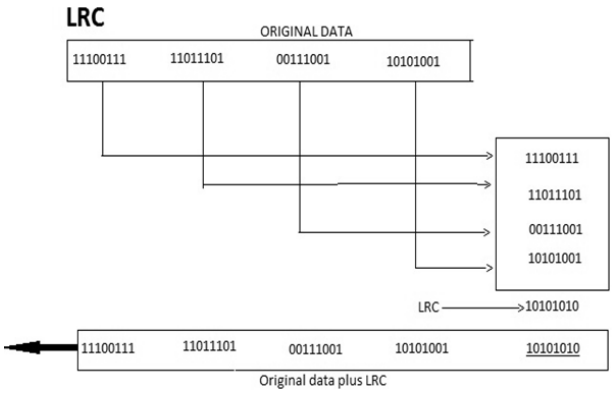

Fig 4: Schematic diagrams for LRC generation mechanism

5.1 Implementation of LRC

```
LRC = Calc_LRC(data, (int)strlen(data));
{
        printf("LRC is %u",LRC);
        getchar();
        return;
 }
unsigned char Calc_Crc(unsigned char *Arr, int count)
{
  unsigned char LRC = 0x00;
  int index;
  for (index = 0; index < count; index++)
        {
            LRC = (byte)(Arr[index] + LRC);
        }
 LRC = (byte)(0xFF - LRC); // 1's complement
 LRC = (byte)(LRC+1);      // 2's complements
 return (LRC);
}
```

6. CHANNEL ESTIMATOR

The communication channel is modeled as a nonlinear amplifier. A MLP neural network architecture is used to "undo" the channel nonlinearities by performing the mapping that is an inverse of the one introduced by the channel. The input sequence used for training is selected such that, it spans the entire amplitude range of the input signal. Otherwise, the network shall be driven into saturation, and this can be a cause of even more severe distortion than the one introduced by the channel itself. In this work, this is removed using data normalization. Higher nonlinearity effects in the channel are taken care by increasing the number of hidden neurons. Two test signals given in eqn. (1) and eqn. (2) are chosen to test the estimator.

s1 = 0.8*sin(2*pi*n/10)+0.25*cos(2*pi*n/25); … (1)
s2 = randn(1,100); … (2)

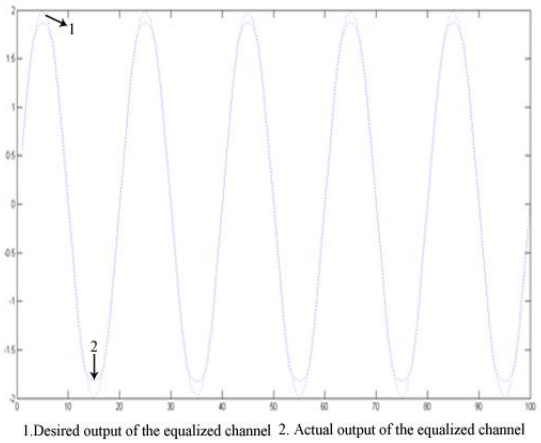

Fig 5(a): Comparison of the desired and actual channel output of the equalized channel to the training signal
x-axis – time samples in sec
y-axis – amplitude in V

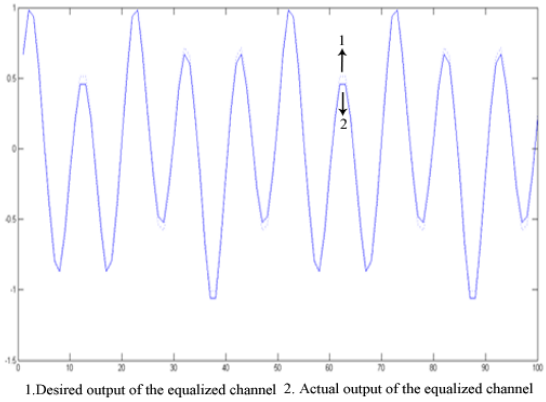

Fig 5(b): Comparison of the desired and actual channel output of the equalized channel to the test signal s_1 (n)
x-axis – time samples in sec
y-axis – amplitude in V

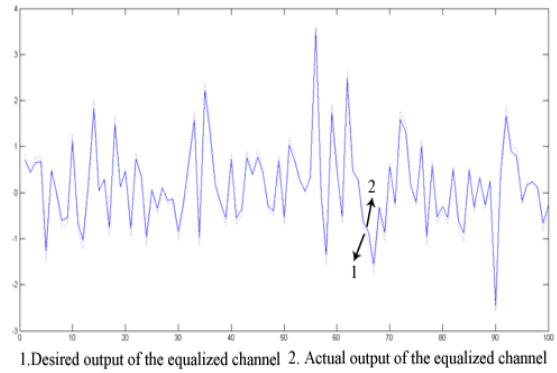

Fig 5(c): Comparison of the desired and actual channel output of the equalized channel to the test signal s_2 (n)
x-axis – time samples in sec
y-axis – amplitude in V

7. Noise Filter at Receiver

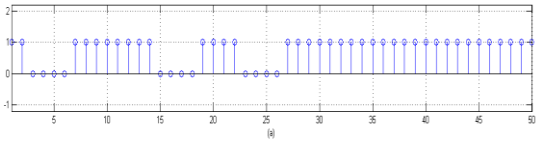

Fig 6(a): original data sequence
x-axis – time samples in sec
y-axis – amplitude in V

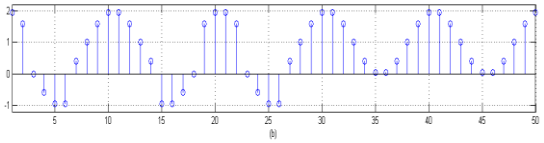

Fig 6(b): Data corrupted with interference signal
x-axis – time samples in sec
y-axis – amplitude in V

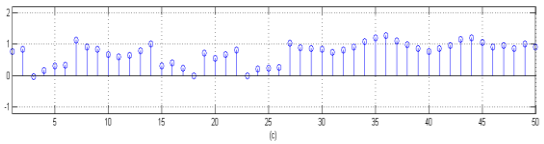

Fig 6(c): Filtered data (using trained Adaline network)
In fig. 5 and 6: x-axis – time samples in sec
y-axis – amplitude in V

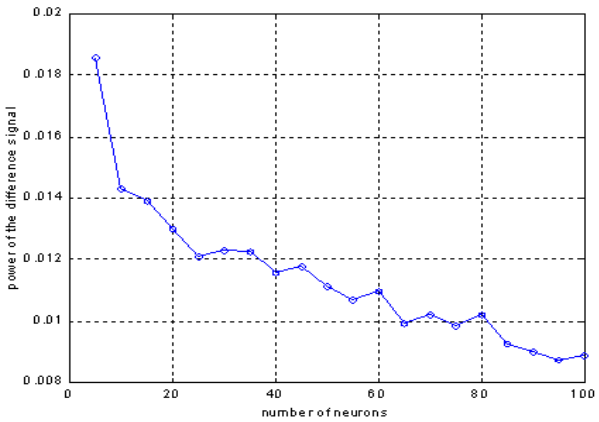

Fig 7: Power of the difference between the original and filtered signal as a function of number of Adaline neurons

8. LRC IMPLEMENTATION RESULTS

Initially, it reads the IP Address and takes the text to form the frame and generate the table with byte and ASCII values. Figure 8(a) represents the LRC value using the table value and in Figure 8(b) at the receiver, the LRC is re-calculated using the received data and checked for matching.

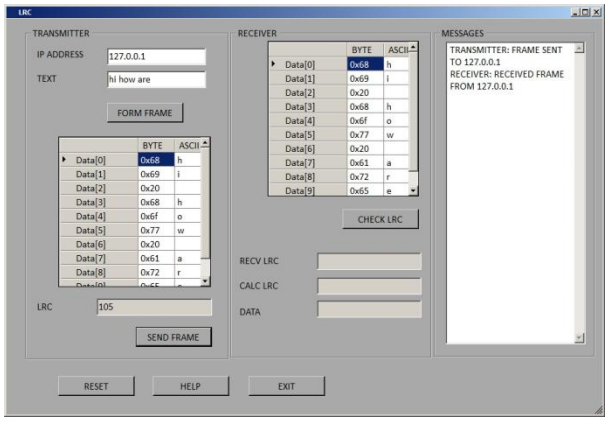

Fig 8 (a): view of LRC Transmitter message

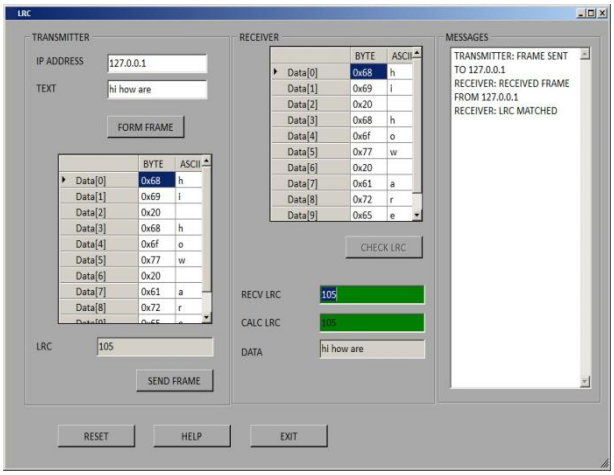

Fig 8(b): LRC matching check at receiver

Table1. Performance Metrics

Performance Metrics																			
Distance (M)	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95	100
Loss (%)	4	4.5	4.9	6.5	9.5	4.7	5.3	1.9	1.8	2.3	2.2	2.4	3.4	4.0	1.1	1.2	1.3	1.8	1.9	2.1
Utilization (%)	65	65	64	63	63	39	38	17	17	17	16	16	16	16	9	9	9	9	9	9
Tx Time(S)	1.7	1.7	1.7	1.7	1.7	2.2	2.2	5.9	5.9	5.9	5.9	5.9	5.9	5.9	11.8	11.8	11.8	11.8	11.8	11.8

Note:

Modulation 1 @ 10 Mbps Data Rate
Modulation 2 @ 5 Mbps Data Rate
Modulation 3 @ 2Mbps Data Rate
Modulation 4 @ 1 Mbps Data Rate

9. CONCLUSION

The approach described in this work auto-generates self-validating models from partial specification of the system there by providing annotations in the implementation itself. The proposed approach thus makes it easier to maintain correspondence between the error detection schemes, which is difficult to achieve in manual verification methods. It also brings the advantages of explicit-state model checking to the verification and error correction in OSI network applications. To mitigate the errors introduced due to the interference automatic error detection and correction schemes for physical layer models is presented. The reconfigurable architecture enables the addition of new features, allows rapid implementation of new standards and protocols on an as-needed basis and protects the investment in computing hardware. It functions as a programmable hardware with higher performance and allows the flexibility of a software based solution while retaining the execution speed of a more traditional hardware based approach.

10. ACKNOWLEDGEMENT

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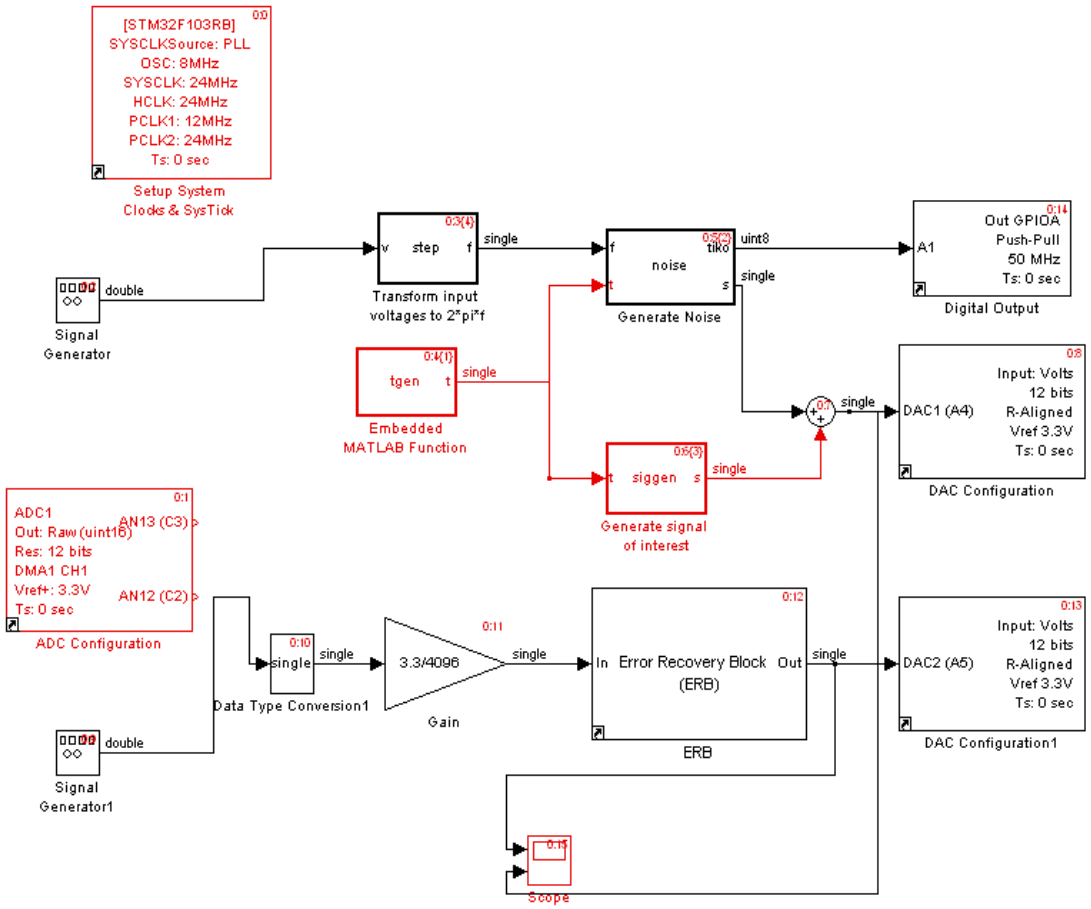
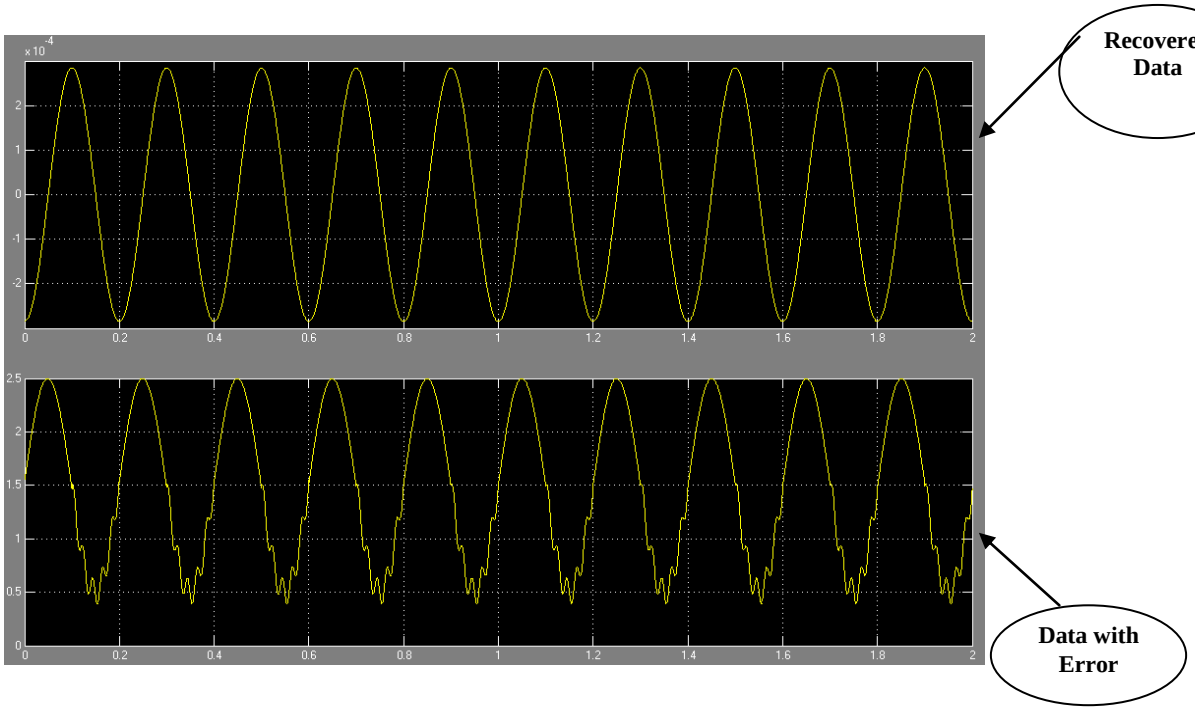


Appendix -1


Recovered Data
Data with Error