Performance Analysis of CNFET based Interconnect Drivers for Sub-threshold Circuits

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ABSTRACT
Subthreshold VLSI circuits design received ample interest due to rapid growth of portable devices. The portable domain places in flexible limitation on the power dissipation. Though, device operating in subthreshold region shows huge potential towards satisfying the ultra low power requirement, it holds lots of difficult design issues. As integration density of interconnects increases at every technology node, increased delay and crosstalk effects may comes a more challenging design problem particularly for subthreshold interconnects. Nanometer subthreshold global interconnect faces subthreshold driver design challenges and problems due to increased interconnect capacitance. This paper examined use of CNFET based interconnect driver even for ultra low power circuits and compared the performance with Si-MOSFET based interconnect driver. It has been reported that CNFET driver provides 9.74 times lower EDP over Si-MOSFET based driver. It also reported better combination of number of tubes, inter CNT pitch and tube diameter for lower delay and EDP.

General Terms
Interconnect design

Keywords
Subthreshold interconnect, Ultralow power, Carbon Nano tube Field Effect Transistor

1. INTRODUCTION
Semiconductor devices are aggressively scaled in each technology node to obtain the higher speed of devices and to increase the maximum number of devices on chip. CMOS technology scaling helps in achieving the desired speed but at the cost of increased power dissipation [1-3]. However, there is a special class of emerging ULP applications like body sensor networks, RFIDs, pacemaker, etc. that do not require high speed. The primary motivation for these applications is ULP consumption so as to prolong the battery life or to employ energy harvesting effectively [4-6]. It is evident from Figure 1 that there is a significant power requirement gap between the high performance microprocessor chip and portable low power systems. To satisfy the ULP demand of these applications, it is necessary to operate the circuit under subthreshold condition [4]. Subthreshold operating region shows great prospective towards fulfilling the ULP demand of portable devices, however, speed of ULP circuit is very low and it limits further expansion of subthreshold circuits in real time applications. The scaling of semiconductor technology node negatively affects the interconnect performance at deep nanometer technology node.

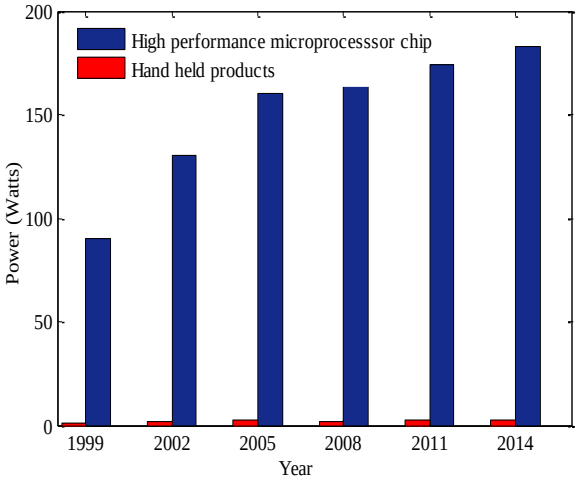

Fig 1: Power requirements of high performance microprocessor chip and handheld products as per ITRS [16].

In subthreshold region, electromigration is insignificant due to lower current density (<< 0.5 − mA/μm) [2] of drive current. Long interconnects poses several design challenges due to increased chip size and interconnect capacitance at every technology node with only a few potential solutions. Numerous research works has been modeled on global interconnects design for superthreshold circuits [3-5]. However, very few publications has been modeled the interconnect design challenges under subthreshold conditions. Interconnect resistance is get dominated by the device resistance under subthreshold conditions. Hence, it is essential to explored appropriate interconnects driver to enhance the speed. This provides an opportunity to optimize and compare the performance of Carbon Nano Tube devices (CNFET) as an interconnect driver. This paper is organized as below. Section 2 introduces subthreshold operating domain. Section 3 introduces the interconnect geometry considered for result analysis. Section 4 focuses on CNFET model. Section 5 explores the performance analysis and section 6 draws conclusion.

2. SUBTHRESHOLD OPERATING REGION
Subthreshold operating region uses subthreshold leakage current as switching current (I_{sub}) as shown in Figure 2. This enables the ULP circuit design to enhance the battery life-time. I_{Sub} through Si-MOSFET is given by [3],

$$I_D = I_0 e^{\frac{(V_{GS}-V_{th}+\eta V_{DS})}{nV_T}} (1-e^{\frac{-V_{DS}}{V_T}}) \quad \ldots\ldots\ldots 1$$

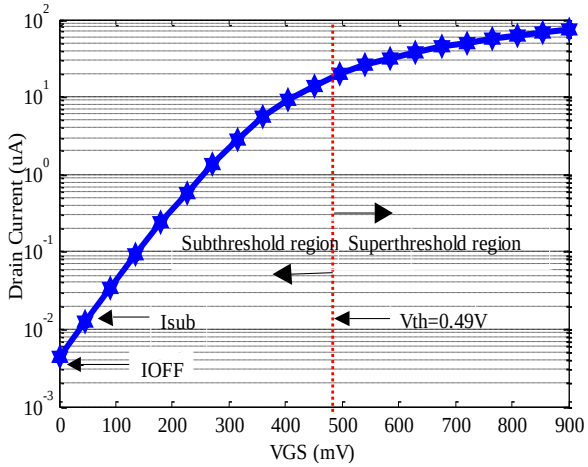

Fig 2: I-V characteristics of NMOS transistor.

Where 'V_{th}' is the transistor threshold voltage, 'n' is the subthreshold slope factor ($n=1+C_d/C_{ox}$), 'V_T' is the thermal voltage, 'η' is DIBL coefficient and 'I_0' is the drain current at $V_{GS}=V_{th}$ @ $V_{DS}=V_{DD}$.

3. INTERCONNECTS TEST SETUP

The propagation delay of an RLC line driven by CMOS driver with driver resistance R_{tr} and a load capacitance C_L can be expressed as follows[7],

$$\Gamma_d = R_{driv}(C_{driv}+C_{load}) + 0.4R_W C_W L^2 + (R_{driv}.C_W + R_W C_{load})L \quad \ldots\ldots\ldots\ldots 2$$

R_{driv} is driver resistance, C_{driv} is driver capacitance, R_w and C_w are interconnects resistance and capacitance, and C_{load} is the load capacitance. R_{driv} increases exponentially as V_{DD} scales below the V_{th} and it is very high as compared to interconnect resistance (R_W) of global interconnect. However, C_{driv} is very small as compared to global interconnects capacitance (C_W). Hence from (1) and (2), in subthreshold region global interconnect delay is dominated by driver resistance and interconnect capacitances. Interconnect geometry as shown in Fig. 3 is used to explored performance analysis of CNFET based interconnects drivers. Equivalent RLC circuit model is used for HSPICE simulation. The equivalent RLC parameters of Cu interconnect is extracted using PTM [8] at 32nm using interconnect geometry parameters suggested by ITRS [9].

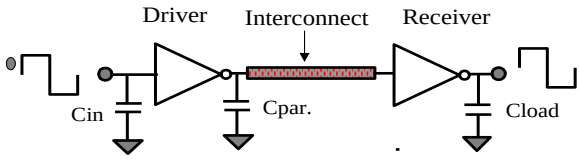

Fig 3: The test structures used for interconnect analysis.

4. CNFET DEVICE STRUCTURE

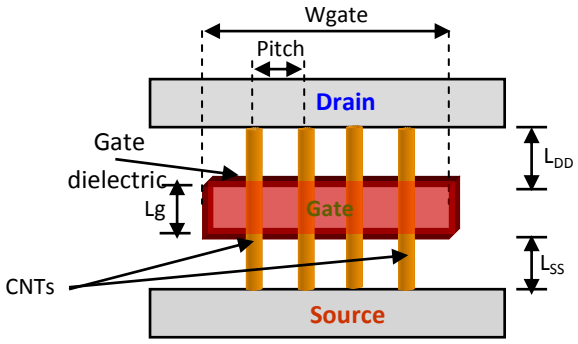

Fig 4: Three-level hierarchy of CNFET model.

A circuit-compatible CNFET model from Stanford University is used for the simulation purpose [11]. It provides improved accuracy by accounting for several practical non-idealities, such as scattering, effects of the doped source/drain extension region, and inter-CNT charge screening effects. A MOS-like representative structure of n-type CNFET is as shown in Figure 4. The semiconducting intrinsic CNT, shown in Figure 4, under the gate acts as the channel and heavily doped CNT regions outside the gate forms the source/drain extension regions. The third level CNFET model is shown in Figure 4 [12]. 'W_{gate}' is the width of the metal gate, channel length (L_g) =32 nm and source drain under-lapped $L_{SS}=L_{DD}$=32 nm. This work considered a planar gate structure with multiple cylindrical conducting channels and high-k gate dielectric material on a substrate with a different dielectric constant (k_1=16 and k_2=3.9). The k_1 and k_2 are the dielectric constants of the gate oxide and insulating bulk oxide respectively. The diameter of the cylinder (tube) is'd'. The normal distance between the CNT center and gate i.e. (thickness of gate dielectric oxide) is denoted by 'h', and the distance between the centers of the two adjacent parallel CNTs is denoted by inter CNT pitch 'P'.

5. PERFORMANCE ANALYSIS

As driver resistance is very high under subthreshold conditions, it is essential to investigate the performance of different interconnect drivers to increase the speed and energy delay product (EDP). This section investigates the performance of CNFET based interconnect driver for different interconnect length. The drive current, and hence the speed of CNFET, is a function of the number of tubes per device (n), tube diameter, device transconductance (g_{CNFET}), V_{DD}, V_{th}, and voltage drop across the doped source region (V_{SS}) [11, 12]. The power dissipation and the speed of CNFET device are mainly governed by 'n', tube diameter and inter CNT pitch. Hence, this section investigates the effect of number of tubes and inter CNT pitch on CNFET based interconnect driver performance. For 32nm CNFET device, we have considered two different numbers of tubes and pitch ratio (N/P).

It is observed that CNFET device with N/P=8/4 provides 34% higher speed and 1.74 times lower EDP over N/P=4/8 at 100 µm interconnect length as shown in Figure 5 and Figure 6 respectively. Figure 7 and Figure 8 shows effect of N/P ratio on global interconnect length upto 5 mm. It has been observed that CNFET based interconnect driver with N/P=8/4 provides lower delay and EDP. Hence, for further analysis and comparison of CNFET based interconnects N/P=8/4 is considered for lower delay and EDP.

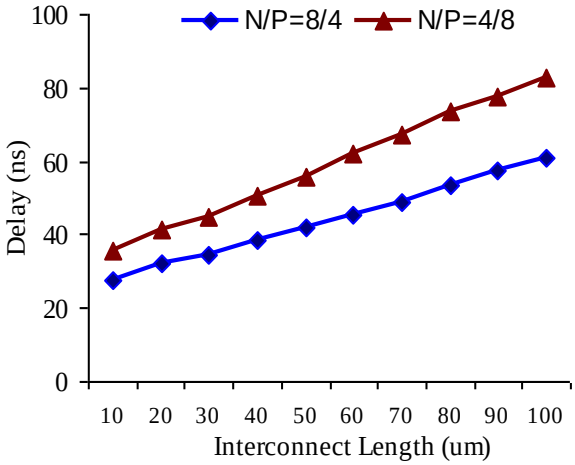

Fig 5: Delay as function of number of tubes and pitch.

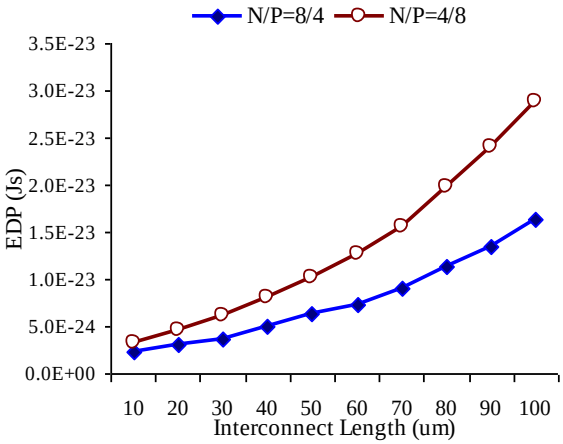

Fig 6: EDP as function of number of tubes and pitch.

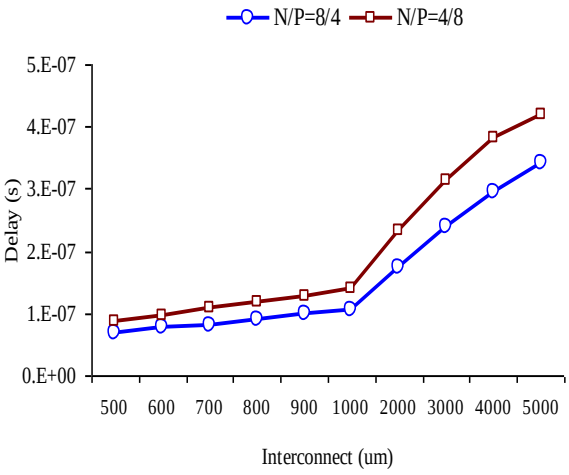

Fig 7: Comparison of delay at different interconnect length.

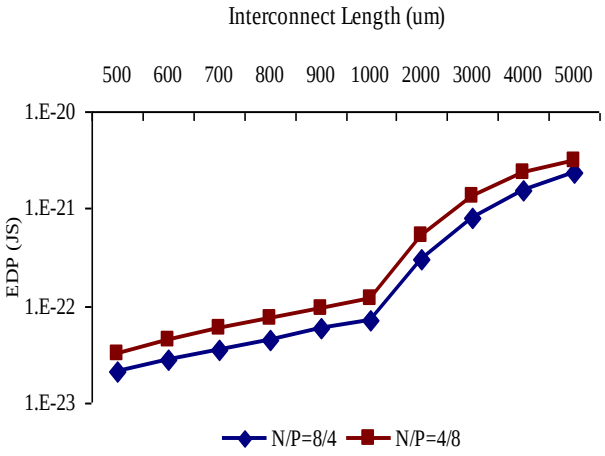

Fig 8: Comparison of EDP at different interconnect length.

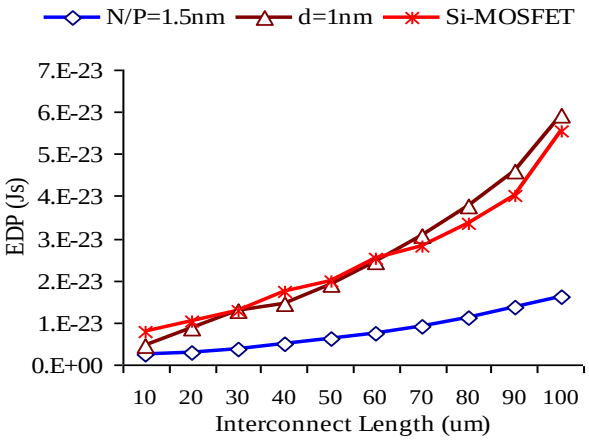

Fig 9: Comparison of EDP for short and intermediate interconnect length.

However, CNFET threshold voltage is depends upon CNT diameter. Hence, to produce fair comparison we have kept same delay for all three drivers (CNFET with N/P=8/4, N/P=4/8 and Si-MOSFET) by adjusting the V_{DD} for different interconnect length. It is well established that CNFET drive current is strong function of CNT diameter. Hence, it is essential to explore the effect of tube diameter on interconnect performance.

Figure 9 shows EDP performance at various interconnect length for CNFET with tube diameter (d) 1.5 nm and 1nm. It also compares the EDP performance with Si-MOSFET driver. It has been reported that CNFET with d=1.5 nm shows 2.8 times lower EDP over d=1 nm at 50 µm interconnect length. In addition, it is observed that delay performance of CNFET with d=1 nm and Si-MOSFET is almost comparable.

Furthermore, Figure 10 compared the performance of CNFET with different tube diameter and Si-MOSFET. It is observed that CNFET with diameter of 1.5 nm provides 9 times lower

EDP over Si-MOSFET and CNFET with 1 nm tube diameter at same delay for 1000 µm.

From above analysis, it is observed that CNFET with 1.5 nm tube diameter provides excellent performance over Si-MOSFET.

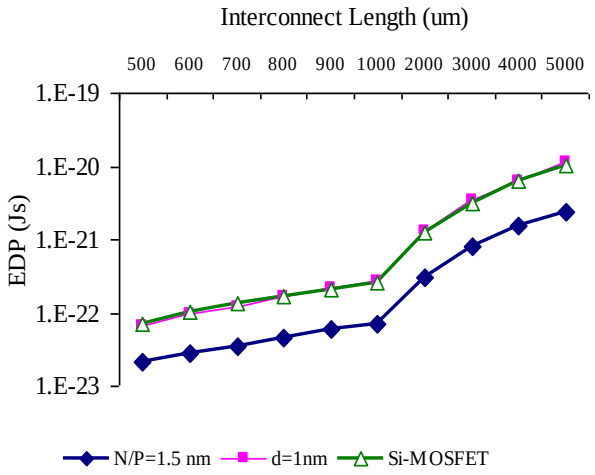

Fig 10: Comparison of EDP for global interconnect length

6. CONCLUSION

Interconnects delay may cause functionality failure of ultra low power digital systems. Recently, research for ultralow power is mainly focused at designing of subthreshold circuits. However, interconnects for subthreshold logic remains unfocused for long times and needs more attention for better performance even at very low supply voltage. Specially there is need to reduce global interconnect delay. This paper put efforts towards reducing the delay and EDP for different interconnect length using interconnects drivers with emerging nano devices. This paper has been successively reported that CNFET based drivers provides significant improvement in EDP and delay for different interconnect length over Si-MOSFET at appropriate geometry parameters.

7. REFERENCES

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