Low Power High Speed 16x16 bit Multiplier using Vedic Mathematics

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ABSTRACT

High-speed parallel multipliers are one of the keys in RISCs (Reduced Instruction Set Computers), DSPs (Digital Signal Processors), and graphics accelerators and so on. Array multiplier, Booth Multiplier and Wallace Tree multipliers are some of the standard approaches used in implementation of binary multiplier which are suitable for VLSI implementation.

A simple digital multiplier (henceforth referred to as Vedic Multiplier in short VM) architecture based on the Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra of Vedic Mathematics is presented. An improved technique for low power and high speed multiplier of two binary numbers (16 bit each) is developed. An algorithm is proposed and implemented on 16nm CMOS technology.

The designed 16x16 bit multiplier dissipates a power of 0.17 mW. The propagation delay time of the proposed architecture is 27.15ns. These results are many improvements over power dissipations and delays reported in literature for Vedic and Booth Multiplier.

Keywords

Vedic Multiplier, Urdhva Tiryakbhyam, CMOS Technology, Power Dissipation, Propagation Delay.

1. INTRODUCTION

The ancient system of Vedic Mathematics was rediscovered from the Indian Sanskrit texts known as the Vedas, between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884-1960) from the Atharva Vedas. According to his research all of mathematics is based on sixteen Sutras, or word-formulas [1]. These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. In the Vedic system difficult problems or huge sums can often be solved immediately by the Vedic method. These striking and beautiful methods are just a part of a complete system of mathematics which is far more systematic than the modern system. Vedic Mathematics manifests the coherent and unified structure of mathematics and the methods are complementary, direct and easy. It's a unique technique of calculations based on simple principles and rules , with which any mathematical problem - be it arithmetic, algebra, geometry trigonometry, or even calculus can be solved mentally[2].

In this paper a simple 16 bit digital multiplier is proposed which is based on Urdhva Tiryakbhyam (Vertically Crosswise) Sutra of the Vedic Maths. Two binary numbers (16-bit each) are multiplied with this Sutra. The potential of this method is that the power dissipation of this circuit is 0.17 mW. & propagation delay of the proposed architecture is 27.15ns. These results are improvements over power dissipations and delays reported in literature for Vedic and Booth Multiplier. Array multiplier, Booth Multiplier and Wallace Tree multipliers are some of the standard approaches used in implementation of binary multiplier which are suitable for VLSI implementation.

Table (1): Comparison of Different Conventional Multipliers

Parameter	Array Multiplier	Wallace Tree Multiplier	Booth's Multiplier
Operation Speed	Less	High	Highest
Time Delay	More	Medium	Less
Area	Maximum area because it uses a large number of Adders	Medium area because Wallace Tree used to reduce Operands	Minimum area because no of adder/subtractor is small/
Complexity	Less complex	More complex	Most complex
Power Consumption	Most	More	Less
FPGA implementation	Less efficient	Not efficient	Most efficient

In the section 2 introduction of the method will be discuss, with the description of the Sutra, steps of multiplication. In section 3 design of the 16x16 bit multiplier with the basic building blocks like 2x2 bit Multiplication, 4x4 bit multiplication, 8x8 bit multiplication. In section 4 we state the comparison of different multiplier. In section 5 we conclude.

2. Introduction to Proposed Technique

2.1 Design Factors of Multiplication: Latency, throughput, area, and design complexity are the important factors to choose a suitable design for the requirement. Latency is a measure of how long the inputs to a device are stable until the final result available on outputs. Throughput is

the measure of how many multiplications can be performed in a given period of time**.**

2.2 Urdhva Tiryakbhyam Sutra[2]

The basic Sutras and Urdhva Tiryakbhyam Sutra in the Vedic Mathematics helps to do almost all the numeric computations in easy and fast manner[3]. The Sutra which we employ in this project is Urdhva Tiryakbhyam (Multiplication)

2.3 Description of Sutra[2]

This is the general formula applicable to all cases of multiplication [3]. Urdhva Tiryakbhyam means "Vertically and Crosswise", which is the method of multiplication followed.

Illustration:

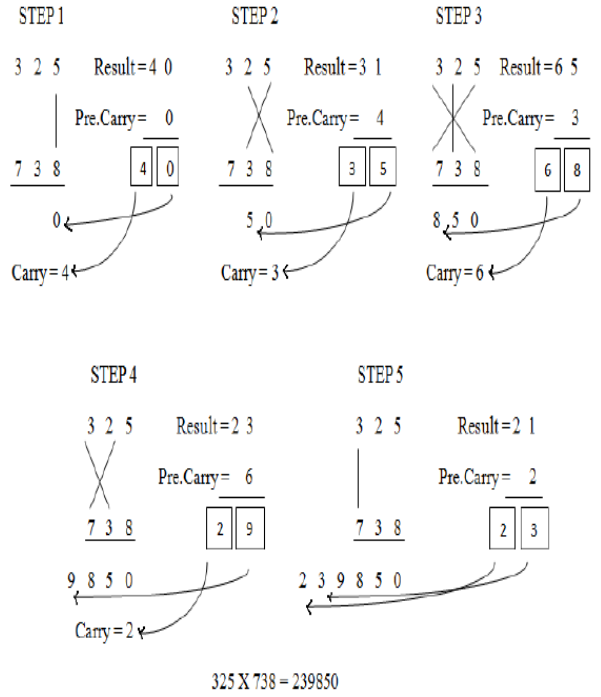

Figure (1): Multiplication of two decimal numbers by Urdhava Tiryakbhyam Sutra [1]

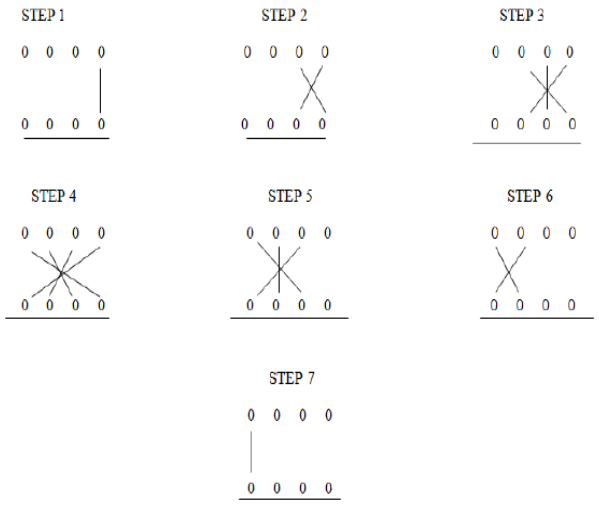

Figure (2): Line diagram for multiplication of two 4 – bit numbers[1].

3. Design Of The 16x16 Multiplier

3.1 The Fundamental Block (2×2 block)

In the design of the proposed Vedic multiplier a 2×2 block is a fundamental block (Basic block) is shown in fig 3. Also symbol of this fundamental block is shown to be used in 4 x 4 bit Multiplier. We know that in binary multiplication basically we AND each two bits in 2-input AND gate[4]. First off all vertical bits (LSBs) are ANDed this will result in the LSB of the result. Than we and crosswise bits and then result is added using a half adder. The sum output of the half adder is the next bit of the result right to the LSB. The carry output is also added in half adder with the AND output of the MSBs. The carry of this adder is the MSB of the result. The waveforms of input and output of 2-bit multiplier using Urdhva Tiryakbhyam Sutra [5] of Vedic mathematics is shown in figure 4. Power dissipation of this multiplier is 23.2 µW and propagation delay is 1.51 nsec. 62 transistors are used in this design.

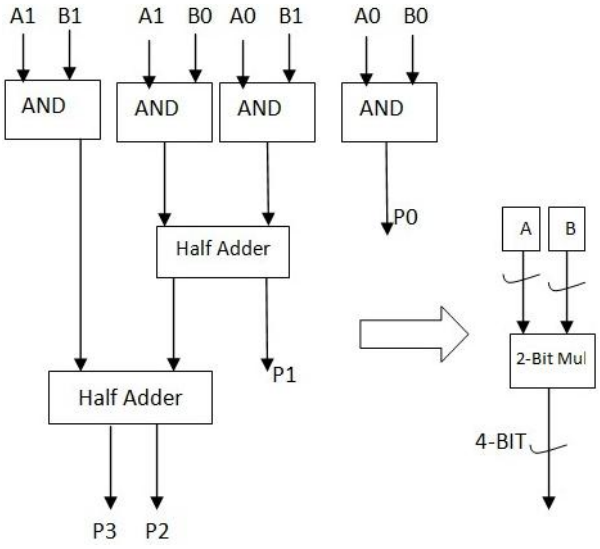

Figure (3): 2-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

Figure (4): Input Output waveforms of 2x2 Bit multiplier

3.2 Design of 4×4 block

The design of 4×4 block shown in fig (5) is a simple arrangement of 2×2 blocks in an optimized manner. The first step in the design of 4×4 block will be grouping the 2 bit of each 4 bit input. These pair terms will form vertical and crosswise product terms. Each input bit-pair is handled by a separate 2×2 Vedic the schematic of a 4×4 block designed using 2×2 blocks. The partial products represent the Urdhva vertical and cross product terms. Then using or and half adder assembly to find the final product. Power dissipation of this multiplier is 0.18 mW and propagation delay is 1.71 nsec. 618 transistors are used in this design

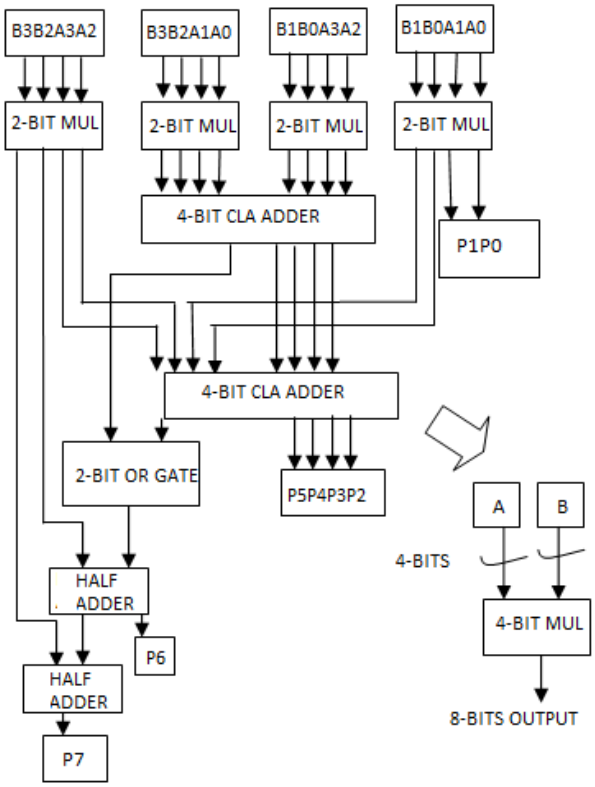

Figure (5): 4-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

3.3 Design of 8×8 block

The design of 8×8 block is a similar arrangement of 4×4 blocks in an optimized manner as in figure 3. The first step in the design of 8×8 block will be grouping the 4 bit (nibble) of each 8 bit input. These quadruple terms will form vertical and crosswise product terms. Each input bit-quadruple is handled by a separate 4×4 Vedic multiplier to produce eight partial product rows. These partial products rows are then added in an 8-bit carry look ahead adder optimally to generate final product bits.

The figure (6) shows the schematic of an 8×8 block designed using 4×4 blocks. The partial products represent the Urdhva vertical and cross product terms. Then using or and half adder assembly to find the final product. Power dissipation of this multiplier is 0.035mW and propagation delay is 1.72 nsec. 3222 transistors are used in this design.

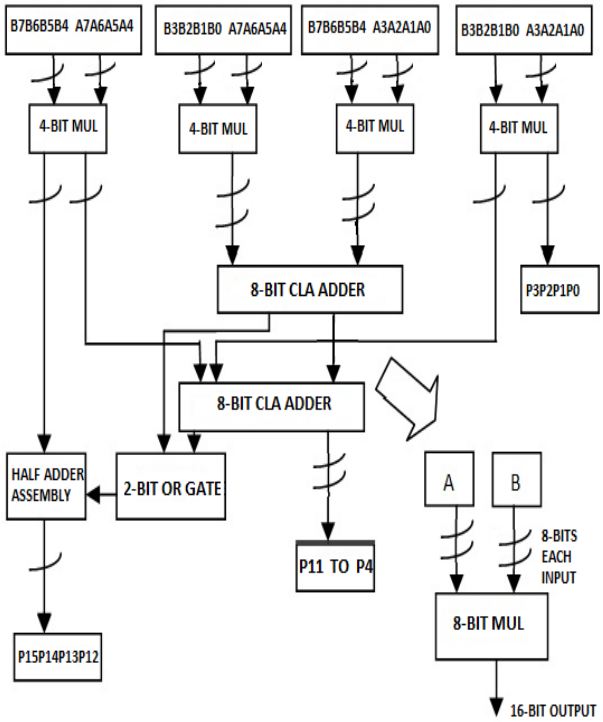

Figure (6): 8-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

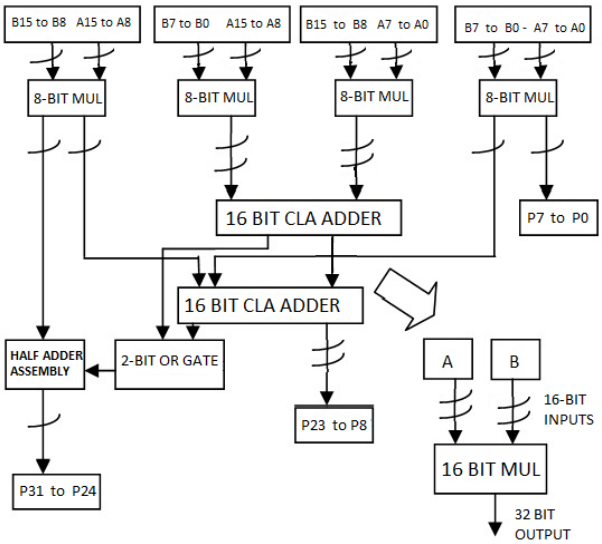

Figure (7): 16-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

3.4 Design of a 16×16 Multiplier

The design of 16×16 block is a similar arrangement of 8×8 blocks in an optimized manner as in figure (7). The first step in the design of 16×16 block will be grouping the 8 bit (byte) of each 16 bit input. These lower and upper bytes pairs of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are then added in a 16-bit carry look ahead adder optimally to generate final product bits. The figure 5 shows

the schematic of a 16×16 block designed using 8×8 blocks. The partial products represent the Urdhva vertical [6] and cross product terms. Then using or and half adder assembly to find the final product. Power dissipation [7] of this multiplier is 0.18 mW and propagation delay is 1.71 nsec. 618 transistors are used in this design.

4. CONCLUSION

The proposed Vedic multiplier (discussed in section 3) is simulated using Tanner Tool v14.1. The Comparison between proposed multiplier and Booth radix-4 multiplier and the multiplier in [3] is shown in table (2). As from the table this multiplier helps in future to make fast processors. Schematic from S Edit is shown in figure (8).

Table (2): Table of design comparison of Multipliers

S.No.	Parameters of Comparison	Paper [3] design	Booth algorithm	Proposed design
1	Delay (n sec)	37.668	46.740	27.14865
2	Power Dissipation (m Watts)	29.34	151.34	0.1692638
3	No. of Transistors used	4299	7296	14382

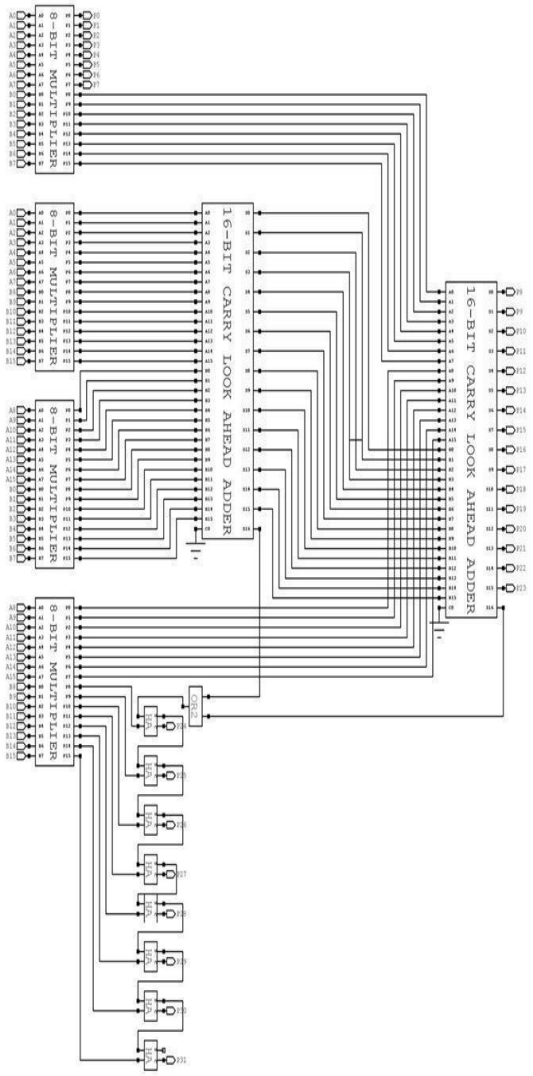

Figure (8): Schematic diagram of 16 bit Multiplier using Urdhva Tiryakbhyam Sutra

5. REFERENCES

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