Second Order Mixed Mode Quadrature Oscillator using DVCCs and Grounded Components

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ABSTRACT

A new mixed-mode second order quadrature oscillator using two differential voltage current conveyors as active elements, two grounded capacitors and two grounded resistors each is proposed. The circuit provides several current and voltage outputs simultaneously. The circuit has low active and passive sensitivities. Non-ideal and parasitic study of the proposed circuit is also included. PSPICE simulation results are given to validate the proposed circuit.

General Terms

Analog signal processing, Mixed mode circuits

Keywords

Oscillators, Differential Voltage Current Conveyor

1. INTRODUCTION

Current conveyor (CC) is an important and versatile current mode active building block, which has received considerable attention in last two decades as an alternative to the voltage mode operational amplifier. When arranged with other electronic elements, it can be used for the implementation of various functions operating either in voltage-mode or current-mode. It has been considered superior to operational amplifier and can offer higher design flexibility. Current conveyor offers many advantages such as higher voltage gain over a large signal bandwidth thus resulting in larger gain-bandwidth-product without trade off, wider dynamic range, low power consumption and higher slew rates [1 – 3].

Sinusoidal quadrature oscillators have a wide range of applications in telecommunications, power electronics and signal processing and measurement systems. As a result, a number of circuits have been presented in the technical literature which provide voltage output(s), current output(s), both voltage as well as current output(s), with a certain phase shift giving rise to quadrature and multiphase oscillators [4 – 23]. In the last few years, differential voltage current conveyor (DVCC) has also become popular for realizing various analog electronic functions including oscillator circuits [9 – 15]. It may be noted that the circuits with both voltage and current outputs have also been termed as mixed mode oscillators [16 – 21].

In this paper, a new mixed mode second order quadrature oscillator based on DVCCs is presented. The proposed circuit employs two DVCCs, two grounded capacitors and two grounded resistors. The use of grounded capacitors and resistors makes the proposed circuit suitable for integrated circuit implementation. Non-ideal and parasitic study is also performed. The proposed circuit also exhibits low active and passive sensitivities. The proposed theory is verified by PSPICE simulation results.

2. PROPOSED CIRCUIT

The symbol and CMOS implementation of differential voltage current conveyor (DVCC) are shown in Fig. 1. DVCC is a five-port building block and is characterized by the following port relationship.

$$V_X = V_{Y1} - V_{Y2}, I_{Y1} = I_{Y2} = 0, I_{Z+} = +I_X, I_{Z-} = -I_X \quad (1)$$

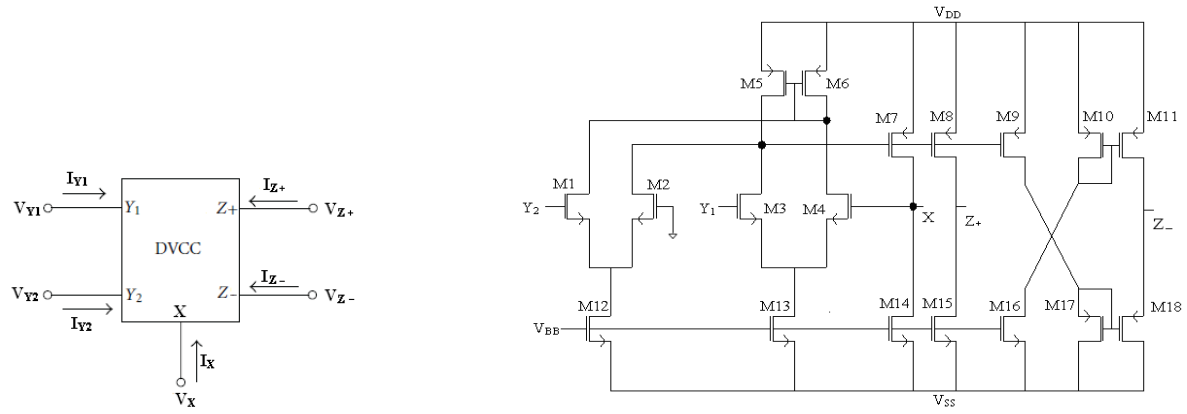
In a DVCC, no current flows in terminal Y_1, Y_2. Thus, terminals Y_1, Y_2 exhibit infinite input impedances. The terminal X exhibits zero input impedance. The Z+ and Z- terminals are high impedance terminals suitable for current outputs. The proposed circuit of mixed-mode second order quadrature oscillator is shown in Fig. 2. It is composed of two DVCCs, two grounded capacitors and two grounded resistors. However, the proposed circuit uses DVCCs with extra Z+ stages, which can be achieved by cascading current follower stages using extra transistors to the available Z+ stage in CMOS implementation of DVCC.
The characteristic equation of the circuit can be expressed as

$$s^2 + s\frac{(C_1R_1 - C_1R_2)}{C_1C_2R_1R_2} + \frac{1}{C_1C_2R_1R_2} = 0 \quad (2)$$

The frequency of oscillation (FO) and condition of oscillation (CO) can be obtained as

FO: $$f_0 = \frac{1}{2\pi\sqrt{C_1C_2R_1R_2}} \quad (3)$$

CO: $$R_1 \leq R_2 \quad (4)$$



(a) **(b)**

Figure 1: (a) Symbol of DVCC (b) CMOS implementation of DVCC

The various voltage and current outputs depicted in Fig. 3 are related as

$$V_2 = -(j\omega C_2 R_1)V_1 \quad (5)$$

$$I_3 = (j\omega C_2 R_1)I_1, I_1 = -I_2 \quad (6)$$

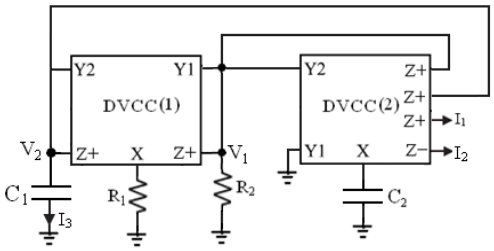
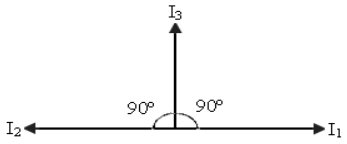


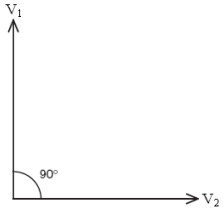
Figure 2: Proposed circuit of mixed-mode second order quadrature oscillator

The sensitivity figures of FO with respect to passive components are low and given in equation (7).

$$S^{f_0}_{C_1,C_2,R_1,R_2} = -\frac{1}{2} \quad (7)$$



(a)



(b)

Figure 3. (a) Phasor diagram depicting quadrature current outputs (b) Phasor diagram depicting quadrature voltage outputs

3. NON IDEAL ANALYSIS

Taking the non-idealities of the DVCC into account, the relationship of the terminal voltages and currents of the DVCC can be rewritten as:

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2}, I_{Y1} = I_{Y2} = 0, I_{Z+} = +\alpha I_X, I_{Z-} = -\alpha I_X \quad (8)$$

Here, β_1, β_2 are the voltage transfer gains from Y_1 and Y_2 terminals respectively to the X terminal. α is the current transfer gain from X terminal to Z terminals. The above transfer gains deviate unity by the voltage and current transfer errors, which are quite small and technology dependent. Moreover, the transfer gains, instead of being real, are actually frequency dependent.

The novel mixed-mode second order quadrature oscillator of Fig. 2 is reanalyzed using equation (8), so as to get modified characteristic equation as:

$$s^2 + s\frac{(C_1R_1 + \alpha_1\beta_{12}C_2R_2(1-\alpha_2\beta_{22}) - \alpha_1\beta_{11}C_1R_2)}{C_1C_2R_1R_2} + \frac{\alpha_1\beta_{12}}{C_1C_2R_1R_2} = 0 \quad (9)$$

The modified frequency of oscillation and condition of oscillation are

$$\text{FO: } f_0 = \frac{1}{2\pi}\sqrt{\frac{\alpha_1\beta_{12}}{C_1C_2R_1R_2}} \quad (10)$$

$$\text{CO: } C_1R_1 \le \alpha_1\beta_{11}C_1R_2 - \alpha_1\beta_{12}C_2R_2(1-\alpha_2\beta_{22}) \quad (11)$$

Here, β_{11}, β_{12} are the voltage transfer gains from Y_1, Y_2 terminal respectively to the X terminal of $DVCC_1$ and β_{22} is the voltage transfer gain from Y_2 terminal to the X terminal of $DVCC_2$. α_1 is the current transfer gain from the X terminal to Z+ terminal of $DVCC_1$ and α_2 is the current transfer gain from the X terminal to Z- terminal of $DVCC_2$. The active and passive sensitivities are shown in equation (12).

$$S^{f_0}_{\alpha_1,\beta_{12}} = -S^{f_0}_{C_1,C_2,R_1,R_2} = \frac{1}{2}, S^{f_0}_{\alpha_2,\beta_{11},\beta_{22}} = 0 \quad (12)$$

The sensitivities of active and passive components are within unity in magnitude. Thus, the new circuit of mixed mode quadrature oscillator exhibits attractive active and passive sensitivity performance.

4. PARASITIC CONSIDERATIONS

A parasitic model of DVCC is shown in Fig. 4. It is shown that the real DVCC has parasitic resistors and capacitors from the Y and Z terminals to ground and also, a series resistor at

the input terminal X. As the X terminal of the $DVCC_1$ is connected to a resistor, the parasitic resistance at the X terminal of the DVCC (R_{X1}) can be absorbed as a part of the main resistance. However, the X terminal of the $DVCC_2$ is connected a capacitor; hence, the parasitic resistor R_{X2} appears in series with it. As the value of R_{X1} and R_{X2} is much smaller then the external components, so frequency of oscillation of the proposed circuit of quadrature oscillator will be less affected. The effects of the capacitors at port Y and Z of the DVCC are also negligible because these capacitors are quite small (and process dependent) as compared to the external capacitors. However, the proposed circuit of quadrature oscillator is re-analyzed taking into account the above parasitic effects. A re-analysis of the proposed circuit of quadrature oscillator yields:

$$As^2 + Bs + C = 0 \qquad (13)$$

where,

$$A = C_2^2 R_{X2} R_1' (Z_2 R_{X2} - Z_2 R_1' - R_1' R_{X2} - Z_1 R_{X2})$$

$$B = C_2 R_1' (2Z_2 R_{X2} - Z_2 R_1' - R_{X2} - R_1' R_{X2} - 2Z_1 R_{X2})$$

$$C = R_1' (Z_2 - Z_1 - R_1')$$

where,

$$R_1' = R_1 + R_{X1}$$

$$Z_1 = (C_1 + C_{Y12} + C_{Z1+} + C_{Z2+}) // (R_{Y12} // R_{Z1+} // R_{Z2+})$$

$$Z_2 = R_2 // (C_{Y11} + C_{Y22} + C_{Z1+} + C_{Z2+}) // (R_{Y11} // R_{Y22} // R_{Z1+} // R_{Z2+})$$

In equation (13), undesirable factors are yielded by the inclusion of parasitics of the DVCC. However, from the above discussion it is to be concluded that the circuit is not adversely affected by the parasitics of the DVCC.

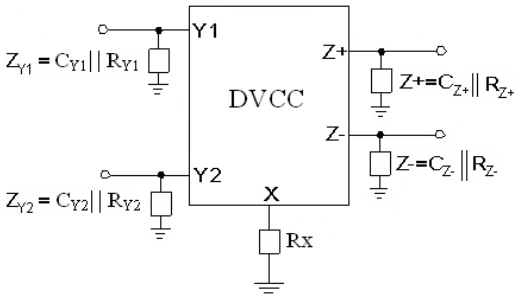


Figure 4. Parasitic model of DVCC

5. SIMULATION RESULTS

The proposed mixed-mode second order quadrature oscillator was next simulated using PSPICE. The DVCC implementation of Fig. 1 was used with the supply voltages as $V_{DD} = -V_{SS} = 2.5V$. The biasing voltage V_{BB} was taken as $-1.4V$. The circuit was designed using equal capacitors of value $C_1 = C_2 = 10pF$, $R_1 = 3.66k\Omega$, $R_2 = 4k\Omega$. The theoretical FO using this design was 4.15MHz. The simulated FO was found to be 4.12 MHz, which is very close to the theoretical value and only 0.72% in error. The results for the three current outputs and two voltage outputs are shown in Fig. 5 and Fig. 7 respectively. The Fourier spectrum of the outputs of Fig. 5 and Fig. 7 are shown in Fig. 6 and Fig. 8 respectively, each output enjoying a total harmonic distortion (THD) of within 1%. To further support the circuit's practical utility, R (for $R_1 = R_2 = R$) was varied so as to vary the FO. The FO tuning through R is shown in Fig. 9. The FO is found to vary from 1.59MHz to 7.96MHz for variation of R from 10KΩ to 2KΩ respectively.

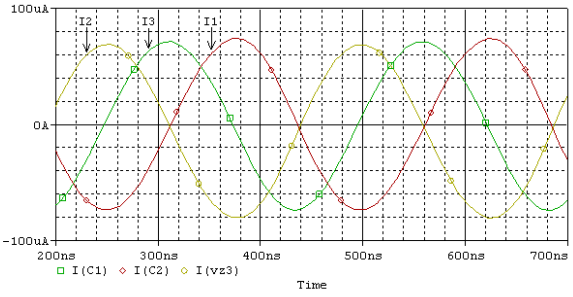


Figure 5. Quadrature current output waveforms

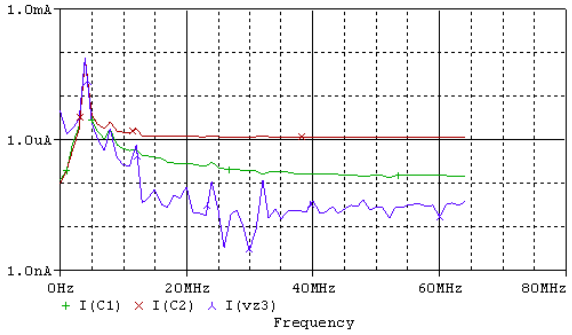


Figure 6. Frequency spectrum of current outputs

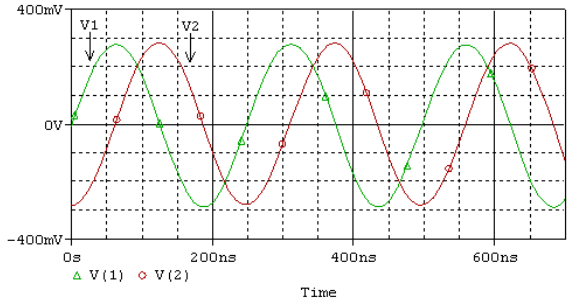


Figure 7. Quadrature voltage output waveforms

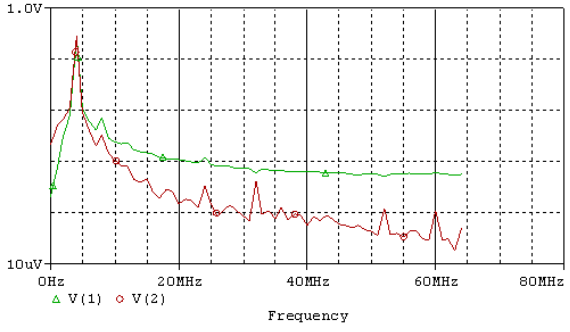


Figure 8. Frequency spectrum of outputs V_1 and V_2

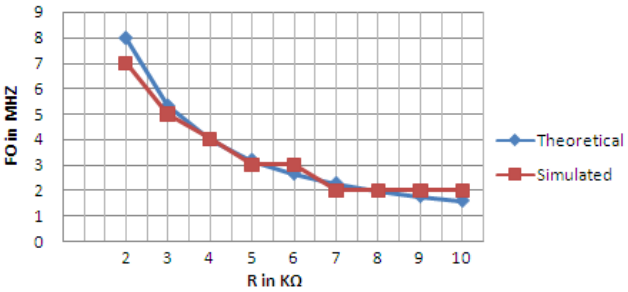


Figure 9. Frequency of oscillation variation with R

6. CONCLUSION

A new mixed-mode second order quadrature oscillator circuit based on two DVCCs as active element, two grounded capacitors and two grounded resistors is presented. The circuit employs all grounded components, ideal for IC implementation. The circuit provides two quadrature voltages and three current outputs. The circuit also exhibits the feature of low THD. Non-ideal analysis and parasitic study is also given. The PSPICE results validate the proposed theory.

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