Reconfigurable Design of GSM Digital down Converter for Enhanced Resource Utilization

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ABSTRACT
In this paper a hybrid approach is presented to design and implement a GSM digital down convertor for enhanced resource utilization. The proposed DDC has been implemented by hybridizing the multiplier less and multiplier based decimators. A multiplier less CIC decimator has been used to reduce the cost by reducing the multiplier requirement. Two computationally efficient equiripple polyphase decomposition structure based decimators have been to reduce the filter order and hardware complexity. The embedded multipliers, LUTs and BRAMs have been efficiently utilized to enhance the system performance and resource utilization. The proposed GSM DDC has been designed and simulated Matlab and Simulink, synthesized with Xilinx Synthesis Tool and implemented on Virtex-II Pro based xc2vp20 FPGA device. The proposed design has shown a minimum period of 159.96 MHz with enhance resource utilization ranging from 4-12 % in terms slices, flip flops LUTs, BRAMs and multipliers.

General Terms
Multirate Signal Processing, Software Defined Radios, Mobile Communication

Keywords
BRAM, DDC, FPGA, LUT, GSM

1. INTRODUCTION
Digital Signal Processors (DSPs) are specialized devices designed to implement digital signal processing algorithms on stream of digitized signals. DSPs are widely used in wireless systems to perform various filtering, encoding, decoding and transform functions. The highly competitive nature of the wireless communications market and constantly evolving communication standards have resulted in short design cycles and product lifetimes. This environment has led to the emergence of a new class of configurable DSPs, which can leverage hardware flexibility, programmability, and reusability, to provide highly customizable DSP solutions [1]. DSPs can broadly be divided into two classes: ASIC and Programmable DSP. ASICs implement complex algorithms in hardware and are used in applications that demand high computational performance. Programmable DSPs on the other hand are used to implement low to medium-complexity algorithms in software, and are mainly used in applications that require good performance at low system costs. For this reason, programmable DSPs are widely used in wireless handsets to perform various baseband processing functions such as filtering, equalization, and echo cancellation [2].

As communication standard evolve and time-to-market pressures yield shorter design cycles, programmable DSPs become more appealing than ASICs due to the ease with which their functions can be modified. However when hardware acceleration is the only approach for satisfying the computational demands of an applications, ASICs maintain their advantage. For high end digital signal processing where the highest possible performance is needed at low power consumption, ASICs are still the processors of choice. However, ASICs require very long design and development times and are very expensive to design and manufacture. Moreover, ASICs are inherently rigid and are not very well suited to applications that are constantly evolving. For these reasons, Programmable Logic Device like Field Programmable Gate Arrays (FPGAs) have emerged as an alternative to ASICs in wireless communication systems.

FPGAs are mainly used for the flexibility they provide. Like programmable DSPs, FPGAs are programmed and configured in software. This makes it very easy to upgrade or add functionality to an FPGA, even if it is already deployed in the field. Like ASICs, FPGAs achieve high levels of performance by implementing complex algorithms in hardware. FPGAs are particularly well suited for accelerating algorithms that exhibit a high degree of data flow parallelism. The FPGAs suffer from the drawbacks of inefficient resource utilization, high cost and power consumption [3]. The cost factor can be improved by using lower end less expensive FPGAs for system design and by efficient utilization of FPGA resources. Continued advances in VLSI fabrication technology and increasing transistor densities have ushered in the era of the system on chip (SoC). Today it is possible to design entire systems, including processors, memories, buses, and interfacing logic on a single silicon chip. By integrating all components on the same chip, execution performance is improved and overall system costs are reduced significantly.

In the recent past, telecommunications techniques have achieved a wide popularity, mainly due to the huge diffusion of cellular phones and wireless devices. The request for more complex and complete services, such as high speed data transmission and multimedia content streaming, has moved many research groups in the electronic field towards the study of new and efficient algorithms, codes and modulations. Software Defined Radio is an emerging technology that has been used to describe radios whose implementation is largely software-based. In a SDR, most radio receiver processing functions to be run on a general purpose (GP) programmable processor rather than being implemented strictly on non programmable hardware.

The functionality of SDR receiver processor can be changed via "software reprogramming." The concept of SDR is now an IEEE Standard i.e. IEEE P1900 [4]. These radios are reconfigurable through software updates. Software defined radios are beginning to find also commercial potential. When the software defined radio becomes main stream, the full potential of adaptability may create possibilities for new kind of services. From the users' point of view, seamless operation across networks, without caring about the underlying technology, would be a very desirable feature. The Second Generation (2G) and Third Generation (3G) systems differ mainly in the channel access technique. The 2G or GSM is basically a TDMA oriented system and 3G is strongly based on CDMA. According to an increasing demand for simultaneous global roaming and all-in-one wireless phones, the interest in the development of the so-called multi-standard transceivers was fostered. One leading solution is the dynamic reconfiguration of the different modules in the system to suit the specifications of as many standards as possible so, the system should be capable of dynamically reconfiguring itself to the environment as needed [5].In this scenario the availability of reconfigurable platforms both for the base stations and mobile terminals will be of great concern. This will enable the possibility to reconfigure the receiver while the user is moving, leading to ubiquitous access to services.

SDR platforms rely heavily on programmable platforms to realize complex architectures and evolving standards. Although cost is a major motivating factor in pursuing this technology, the flexibility of accommodating multiple standards under a single hardware "umbrella" is of particular importance to emergency responders (ER) who are often forced to function in environments where wireless coverage is limited or altogether non-existent [6]. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands [7].

2. DIGITAL DOWN CONVERTER

The software defined radio (SDR) system can change its radio functions by swapping software instead of replacing hardware, seems to be the best solution given that mobile standards are springing up like mushrooms [8]. SDR thereby makes it possible to reprogram cell phones to operate on different radio interface standards. But that's not all. Putting much of a radio's functionality in software opens up other benefits. A mobile SDR device can cope with the unpredictable dynamic characteristics of highly variable wireless links [9]. There are many advanced signal processing tasks performed in a modern digital receiver. Fig.1 illustrates SDR BS receiver that consists of two sections – a front-end high-data rate processing section and a back-end symbol rate or chip-rate processing section. The front-end high-data rate FPGA DSP implements channelization functions for a multi-carrier system. Each channelizer accesses the digital IF (intermediate frequency), translates a channel to baseband and using a multi-stage multi-rate filter adjusts the sample rate to satisfy Nyquist for the selected band. The back-end processor will typically operate on multiple slower rate to perform rake processing, adaptive rake processing, adaptive equalization, adaptive noise cancellation, forward error correction using various techniques like turbo coding, Viterbi coding, BCH coding and RS coding etc. In a QAM system, carrier recovery, timing recovery and adaptive channel equalization is also required [10].

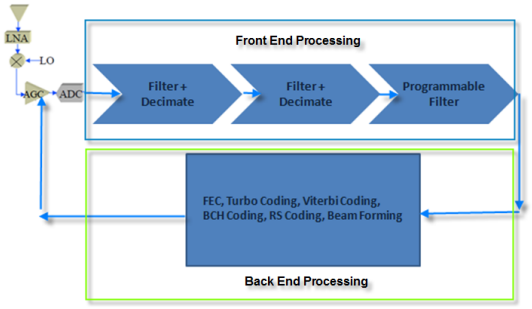

Fig 1: Reconfigurable Base Station Reciever

A variety of communication systems, which carry massive amounts of data between terminals and end users of many kinds, exist today. Necessitated by the global compliant requisition, original equipment manufacturers are expected to provide convergent solutions that accommodate various standards within a single embodiment. Such systems, however, achieve the desired convergence with the least expendable resources: hardware silicon real estate and product turn over time. This necessity represents a major bottleneck in attempting to achieve higher levels of integration and performance in broadband communication systems. For instance commercial wireless chip manufacturers often offer a multi-chip solution to encompass the multi-channel digital up conversion e.g. Texas Instrument GC5316 and digital down conversion e.g. Texas Instrument GC4016 for the digital front-end of the wireless base stations (BSs) [11, 12]. These multi-chip solutions often result in higher integration overhead that translates into higher capital expenses. In contrast, reconfigurable architectures provide flexible and integrated system-on-chip solutions that accommodate smooth migration from archaic to innovative designs, allowing recycling of hardware resources across multiple generations of the standards [13].

Digital up-converters (DUCs) and digital down-converters (DDCs) are important components of every modern wireless base station design. DUCs are typically used in digital transmitters to filter up-sample and modulate signals from baseband to the carrier frequency. DDCs, on the other hand, reside in the digital receivers to demodulate, filter, and down-sample the signal to baseband so that further processing on the received signal can be done at lower sampling frequencies [14]. The first reconfigurable block for a Software Defined Radio implementation is the Digital IF which consists of Digital down convertor (DDC) and Digital up convertor (DUC). They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance [15]. The DDC block is particularly critical from the implementation point of view because of its main goals. Digital down Converter is now an indispensable component in modern radar, sonar, wireless communication and software radio system. DDC shifts the spectrum of interest from its carrier frequency i.e. intermediate frequency to baseband frequency and the data rate is reduced so that the amount of effort required for subsequent processing of signal is greatly reduced without losing any information [16].

The main bottleneck of DDC seems to be located in the multiplier stages that depend on the filter order. The number of multipliers required for implementation depends upon the

filter order. As the filter order increases it increases the required number of multipliers for implementation which in turn increases the processing time and degrades the speed performance. Moreover higher filter order also consume more resources of target FPGA which in turn increases area consumption and cost of the overall system. The drawback of increased number of multipliers can be overcome by multiplier less technique called Cascaded Integrator Comb [17]-[21]. So in this paper multiplier less and multiplier based techniques have been hybridized for optimal utilization of multipliers to develop the proposed GSM DDC design.

3. PROPOSED DDC SIMULATION

A GSM DUC has been designed and simulated by hybridizing the multiplier less and multiplier based techniques. A multi-section CIC decimator has been used multiplier less technique and two equiripple polyphase decimators have used multiplier based technique. The equiripple window based technique is used which results in less number of required coefficients as compared or other window techniques to reduce the computational complexity. The developed DDC is designed to convert the high input sample rates found in a digital radio i.e. 70 MHz, down to lower sample rates i.e. 270 KHz for further and easier processing to model Texas Graychip's GC4016 Multi-Standard Quad DDC Chip [22].

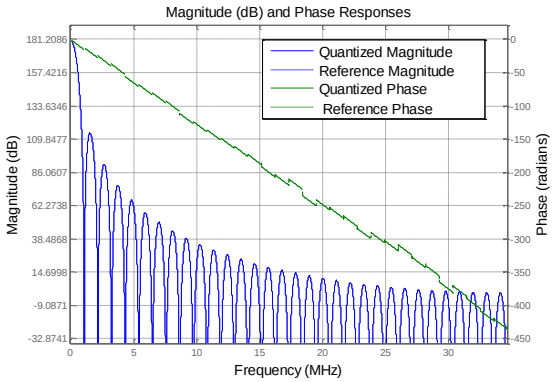

Fig 2: CIC Magnitude Vs Phase Response

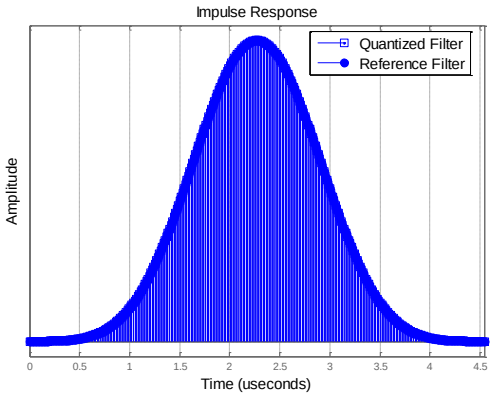

Fig 3: CIC Magnitude Vs Phase Response

The GSM bandwidth of interest is 160 KHz. Therefore, the DDC's three-stage, multirate filter response must be flat over this bandwidth with passband ripple less than 0.1 dB peak to peak in this bandwidth. The filter must also achieve 18 dB of attenuation at 100 KHz. In addition, GSM requires a symbol rate of 270.833 Ksps. Since the Graychip's input sample rate is the same as its clock rate of 69.333 MHz, we must downsample the input down to 270.833 KHz. This requires multistage multirate filtering to provide decimation factor of 256. At first stage, CIC filter is used because it can achieve high sampling rate and can be implemented magnitude vs phase and impulse response have been shown in Fig. 2 & 3 respectively. But CIC filters incur attenuation in the passband region due to their sinc-like response. So CIC filter is followed by a compensating filter. The compensating filter must have an inverse-sinc response in the passband region to lift the droop caused by the CIC. A 4 stage CIC filter $C(z)$ has been used that consists of integrator and differentiator sections.

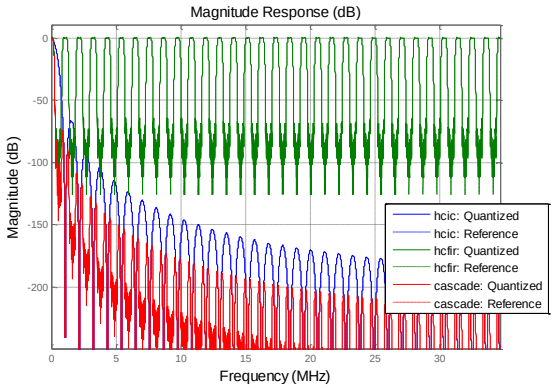

Fig 4: Cascade of CIC & FIR Magnitude Response

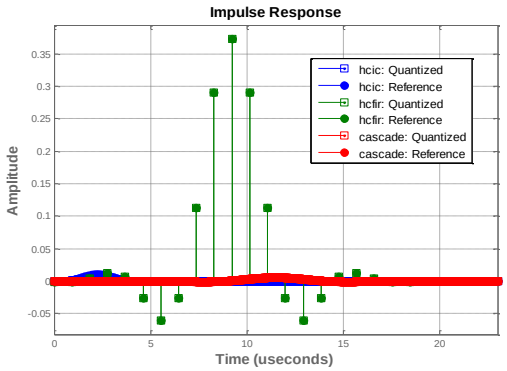

Fig 5: Cascade of CIC & FIR Magnitude Response

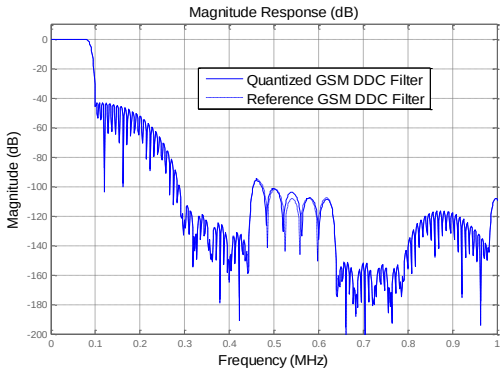

Fig 6: GSM DDC Magnitude Response

The second stage consists of compensation FIR decimator to compensate for the passband droop caused by the CIC. This filter acts as inverse sinc filter. The CIC filter and compensation filter are cascaded together whose magnitude and impulse responses have been shown in Fig 4 & 5

respectively. Third Stage is simple equiripple based low pass FIR Decimator to achieve 18dB attenuation at 100 KHz to meet the GSM requirements. Finally all the three decimators are cascaded to get the GSM DDC response as shown in Fig.6. The magnitude vs phase and impulse response of developed GSM DDC are shown in Fig. 7 & 8.

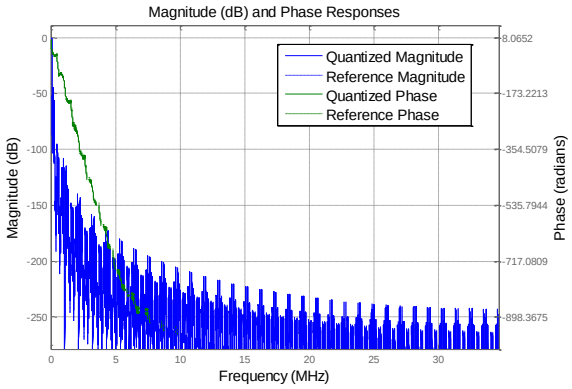

Fig 7: GSM DDC Magnitude Vs Phase Response

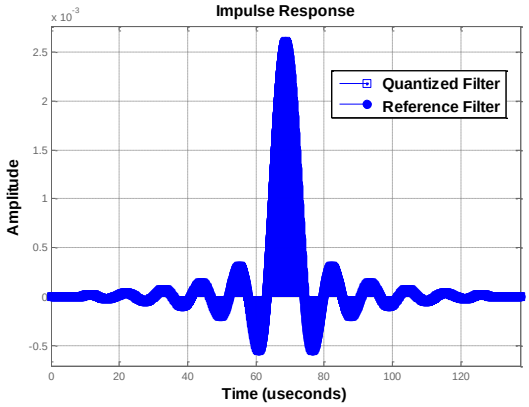

Fig 8: GSM DDC Impulse Response

The developed GSM DUC has been further simulated and verified using Simulink whose output response is shown in Fig. 9. The first two waveforms show I & Q input signals. Third and fourth waveforms show the decimated I & Q output signals.

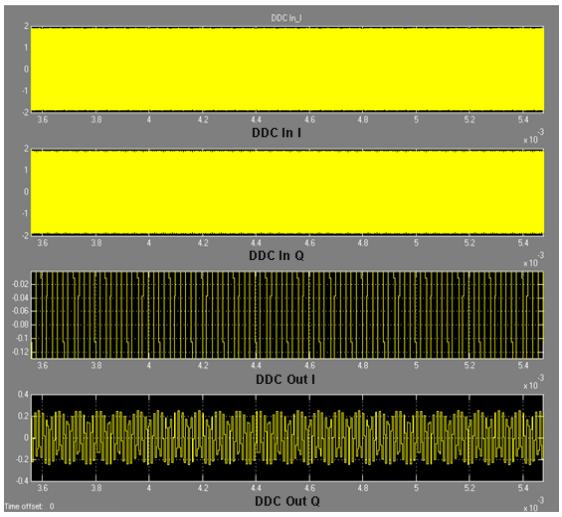

Fig 9: GSM DDC Input & Output Response

4. FPGA IMPLEMENTATION

The CIC filter *C*(z) is multiplier less consisting only of integrator and differentiator sections. A cascade of 4 integrators followed by 4 differentiators, with an embedded 48:1 rate change is used as shown in Fig.10. The CIC filter is followed by a cascade of two 2:1 polyphase decimators shown in Fig.11 & 12 respectively to produce the required input-to-output sample rate change of 192:1. The two FIR decimators have been developed using two multipliers to enhance the cost effectiveness.

In mixer section two embedded multipliers M1 and M2 of Virex II Pro FPGA have been used along with pipelined operation to enhance the sample rate. Each Virtex-II Pro FPGA contains a large number of embedded 18-bit X 18-bit two's-complement embedded multipliers. These embedded multipliers have been used to offer fast, efficient multiplication products. To increase the efficiency the multiplier blocks are sharing routing resources with the Block Select RAM memory. Each embedded multiplier block supports two independent dynamic data input ports: 18-bit signed or 17-bit unsigned.

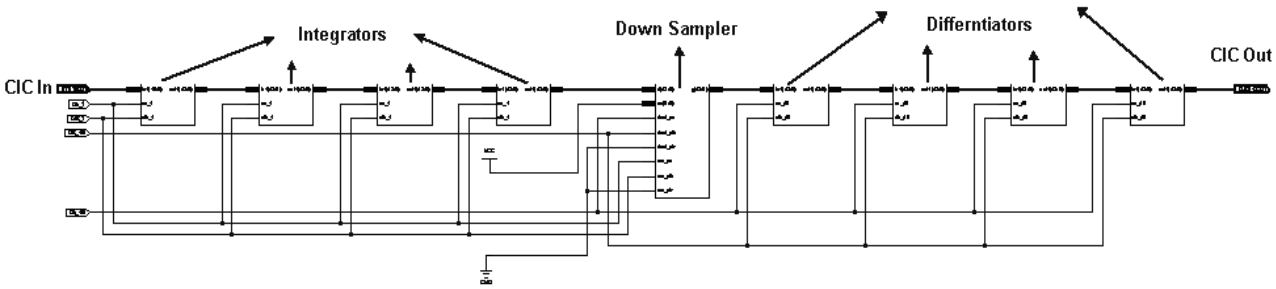

Fig 10: Four Stage Multiplier less CIC Decimator C(z)

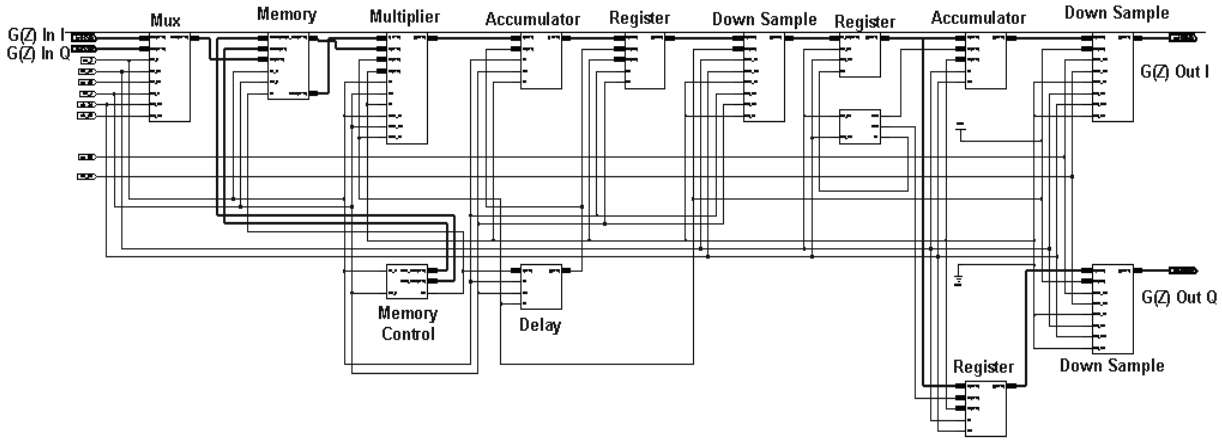

Fig 11: FIR Decimator G(z)

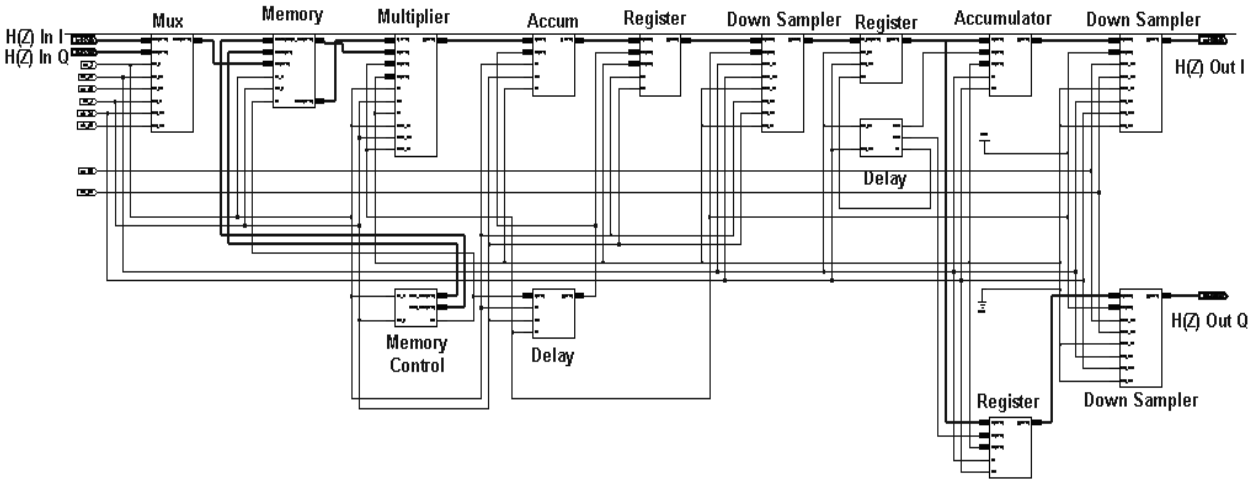

Fig 12: FIR Decimator H(z)

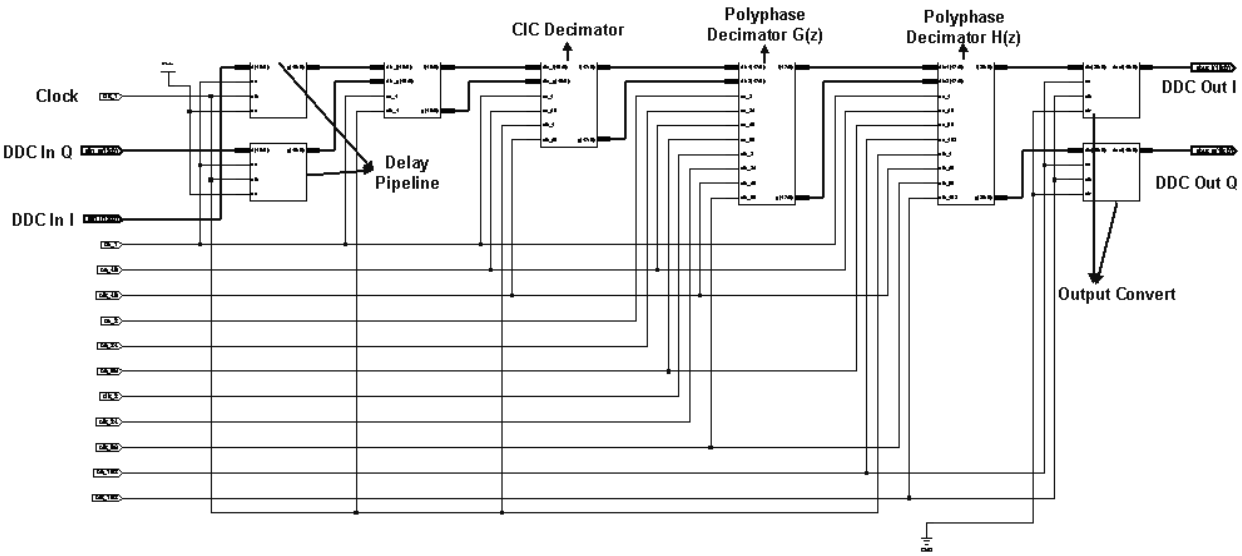

Fig 13: Proposed GSM DDC Design

Finally all the three decimators have been cascaded together to get the final GSM DDC whose schematic has been shown in Fig. 13. The embedded BRAM are also used along with embedded multipliers to enhance the The BRAM memory is a Dual-Port RAM which has been used as fast, discrete, and 18 Kb large blocks of memory. These blocks have been cascaded to enable a deeper and wider memory implementation, with a minimal timing penalty through optimized routing resources. The BRAM dual-port memory consists of an 18 Kb storage area and two completely independent access ports, A and B. The structure is fully symmetrical, and both ports are interchangeable. Data can be written to either port and can be read from the same or the other port. Each port is synchronous, with its own clock, clock enable, and write enable. To maximize utilization of BRAM at each clock edge, the "read during write" option has been used that enhances the flexibility of using the data output bus during a write operation on the same port. It increases the efficiency of BRAM memory at each clock cycle and allows the use of maximum bandwidth.

The developed design has been synthesized on Virtex-II Pro based xc2vp20-7ff896 target device. The resource utilization comparison of proposed GSM DDC design with design of [23] has been shown in Table 1. The optimized GSM DDC can operate at maximum frequency of 159.96 MHz as compared to 125 MHz in case of [11, 12] by consuming 9 embedded BRAMs and 4 multipliers of target FPGA device. The minimum period of developed DDC is 6.251 ns. The DDC design has utilized 17% Slices, 12 Flip Flops, 10 LUTs of xc2vp20 target device as compared to 11% Slices, 8% Flip Flops, 7% LUTs of xc2vp30 device in case DDC design of [23].

Table 1. GSM DDC Resource Utilization Comparison

Logic Utilization	Utilization (%) xc2vp30 [23]	Utilization (%) xc2vp20
Number of Slices	11	17
Number of Flip Flops	8	12
Number of LUTs	7	10
Number of MULT	2	4
Number of BRAMs	6	10

5. CONCLUSION

This paper presents a hybrid technique to design an optimized GSM digital down convertor for software defined radios. The multiplier less technique based CIC decimator has been hybridized with multiplier based equiripple FIR decimators technique to optimize the multiplier requirement in proposed GSM DDC hardware implementation. The Fir decimators are further supported by polyphase composition technique to reduce the computational and hardware complexity. The design has been implemented on lower end less expensive Virtex-II Pro based xc2vp20 target FPGA device. The proposed design has shown a minimum period of 6.251 ns. The developed DDC has shown better resource utilization of slices, flip flops, and LUTs to provide cost effective solution for GSM based SDR applications.

6. ACKNOWLEDGMENTS

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