# Design of Hybrid Adder-Subtractor (HAS) using Reversible Logic Gates in QCA

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## ABSTRACT
Quantum computers for the efficient simulation of physical systems are emerging today. Effect of Spin on Quantum Dots (QDs) paved the way for QCA. Quantum-dot cellular automata (QCA) have a simple cell as the basic element. The cell is used as a building block to construct gates and wires.Reversible logic has extensive applications in quantum Computing. Reversible logic is widely being considered as the potential logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on physical entropy. Reversible gates such as Fredkin and DKG gates can be of great use for the implementation of the logic designs. Recent advances in reversible logic allow for improved quantum computer algorithms and schemes for corresponding computer architectures.In this paper, a design constructing the hybrid adder - Subtractor based on reversible logic gates as logic components using QCA is proposed. By using reversible logic gates instead of using traditional logic gates such as AND, OR, XOR, NOT, a Hybrid reversible Adder - Subtractor whose function is the same as the traditional Adder and Subtractor are designed and compared with the functioning of DKG gate based adder-subtractor. The simulation results shows that higher speed, smaller size and lower power consumption can be achieved with the proposed HAS system.

## GeneralTerm
Design

## Keywords
Adder, DKG gate, QCA, Reversible logic, Spin, Subtractor

## 1. INTRODUCTION
The idea of exploiting the quantum degrees of freedom for a novel way of information processing was envisioned in 1980s by Feynman [1, 2] & Deutsch [3].The idea of "Quantum Computer" for the efficient simulation of finite physical system emerged relatively recently. Various experimental studies [4-7] have shown the effect of Spin on Quantum Bits (qbits) and it's encoding in the form of QCA cells.Quantum-dot cellular automata (QCA) is an emerging field of nanotechnology, with the potential for faster speed, smaller size, and lower power consumption than transistor-based CMOS technology.[8-12]

Although not yet mature in manufacturing or performance characterization to quantitatively assess performance versus CMOS technology, research has been progressing on QCA based logic and architecture design due to projected performance levels [13].

Conventional Combinational logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit if it is constructed using the reversible logic gates will allow the recovery of the information. It has been demonstrated that circuits and system constructed using irreversible logic will result in energy dissipation due to information loss in 1960's [15]. It is proved that the loss of one bit of information dissipates $K_BT\times log_e2$ joules of heat energy, where $K_B$ is Boltzmann's constant and T, the absolute temperature at which computation is performed [15]. Zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates [14]. Reversible logic has applications in quantum computing, low power CMOS, nanotechnology, optical computing, and DNA Computing.

Rolf Landauer proposed in 1961 that a logical computing device with information-bearing degrees of freedom will act as a heat sink for the energy required for computation [15], resulting in computing errors. Therefore, the entropy gain in such a device without a bijection (one-to-one correspondence) between input and output states can be found using Boltzmann's entropy equation [16], where the number of states is represented by, giving an energy dissipation of joules per computing cycle [15]. C.H. Bennett showed that the dissipated energy directly correlated to the number of lost bits, and that computers can be logically reversible, maintain their simplicity and provide accurate calculations at practical speeds [14]. Resultantly, a new paradigm in computer design arose with the goal of reducing the entropy increase, and subsequent energy dissipation.

Reversible logic is useful in mechanical applications of nanotechnology, given that the friction generated by contacting corpuscles within a confined volume can be significantly reduced by eliminating sliding contact using mechanical reversible logic [17]. In addition, reversible logic is also applicable to fields such as quantum computing, since the laws of quantum physics are time reversible [18], and the bijection (one-to-one correspondence) between the input and output states enables probabilistic computations.

In this paper, we describe some basics of reversible logic and design of adder/subtractor using reversible logic gates. The design of a hybrid reversible adder and subtractor is presented which is implemented with the proposed gates and analyzed. A reversible adder/subtractor is proposed that uses Basic reversible gate and majority voter gate which can work as a reversible full adder and a full subtractor and also designed using Reversible DKG gate which can singly work as a full adder and full

subtractor. This design is verified and simulated using QCA Designer tool.

# 2. QCA DESIGN SCHEME

## 2.1 QCA Cell

A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells confining free electrons. Each cell has four quantum dots which can hold a single electron per dot. The four dots are located at the corners of the cell and only two electrons are injected into a cell. By the clocking mechanism, the electrons can tunnel through to neighboring cells during the clock transition by the interaction between electrons. A high potential barrier at the settled clock signal locks the state and results in a local polarization which is determined by Coulombic repulsion. The two electrons reside in opposite corners so that two polarizations are possible as seen in Figure 1. Those two binary states can be used to make QCA cell a storage cell, a computing cell, or a wire.

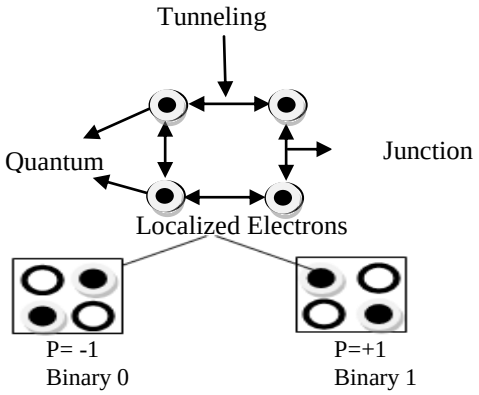


**Fig 1:Basic QCA cell and two possible polarizations**

## 2.2 Signal Flow

A series of QCA cells act like a wire. An illustration of a QCA wire is shown in Figure 2. During each clock cycle, half of the wire is active for signal propagation, while the other half is stable. During the next clock cycle, half of the previous active clock zone is deactivated and the remaining active zone cells trigger the newly activated cells to be polarized. Thus signals propagate from one clock zone to the next.

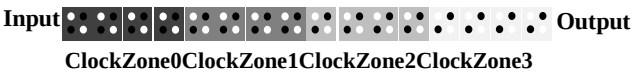


**Fig 2: QCA wire**

## 2.3 Clocking Zones

The circuit area is divided into four sections and they are driven by four phase clock signals. As shown in Figure 3, there is a $90^{o}$ phase shift from one section to the next. In each clock zone, the clock signal has four states: high-to-low, low, low-to-high, and high. The cell begins computing during the high-to-low state and holds the value during the low state. The cell is released when the clock is in the low to- high state and inactive during the high state.The cells in each clock zone behave like a single latch. To be used as a memory cell, a loop of the cells is needed, in which a series of clock zones are used. Because of the signal flow control and synchronization, QCA naturally accepts pipeline designs.

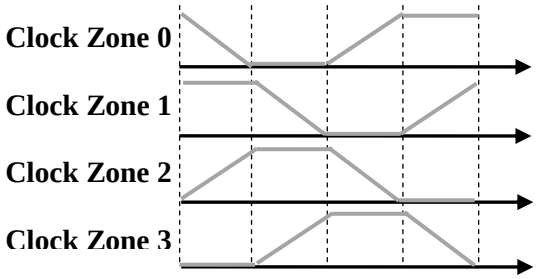


**Fig 3: QCA clock zones**

## 2.4 Logic Gates

Logic gates are required to build arithmetic circuits. In QCA, inverters and three-input majority gates serve as the fundamental gates. The governing equation for the majority gate is

$$M(A;B;C) = A.B + B.C + C.A$$

Figure 4 shows the gate symbols and their layouts. Two input AND & OR gates can be implemented with 3 input majority gates by setting one input to a constant. WithANDs, ORs, and inverters, any logic function can be realized.

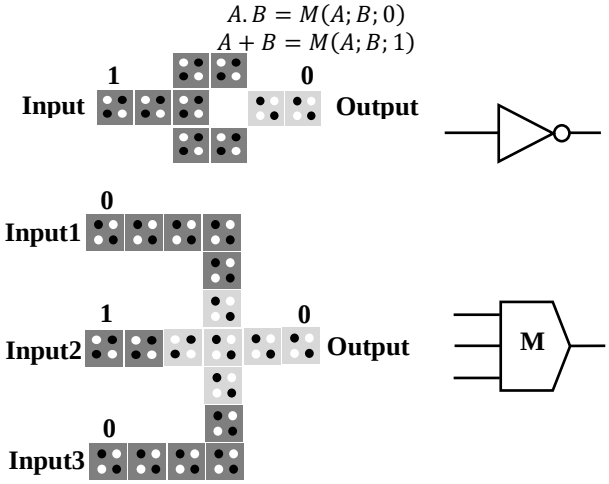


**Fig 4: QCA inverter and majority gate**

## 2.5 Design Rules

The cell is assumed to have a width and height of 18nm and 5nm diameter quantum-dots. The cells are placed on a grid with a cell center-to-center distance of 20nm. Thus the cell size can be defined as 20nm for the nominal design. Because there are propagation delays between cell to cell reactions, there should be a limit on the maximum cell count in a clock zone. This insures proper propagation and reliable signal transmission. If there is no restriction on the maximum length, the design might have fewer clock cycles, but due to the increased propagation delays, the operating frequency would be reduced. Multi-layer crossovers are used for wire crossings in this paper. They use more than one layer of cells like a bridge. An example of a multi-layer wire crossing is shown in Figure 5. The multi-layer crossover design is straightforward although there are questions about how it can be realized in practice, since it requires two overlapping active layers with via connections.

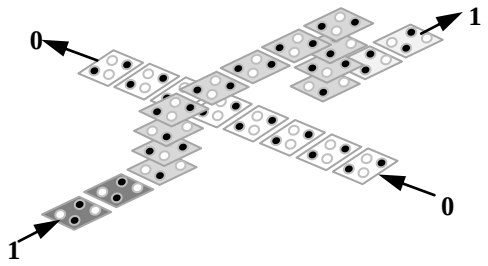


**Fig 5: Layout of multi-layer wire crossing**

## 2.6 Simulation

For circuit layout and functionality checking, a simulation tool for QCA circuits, QCA Designer [28], is used. Thistool allows users to do a custom layout and then verify QCAcircuit functionality by simulations. It includes two different simulation engines such as a bi-stable approximation and a coherence vector.

# 3. PREVIOUS WORK ON ADDER & SUBTRACTOR

## 3.1 Full Adder

The University ofNotre Dame first proposed the design of one-bit full adder. As shown in Fig. 6, it consists of five majority gates and three inverters [29], [30].

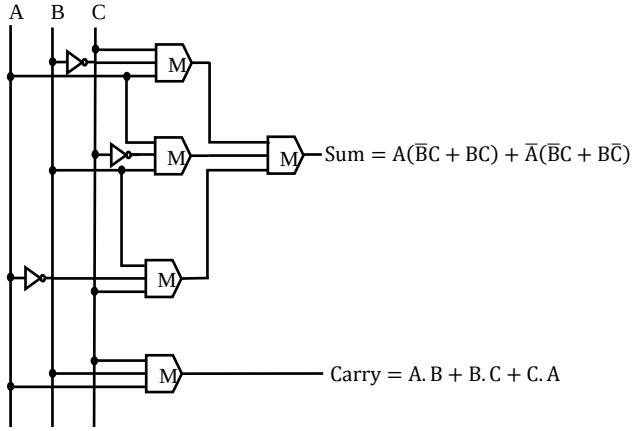


**Fig 6:Schematic of full adder circuit**

By connecting *n* such one-bit QCA full adders, *n*-bit CLA adder can be obtained, since the carry is generated before the sum in the QCA adder.

## 3.2 Full Subtractor

The full subtractor is designed with 3 majority gates and 2 inverters as shown in Fig 7. In the QCA implementation, coplanar crossings are used for interconnections. The QCA implementation requires 192 cells, with an area of208000 nm2 and this also required less number of cells than previous implementations [21].

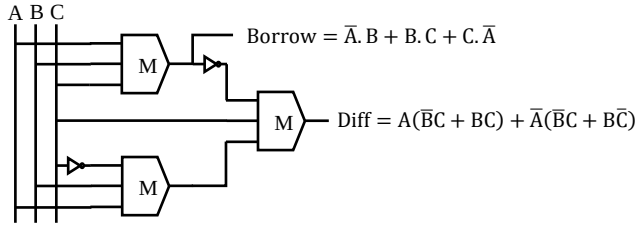


**Fig 7: Schematic of full subtractor circuit**

**Table 1: Truth table of full adder and full Subtractor**

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **Sum** | **Carry** | **Difference** | **Borrow** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 4. DESIGN AND IMPLEMENTATION

Reversible computing cannot be implemented on the existing logic designs which are irreversible in nature. The present day logic gates do not let us un-compute outputs to recover input values, except NOT gate which is the only reversible gate.

Reversible logic gates are circuits that have the same number of inputs and outputs and have one-to-one and onto mappings between inputs and outputs; thus, the input states can be always reconstructed from the output states [21].

## 4.1 Reversible DKG Gate

Reversible DKG gate has 4 inputs and 4 outputs, so it is called Reversible 4*4 DKG gate [19].

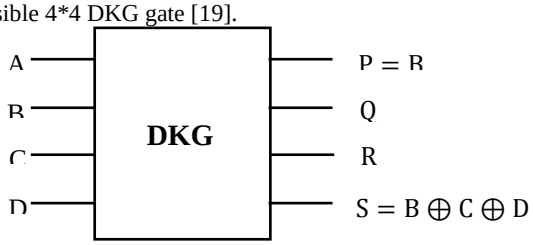


**Fig 8: Reversible DKG gate**

DKG gate with inputs A, B, C, D and outputs are P, Q, R, S. This gate is known as DKG gate. Figure 8 shows the DKG gate with 4*4 inputs and outputs.

**Table2: Truth table for Reversible DKG gate**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **P** | **Q** | **R** | **S** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

## 4.2 DKG Gate Implemented as Full-adder and Full-subtractor

If A=0 then DKG gate work as a Full adder and if A=1 then it will work as a Full subtractor which are shown in Fig. 9(a) & (b) respectively.

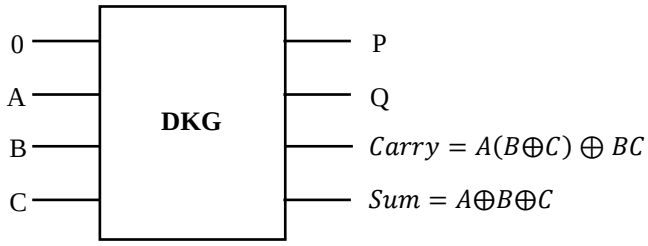


**Fig 9(a): DKG gate as Full adder**

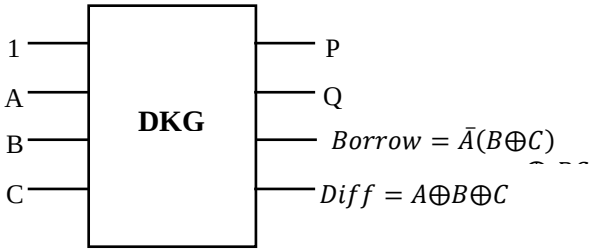


**Fig 9(b): DKG gate as Full Subtractor**

## 4.3 Basic Reversible Gate

Consider the case of a simple two input XOR gate which is irreversible. On repeating one of the inputs to output makes the gate reversible. It can be realized as shown in Figure 10:

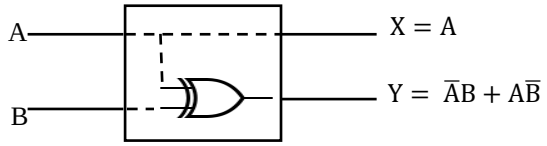


**Fig 10: Basic Reversible Gate**

**Table 3: Truth table for Basic Reversible gate**

| Inputs | | Outputs | |
|---|---|---|---|
| **A** | **B** | **X=A** | **Y=A XOR B** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

## 4.4 Reversible Logic using MajorityVoter Gate

There is another case of reversible logic which has three inputs A, B, C, and using majority voter gate which gives three outputs such as P, Q, R. this circuit gives the reversible output in terms of carry and borrow. It can be realized as shown in Fig. 11:

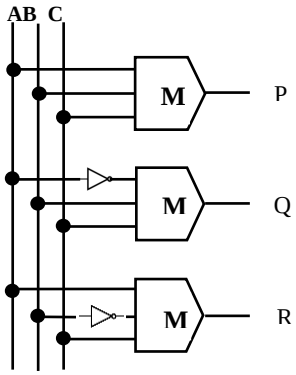


**Fig 11: Reversible logic using majority voter gate**

**Table 4:Truth table of Reversible logic using majority voter gate**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| **A** | **B** | **C** | **P** | **Q** | **R** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

## 4.5 Proposed Hybrid Design of Adder and Substractor using Reversible Logic

Design of adder and Subtractor circuit used basic reversible gate and reversible logic using majority voter gate. This is depicted in figure 12.

**Table 5:Truth table for Hybrid Adder and Subtractor**

| Inputs | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **X** | **Y** | **Z/Sum-Diff.** | **P/ Carry** | **Q/ Borrow** | **R** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

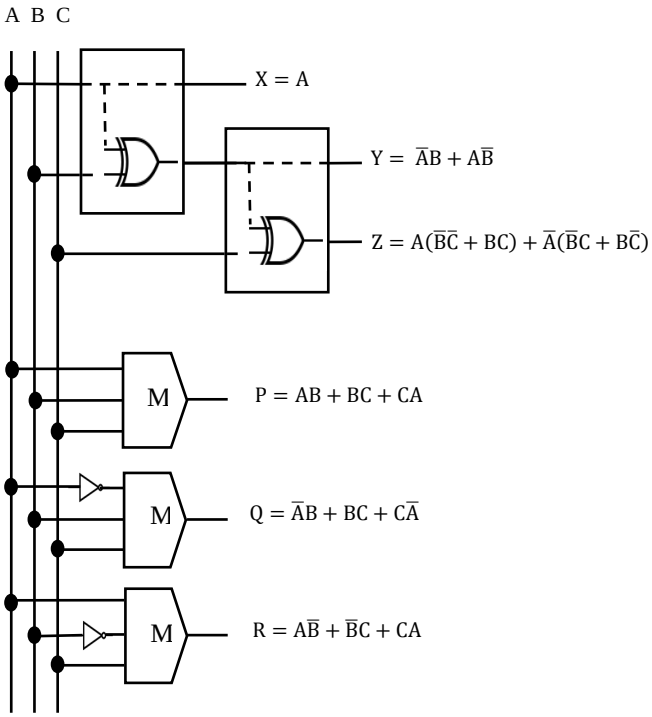


**Fig 12: Adder and Subtractor using Reversible logic**

## 5. IMPLEMENTATION IN QCA

Implementation of adder and Subtractor in QCA is verified using QCA Designer tool. Adder and subtractor designed using reversible DKG gate is shown in figure 13. The proposed designs are shown in Figure 14-16.

### 5.1 Adder and Subtractor using Revercible DKG gate in QCA

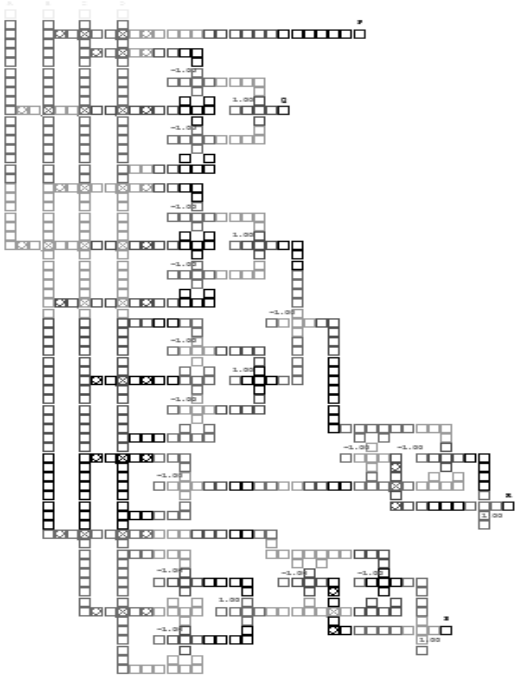

**Fig 13: QCA layout of reversible adder and subtractor using DKG gate**

### 5.2 Hybrid Adder and Subtractor using Reversible Logic in QCA

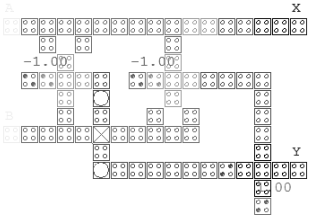


**Fig 14: QCA layout of basic reversible gate**

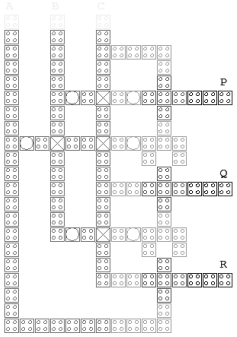


**Fig 15: QCA layout of reversible logic using majority voter gate**

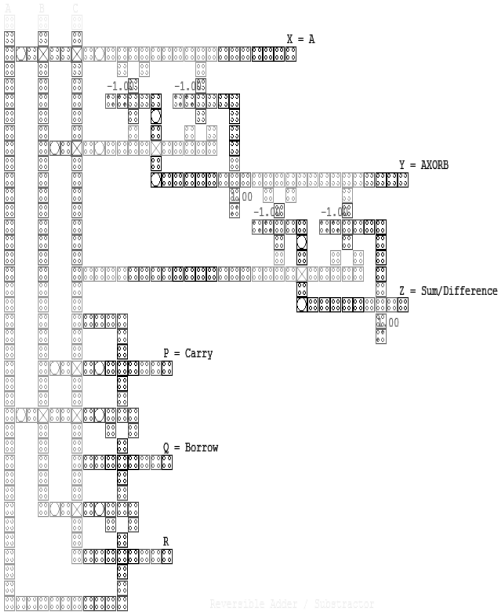


**Fig 16: QCA layout of reversible adder and subtractor**

## 6. SIMULATION RESULT, COMPARISON AND DISCUSSION

All the designs were verified using QCADesigner tool ver. 2.0.3. In the bi-stable approximation, we used the following parameters: cell size=18 nm, number of samples=12800, convergence tolerance=0.001000, radius of effect=65.00 nm, relative permittivity=12.900000, clock high=9.800000e-022, clock low=3.800000e-023, clock amplitude factor=2.000000, layer separation=11.500000, maximum iteration per sample=100. All of these parameters which used are default parameters in QCADesigner tool. In our QCA layouts, we have the goal of workable designs with compact layout. The

simulation results of DKG gate as full adder and full subtractor shown in figure 17, 18 respectively, and simulation results of Basic reversible gate is shown in figure 19, Reversible logic using majority voter shown in figure 20, and finally simulation result of proposed hybrid adder and subtractor is shown in figure 21.

Table6 shows comparison between different adder and Subtractor circuits designed using QCA, in terms of complexity i.e. no. of cells, delay, area, and power consumption. If we see the parameters, we can observe from the given table that the no. of cells are reduces in the proposed design as compared to full adder-subtractor(FAS) and adder – subtractor designed using reversible DKG gate and power consumption is also reduce as compare to FAS and DKG gate, because power consumption is depend on the no. of cells i.e. it's directly proportional to the no. of cells. Delay of proposed HAS is same as compared to FAS.

In the paper [32], it is shown that the average power dissipation per cell is almost the same for different QCA adder designs.

It follows that Power ≡ Complexity.

**Table 6: Comparison between FAS and proposed HAS**

| QCA Circuit | Complexity | Area(in $\mu m^2$) | Delay(in clock) | Power Consumption |
|---|---|---|---|---|
| Full Adder[29],[30] | 190 cells | 0.17 | 1 | 190 |
| Full Subtractor [21] | 192 Cells | 0.20 | 2 | 192 |
| Adder-Subtractor using DKG gate | 752 cells | 1.24 | 4 | 752 (Increase to 96%) |
| Proposed Hybrid Adder Subtractor | 367 cells | 0.54 | 2 | 367 (Reduced to 4%) |

According to the simulation results as we seen that in Figure 17-21 show the outputs waveform from which can we observe that the simulation outputs are same as that can observe from the truth table of adder and subtractor. In the simulation result highlighted blocks show the outputs of proposed hybrid adder and subtractor. The number of clocks before the output is called as delay of the proposed HAS.

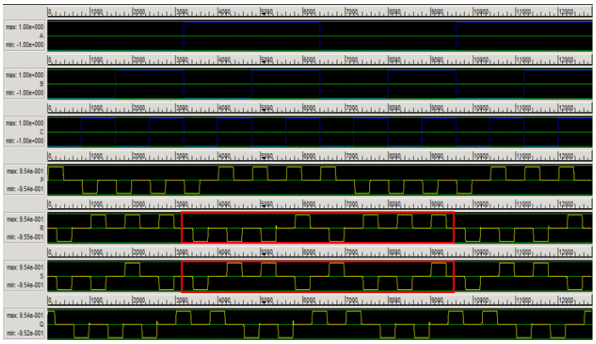

**Fig 17: Simulation result of DKG gate as Full adder**

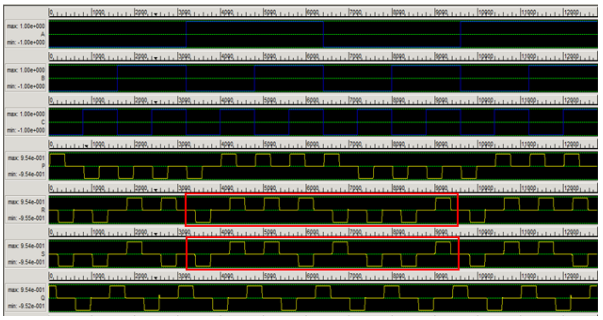

**Fig 18: Simulation result of DKG gate as Full subtractor**

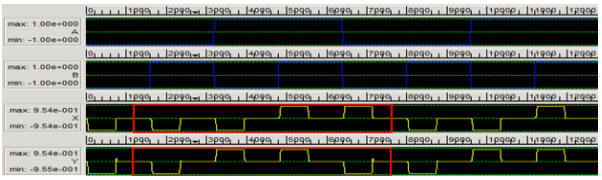

**Fig 19: Simulation result of Basic Reversible Gate**

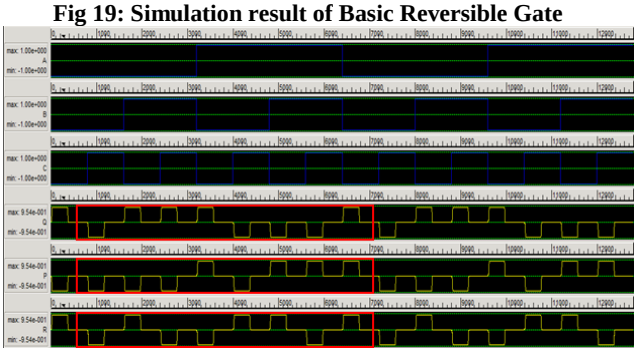

**Fig 20: Simulation result of Reversible logic using Majority Voter gate**

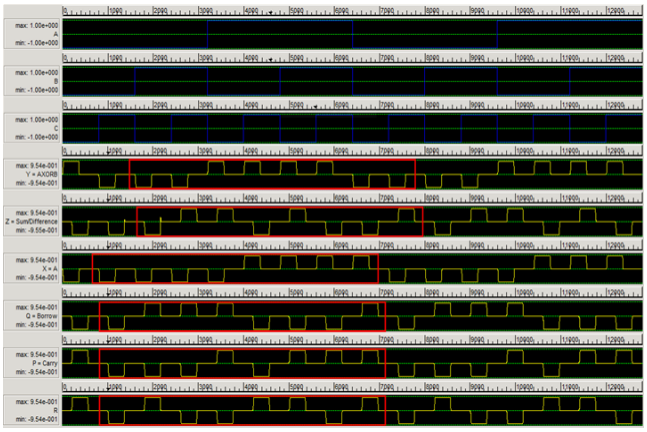

**Fig 21: Simulation result of proposed hybrid adder subtractor (HAS)**

## 7. CONCLUSION AND FUTURE WORK

This paper proposes an adder/subtractor using basic reversible gate and majority voter gate and also designed using reversible DKG gate that works same as a Full adder/subtractor but proposed HAS using reversible logic has greater performance as compared reversible DKG gate. The proposed work shows that in reversible logic, the design of a specific reversible gate for a particular function can be very much beneficial because in proposed design, power consumption is reduced to 4% (ref. table 6). By using reversible logic gates instead of using traditional logic gates such as AND gates and OR gates, the

function of the implemented reversible adder and subtractor is the same with that of the traditional adder and subtractor.

In future, we will design 4-bit adder and subtractor using reversible logic, which reduce the complexity and delay of adder and subtractor. We will also design 4 bit, and 8-bit Arithmetic Logic Unit (ALU) using Reversible logic gates in QCA. By using reversible logic we can improve the speed and performance, and reduce the power consumption, complexity and delay of ALU.

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