A Novel Approach for Reduction in CFO at Channel Estimator in WiMax OFDM System

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ABSTRACT

During Multicarrier transmission in OFDM(Orthogonal Frequency Division Multiplexing), the signal suffers due to fading environment and results in timing and frequency errors at the receiver end.An efficient timing and frequency offset estimation algorithm has been designed in VHDL using ISE XILINX 10.1. The maximum value at which the timing offset is achieved and input signal with a delay are compared to get the frequency offset. This operation ensures that the frequency offset calculation is done at the best time, i.e., when the correlation over the actual received symbol cyclic prefix is complete. The values for frequency offset has been obtained after simulations as .00034232 and timing offset has been observed as1.864ns.The design is achieved at 75.5 Mhz and uses 2% of the total memory of the Virtex-6 Device. The design when implemented was found to reduce 95% of carrier frequency offset(CFO) error, than the performance of a simple frequency estimator.

1. INTRODUCTION

During the past few years, there has been an explosion in wireless technology. This growth has opened a new dimension to future wireless communications whose ultimate goal is to provide universal multimedia communication without regard to mobility or location with high data rates.

Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier transmission technique, many carriers, each one being modulated by a low rate data stream share the transmission bandwidth. Orthogonality is a property that allows multiple information signals to be transmitted perfectly over a common channel and detected without interference. The OFDM is a digital modulation scheme that can support high-speed video communication along with audio with elimination of Intersymbol Interference (ISI) and Interchannel Interference (ICI) [1]. At the same time, it can accommodate more number of users showing the spectral efficiency. Because of high capacity transmission of OFDM ,It has been applied to Digital transmission system,such as Digital audio broadcasting(DAB) system ,Digital video broadcasting TV(DVB-T)system, Asymmetric digital subscriber line(ADSL),Ultra wideband(UWB) system, IEEE 802.11a/g Wireless local area network(WLAN),IEEE 802.16 Worldwide interoperability for microwave access (WiMax)systems and HIPERLAN2(High performance local area network).Its application in mobile communication is more complex especially because of the mobility of the mobile user, thus more exact symbol and frequency offset control must be used to ensure that the subcarrier remain orthogonal.

During the transmission the signal suffers due to the fading environment and hence results in two major problems. One problem is the unknown time instant to start sampling a new OFDM symbol, known as Timing Offset. A second problem is the mismatch of the oscillator frequencies between the transmitter and receiver resulting in frequency offset. The demodulation of a signal with an offset in the carrier frequency can cause large bit errors and may degrade the performance of a symbol synchronizer [2]. Also, Sensitivity to a timing offset is higher in multi-carrier systems than in single-carrier systems .It is therefore important to estimate this offset and minimize its impact. Frequency offset is estimated at the instant the start of the frame is detected, therefore its value is directly related to timing offset. Many algorithms have been designed in past to estimate the values of these offsets, but this approach looks forward to minimize the values of these offsets using VLSI technology.

2. ESTIMATION METHODS

To send the transmitter signal to the receiver with the features to combat the channel problems, some characteristics of the channel must be estimated, maybe in terms of delay between the transmitter and receiver or in terms of the channel impulse response. Channel estimation is basically estimating the channel impulse response at the receiver. Broadly classifying the channel estimation methods, one is the Training sequence based method and the second is the blind method [3].

Channel estimation is essential for removing ISI and noise, and is used in diversity combining, Maximum Likelihood (ML) detection, angle of arrival estimation, etc. Cyclic Prefix/Pilot is basically a reference carrier/tone or reference signal/symbol that is known at the receiver end in terms of position of sequence/pattern and used for the channel estimation because it provides channel state information as it has undergone the most recent channel behavior. It acts as a guard interval in time domain to eliminate the effect of multipath delay spread. A different approach using superimposed pilots has been proposed in [4] where performance of a channel estimator is analyzed for 32 carriers.it has applied the PSK modulation technique. The use of cyclic prefix in the proposed algorithm analyses the channel estimator performance for 256 carriers. The design constraints and data flow are discussed in the next section.

3. DATA FLOW

Work done in past, has been mostly the analysis of the SNR and BER on the channel estimation technique applied that too for pilot schemes.The logic applied for estimation using the cyclic prefix than pilot symbols is better in approach, because Cyclic prefix contains a part of the data in the sent frame, thus converting a linear convolutive channel to a circular convolutive channel ,hence improving the the correlator performance.

Till now schemes have either tracked the start of the frame well or have estimated the frequency error. This novel approach preserves a detail data flow for OFDM based wireless system in such a manner that the frequency offset actually is measured at the instant when acquisition of the start of the frame is done. Also this design structure has been successfully simulated using Virtex 6 Device.

The WiMAX OFDM preamble is defined differently for the uplink and the downlink. The specification also defines variants for doing initial ranging on the downlink. In this case, the time domain signal has a repeated pattern.

The long preamble, used for downlink ranging, consists of a 4x64 pattern symbol, where a 64-sample pattern is repeated 4 times. The uplink uses a short preamble with just a 2x128[5] pattern symbol.The received signal is r(k) =a+bj. This algorithm data flow consists of three parts-

$$ms1= \frac{\rho}{2} \sum_{k=m}^{m+L-1} |r(k+N|^2 + |r(k)|^2 \qquad (1)$$

(N =256)

$$ms2= \frac{\rho}{2} \sum_{k=m}^{m+L-1} r^*(k)r(k+n) \qquad (2)$$

ms1 and ms2 are compared to get the maximum value ie; argmax.

Here even the start of the frame is detected when the cyclic prefix is correlated with the data sequences from which it was extracted.

$$ms3= \frac{\rho}{2} \sum_{k=m}^{m+L-1} r^*(k)r(k+n) \qquad (3)$$

Here (N=64) and ρ is set to 1.

In IEEE802.16-2004 the cyclic prefix can be 64, 32, 16 or 8 samples long[6]. The correlation with delay 64 is used to calculate an angle that is used only when the magnitude of the difference between ms1 and ms2 reaches a maximum (argmax). This operation ensures that the frequency offset calculation is done at the best time, i.e., when the correlation over the actual received symbol cyclic prefix is complete [7].

4. RESULTS & ANALYSIS

4.1 Effect of delay on Timing Offset

The value of Timing offset decreases with the increase in the delay applied in the working of the algorithm at ms2.Effectively there is less computation time observed for the data flow in the algorithm when the delay is less. A comparative analysis has been done for various delays (32,64, 128 &256 bits) and plotted against the observed values of corresponding timing offsets in Fig 1. Here the timing offset value is ideally desired to be very less. But practically timing offset calculated at a delay of 256 bits is observed to be nearly 50% less than the offset value obtained when the delay is 32 bits.

Fig 1. Here the timing offset value is ideally desired to be very less. But practically timing offset calculated at a delay of 256 bits is observed to be nearly 50% less than the offset value obtained when the delay is 32 bits.
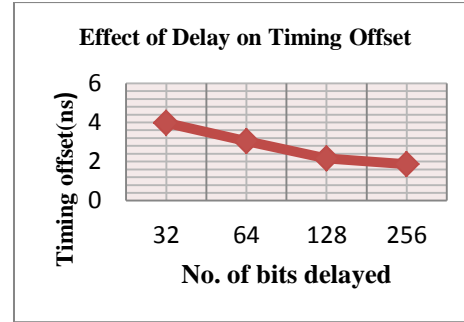

Fig.1 Effect of Delay on Timing Offset

4.2 Effect of delay on Frequency Offset

The value of Frequency offset decreases with the increase in the delay applied in the working of the algorithm at ms2 as shown in fig.2. This approach of reduction of delay has been implemented since the major drawback of cyclic prefix insertion is wastage of bandwidth. Applying reduction in delay not only saves the computation time but also saves the bandwidth.

It is also observed that the frequency offset value estimated with a delay of 256 bits is approx. 60% less than the value observed with a reduced delay of 32 bits. Since our concern lies on the minimization of frequency offset a delay of 256 bits is would be preferred.

4.3 Effect of Length of Cyclic Prefix on MSE(Mean Square Error)&SNR

The length of cyclic prefix can vary from 8, 16, 32 to 64 bits for this algorithm. As shown in the Fig.3, the estimator mean square error as a function of the cyclic prefix length is estimated. The figure shows the estimator performance for 5 dB, 10 dB and 15 dB respectively.
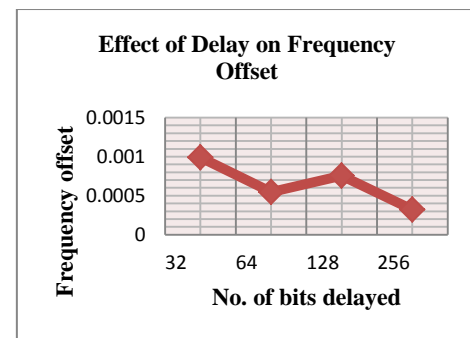

**Fig.2 Effect of Delay on Frequency Offset.**

Note that the threshold value observed in the figure decreases with the SNR. Both the time and frequency estimate exhibit such a performance threshold based on the cyclic prefixes. It is also observed that as the length increases beyond this respective threshold the estimators performance shows continued improvement. With the increase in the length of the cyclic prefix, there is an improvement in the estimator performance to about 46% of the mean square error.

4.4 Reduction in Frequency offset for OFDM modulation in VHDL for different estimators.

Another comparison is done with OFDM Baseband Modulation Technology based on VHDL[8].It implied a simple estimator where the modulation technique was QPSK .The offset estimation done by the designed algorithm is 95% times much better than the simple CP estimator.

Table.1

Parameters	Simple CP estimator	Designed Estimator
Modulation Technique	QPSK	QPSK
Carrier Frequency Offset	.00792	.000342
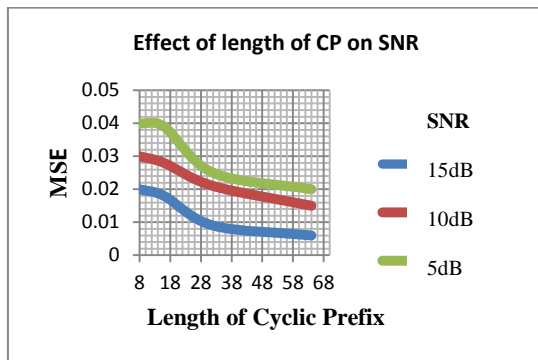
Fig.3 Effect of lengh of CP on SNR.

5. CONCLUSIONS AND FUTURE WORK

An efficient Timing & Frequency offset estimation algorithm has been designed in VHDL.The Estimator has tracked the start of the frame, hence gives the value for Timing offset as 1.864 ns for 256 carriers. The frequency offset have been estimated at the start of the frame and has been estimated to a minimum value of 0.00034232 for 256 carriers.

A Minimization of CFO (Carrier Frequency Offset) Error has been reduced to 95% less as compared to CFO Obtained by simple Cyclic Prefix Estimator. Analysis has been done by varying the delay in the algorithm from 256 bits to 32 bits and it has been inferred that a tradeoff has to be maintained

between the delay applied and the timing and frequency offset values. An increase in operating frequency has been observed with the increase in delay applied in the algorithm It has been concluded that with the increase in the length of the cyclic prefix, there is an improvement in the estimator performance to about 46%.

In the proposed algorithm, Cordic can be implemented while calculating the value for frequency offset which can reduce the size of the algorithm. The proposed algorithm can be tried on backend tool at transistor level and hence more number of bits can be implemented at the input end. Also power reduction can be done by designing the space backend.

6. REFERENCES

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