Low Power Asynchronous UP Counter using CNTFET

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ABSTRACT

In many applications counter is used to divide input clock to produce output, the frequency of the output is the divide by N times of the input clock frequency. Due to these reasons ripple counters can be used as frequency dividers to reduce a high clock frequency down to a more usable value for use in digital clocks and timing applications. In many applications such as ultra low power digital circuits, nano devices, wireless communication etc, designing of low power asynchronous counter is highly desirable. This paper presents the low power asynchronous counter using carbon nanotube field effect transistor, As far as it is known, this is the first attempt to design asynchronous counter using CNTFET. Results of the design are compared with CMOS technology based asynchronous counter.

Keywords: Ripple counter, ultra low power, nano devices, CNTFET, CMOS.

1. INTRODUCTION:

Counter circuits are used in digital systems for many purposes. They may count the number of occurrences of certain events, generate timing intervals for control of various tasks in a system, keep track of time elapsed between specific events, Frequency synthesizers, frequency dividers and so on. Counters of all kinds are used in a variety of digital circuits. The type of counters used includes binary counters, Gray code counters, ring counters, and up-down counters. Most of these counters cycle through a number of states, each state representing a natural number. Because of this cyclic behavior, the next state can be determined from the present state. An up-down counter behaves differently. It counts up or down, depending on the input received. For many counters, the value of the counter, or its count, can be read by the environment. Some- times, however, there is no need to be able to read the value of the counter.

When these counters are designed for very high speed and low power digital circuits in the nano metre ranges, CMOS technology has started to face the many difficult challenges. In CMOS technology the size of the MOSFET is scale down to reduce the size of the device. When the MOSFET scale down to the nanometer ranges, scaling has resulted in increased short-channel effects, reduced gate control, exponentially rising leakage currents, The scaling of MOSFET has progressed rapidly, it may come to an end soon because of the increased short channel effects and power-dissipation constraints. In order to overcome these problems research groups started to explore new devices to replace the CMOS technology. Many new devices has been reported such as single-electron tunneling (SET), rapid single-flux quantum logic, quantum cellular automata (QCA) and carbon nanotube field effect transistor(CNTFET)[1]-[5]. The rest of this paper is organized as follows: Section 2 describes the carbon nanotube field effect transistors. Session 3 describes the HSPICE model of CNTFET. Session 4 narrates the design of 3 bit and 4 bit as3 bit and 4 bit asynchronous up counter using CNTFET based T-Flip Flop. Session 5 provide the simulation results and discussion. Session 6 provides conclusion.

2. CNTFET THEORY

Carbon nanotube field effect transistor (CNTFET) are currently considered, one of the main building block for the replacement of MOSFET based CMOS technology. The core of a CNTFET is carbon nanotube. CNTs are the hollow cylinders. Fig(1) shows the structure of graphene sheet and single walled carbon nanotube (SWCNT). Carbon nanotubes are formed, when a graphene sheet of a certain size that is wrapped in a certain direction, It may be either single walled or multi-walled . Two atoms in the graphene sheet are chosen, one of which servers the role as origin. The sheet is rolled until the two atoms coincide. The vector pointing from the first atom towards the other is called the chiral vector and its length is equal to the circumference of the nanotube. Depending on their chiral vector, carbon nanotubes with a small diameter are either semi-conducting or metallic in nature[6]-[8].

Carbon nanotube field effect transistors (CNTFETs) utilize semi conducting single-wall CNTs to assemble electronic devices. A single-wall carbon nanotube (or SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes

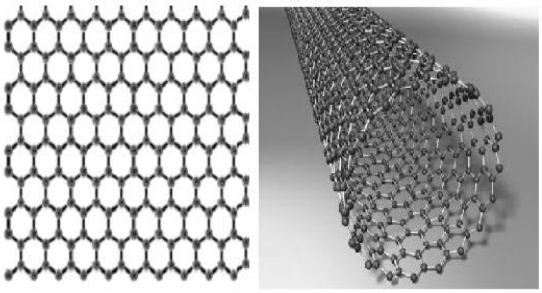

Fig (1) structure of graphene and SWCNT

it very promising alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (*n, m*). The diameter of the CNT can be calculated based on the following equation[9]-[12].

$$D_{CNT} = \frac{\sqrt{3}}{\pi} a_0 \sqrt{n^2 + m^2 + nm} \qquad (1)$$

where a_0 = 0.142 is the inter-atomic distance between each carbon atom and its neighbor. Similar to the MOSFET device, the CNTFET has also four terminals.The current-voltage (I-V) characteristics of the CNTFET are similar to MOSFET's. The

threshold voltage is defined as the voltage required to turn on transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order, as the half band gap is an inverse function of the diameter and the equation for threshold voltage is given below

$$Vth \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \qquad (2)$$

where a = 2.49 Å is the carbon to carbon atom distance, V_π = 3.033 eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. As D_{CNT} of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels, is 0.293V, The device channel consists of a (19,0), zigzag CNT with a band gap of 0.53 eV and a diameter of 1.5 nm. Fig. 2 shows the cross section of a conventional Carbon nanotube field effect transistor (C-CNTFET). The gate dielectric is a 4 nm thick HfO_2 (k = 16) and the device has channel length of 18nm[14]-[16].

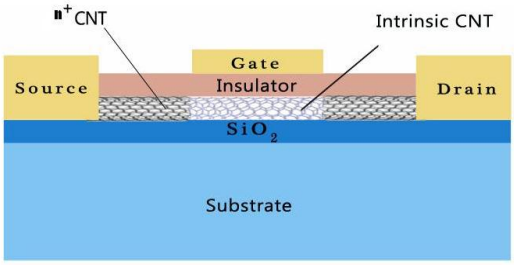

Fig (2) Schematic diagram of a carbon nanotube transistor

3. HSPICE MODEL OF CNTFET:

Fig (2) shows the schematic of MOSFET like CNTFET used for designing the digital circuits. It's HSPICE model is shown in fig (3), model consists of two main parts, current sources and capacitance networks. For semi conducting sub-bands electron current is only considered for the nFET, because the hole current is suppressed by the n-type heavily doped source, drain, and usually is negligible compared to the electron current. The current contributed by the semi conducting sub-bands is given by equation (4)

$$I_D = 2\sum_{k_m}^{M}\sum_{k_l}^{L}\left[J_{m,l}\left(0,\Delta\Phi_B\right) - J_{m,l}\left(V_{ch,DS},\Delta\Phi_B\right)\right] \qquad (3)$$

J m,l ( ) is the current contributed by the substate (m,l). various capacitaces used in model are calculated by equation, (5), (6), (7),(8),(9).[17]-[20].

$$C_{gs} = \frac{L_g C_{ox}[C_{Qs} + (1-\beta)C_c}{C_{tot} + C_{Qs} + C_{Qd}} \qquad (4)$$

$$C_{sg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot} - 2(1-\beta)C_c}{\partial V_G / \partial\Delta\Phi_B}\right) \qquad (5)$$

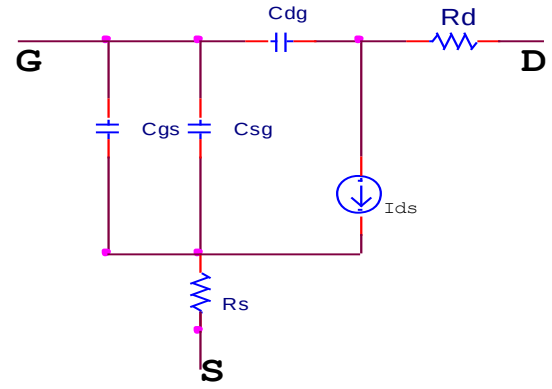

Fig (3) HSPICE model of CNTFET

$$C_{dg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot} - 2\beta C_c}{\partial V_G / \partial\Delta\Phi_B}\right) \qquad (6)$$

$$C_{Qs} = \frac{4e^2}{L_g \cdot kT}\sum_{k_m}^{M}\sum_{k_l}^{L}\left[\frac{e^{\left(E_{m,l}-\Delta\Phi_B\right)/kT}}{\left(1+e^{\left(E_{m,l}-\Delta\Phi_B\right)/kT}\right)^2}\right] \qquad (7)$$

$$C_{Qd} = \frac{4e^2}{L_g \cdot kT}\sum_{k_m}^{M}\sum_{k_l}^{L}\left[\frac{e^{\left(E_{m,l}-\Delta\Phi_B+eV_{ch,DS}\right)/kT}}{\left(1+e^{\left(E_{m,l}-\Delta\Phi_B+eV_{ch,DS}\right)/kT}\right)^2}\right] \qquad (8)$$

Fig (4) shows the drain characteristics of carbon nanotube field effect transistor with the channel length of 18 nm. Drain voltage is varied from 0 to 0.9v for each constant value of Vgs. Current conduction of CNTFET is high due high gate capacitance. In CNTFET higk – k material is used as gate dielectric material (k = 16 for proposed design) which provides the high gate capacitance

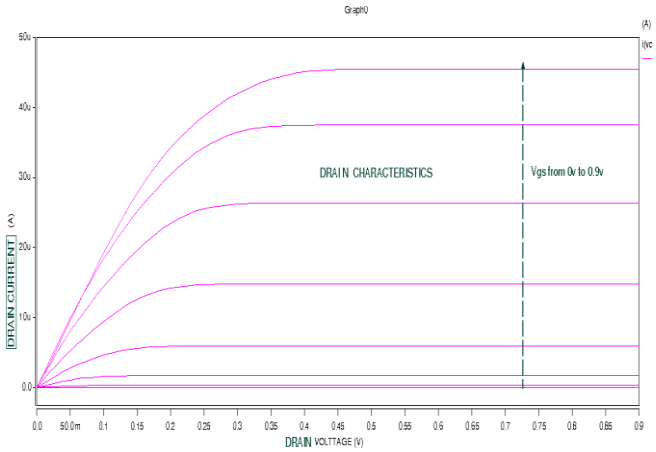

Fig (4) Drain characteristics of CNTFET

4. DESIGN OF ASYNCHRONOUS UP COUNTERS:

A counter can be constructed by a synchronous circuit or by an asynchronous circuit using flip flop. In asynchronous counter the flip-flop within the counter do not

change states at exactly the same time because they do not have a common clock pulse. The main characteristic of an asynchronous counter is each flip-flop derives its own clock from other flip-flops and hence it is independent of the input clock. therefore, the output of each flip-flop may change at different time, hence these counters are called asynchronous. From the asynchronous counter circuit diagram fig (5) It is observed that for the 3 bit counter 3 TFF is used. toggle input of the T FF is always held at logic 1 level. The output of the first flip-flop becomes the clock input for the

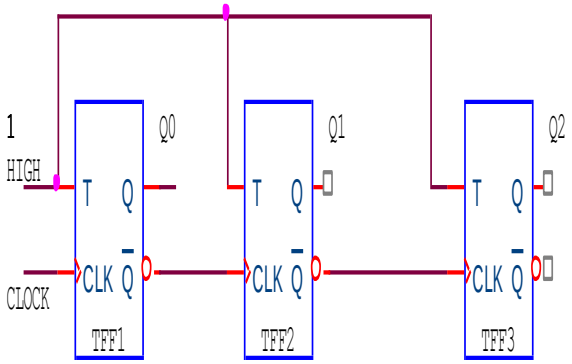

Fig (5) Design of 3 BIT asynchronous up counter using CNTFET

second flip-flop and the output of the second flip-flop becomes the clock input for the third flip-flop. For the first flip-flop, the output changes whenever there is a positive transition in the clock input. This means that the output of the first flip flop produces a series of square waves that is half the frequency of the clock input. Since the output of the first flip-flop becomes the clock of the second flip-flop, the output of the second flip-flop is half the frequency of its clock, i.e. the output of the first flip-flop that in turn is half the frequency of the clock input.

In the proposed design T flip flop is used. For 3 bit asynchronous counter 3 toggle flip flop (T-FF) is employed and for 4 bit counter 4 T-FF is used. With an asynchronous circuit, all the bits in the count do not change at the same time.

A UP counter will count up depending on the input control. Because of limited word length, the count sequence is limited. For an n-bit counter, the range of the count is 0 to 2^{n-1}. The count sequence usually repeats itself. When counting up, the count sequence goes in this manner: 0, 1, 2, … 2^{n-2}, 2^{n-1}, 0, 1, …etc. The counting sequence of 3 bit counter is 0, 1, 2, ….. 7, 0, 1, …. etc. which is shown in table 1.The natural count sequence is to run through all possible combinations of the bit patterns before repeating itself. External logic can be used to arbitrary cause the counter to start at any count and terminate at any count.

Fig (7) shows the 4-bit asynchronous binary counter. It works exactly the same way as a 3 bit asynchronous binary counter. Except it has 16 states due to the fourth flip-flop. Asynchronous counters are commonly referred to as ripple counters dur to effect of the input clock pulse is first "felt" by T-FF1. This effect cannot get to T-FF2 immediately because of the propagation delay through T-FF1. Then there is the propagation delay through FF2 before FF3 can be triggered and so on. Thus, the effect of an input clock pulse "ripples" through the counter, taking some time, due to propagation delays, to reach the last flip-flop

Table.1. 3 bit asynchronous up counter binary state Sequence

Clock Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

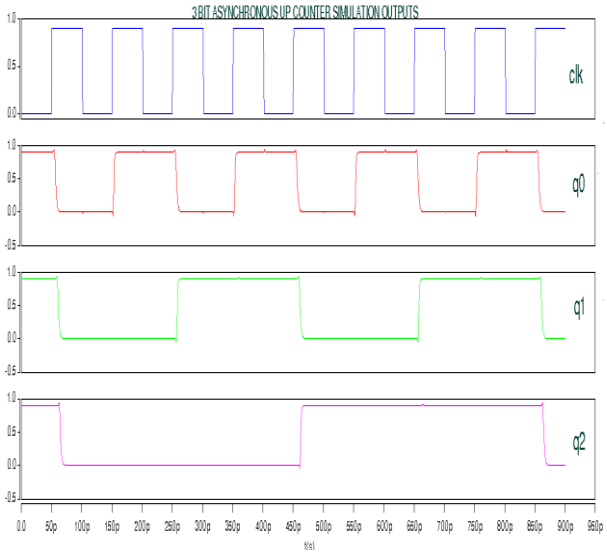

Fig (6) simulation results of 3 BIT asynchronous up counter using CNTFET

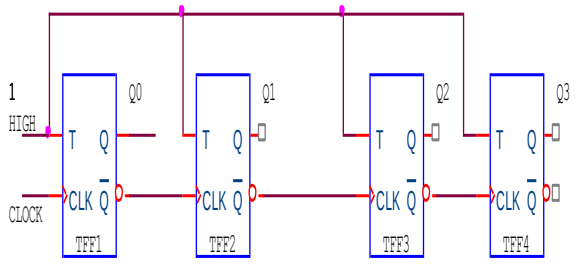

Fig (7) Design of 4 BIT asynchronous up counter using CNTFET

Table.2. 4 bit asynchronous up counter binary state sequence

Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

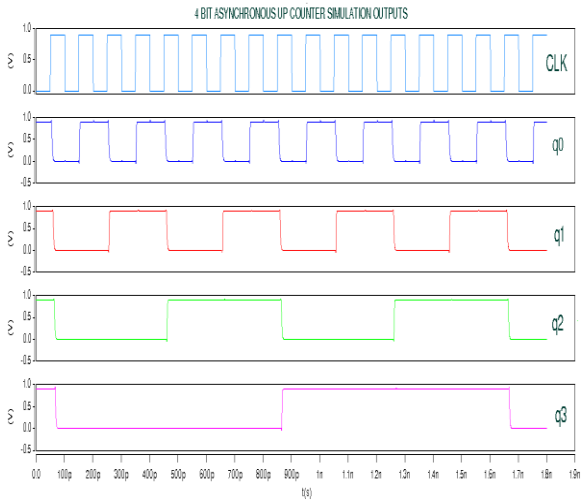

Fig (8) simulation results of 4 BIT asynchronous up counter using CNTFET

5. SIMULATION RESULTS AND DISCUSSION:

In the proposed design of 3 bit and 4 bit asynchronous counter CNTFET is used. Fig 6 shows the Simulation results of the 3 bit counter. the propagation delay t_{PLH} of 3 bit CNTFET based counter is 40.1ps where as for CMOS based design 8.13ns. similarly propagation delay of t_{PHL} for CNTFET based design is 10.2ps and for CMOS based design56ps. This less propagation delay of CNTFET based design gives total delay of the 3 bit counter is 14.9ps where as in CMOS 4.1ns. Power consumption of the 3 bit CNTFET counter is 130.5 µW and for CMOS counter is 194.1µW. simulated parameters of 3 bit counter is shown in table 3. The CNTFET based 4 bit counter consumes 142.7 µW where as CMOS based design consumes 198.3 µW. delay of the counter is 12.6ps and power delay product is 28.1aJ. Simulated parameter of 4 bit counter is shown in table 4 and waveform in fig (8). from Simulated results of CNTFET based counter provides high speed of counting with low power consumption and low operating voltage. The proposed counters can be used for modern frequency synthsizer, phased locked loop, etc., Drain characteristics of the CNTFET is also simulated using HSPICE with the channel length of 18nm and with the high k dielectric material Hfo_2 (k = 16).

Table.3.Simulated parameters of 3 bit counter

PARAMETERS	3 Bit Counter	
	CMOS	CNTFET
Channel length (nm)	180	18
Supply Voltage	1v	0.9v
t_{PLH}	8.13ns	40.1ps
t_{PHL}	56ps	10.2ps
Power (µw/µm)	194.4	130.5
Delay(s)	4.1ns	14.9ps
Power Delay Product (Joules)	9.24-14	30.2aJ

Table.4.Simulated parameters of 4 bit counter

PARAMETERS	4 Bit Counter	
	CMOS	CNTFET
Channel length (nm)	180	18
Supply Voltage	1v	0.9V
t_{PLH}	15.9ns	37PS
t_{PHL}	24.2ns	12PS
Power (µw/µm)	198.3	142.7
Delay(s)	20.1n	12.6ps
Power Delay Product (Joules)	0.47pJ	28.1aJ

6. CONCLUSION:

This paper describes the design of 3 bit and 4 bit asynchronous up counter using carbon nanotube field effect transistor. Simulation is done for both CMOS and CNTFET based technology. CMOS based design is simulated in 180nm technological node and CNTFET based design is simulated in 18nm technological node. . CNTFET has been proposed in

this paper to achieve high-speed operation with low power .As the threshold voltage of the CNTFET can be easily controlled by changing the chirality vector of the CNTs, digital circuit can be designed for the required threshold voltage. Since CNTFET gives the high on state current CMOS will be replaced by CNTFET for future nano devices

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