Analysis of Subthreshold Leakage Current in IP3 SRAM Bit-Cell under Temperature Variations in Deep-Submicrometer CMOS Technology

Neeraj Kr. Shukla
ITM University
Gurgaon (Haryana) India

Shilpi Birla
SPS University
Udaipur (Rajasthan) India

Saksham Dembla
ITM University
Gurgaon (Haryana) India

ABSTRACT
In this paper, we present the analysis of subthreshold leakage current with temperature variations in an IP3 SRAM bit-cell. A comparison of subthreshold leakage current of IP3 SRAM bit-cell with conventional 6T, P4 and P3 is performed at elevated temperatures ranging from 0^0C to 125^0C. It is observed that subthreshold leakage increases with temperature and also IP3 SRAM bit-cell has the lowest subthreshold leakage variations when compared with conventional 6T , P4 and P3 SRAM bit-cell structures.

Keywords
SRAM, Deep-Submicrometer, Standby Leakage, Subthreshold Leakage, Temperature Effect.

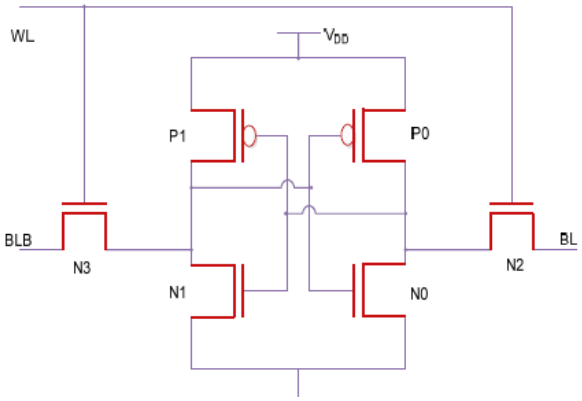
1. INTRODUCTION
At DSM (deep sub-micron) level CMOS technology there is an increasing need for power efficient portable devices as well as high power processors. As there is an increasing demand for multimedia rich applications in handheld and mobile devices, there is a need for technological advancements which endorse power efficiency and performance as well as optimizing constraints such as stability and area requirements. SRAM is an integral component in modern Digital System-on-Chip (SoCs). As SRAMs have a strong impact on overall power, performance, stability, are requirements, these constraints can be managed and optimized by specifically designing SRAMs for target applications such as portable multimedia devices, implantable bio-medical devices, wireless sensor networks etc[8].

In SRAMs, dynamic power dissipation takes place due to switching activity and static power dissipation takes place due to leakage currents. This is the reason why leakage currents are gaining more and more importance. Moreover with scaling down of CMOS transistors gate leakage and sub-threshold leakage currents increase manifold times. It is predicted that gate leakage current will increase 500 times per technology generation and sub-threshold current will increases 5 times per technology generation [1]. As sub-threshold current consists of the major part of leakage current, it is of utmost importance. Also it is expected to increase with the rise in temperature. It is to be noted that temperature dependence of leakage currents is very important in very large scale integration (VLSI) circuits as they operate at elevated temperatures because of power dissipation.

Conventional Six Transistor (6T) SRAM bit cells are most prevalent in nearly all VLSI systems due to its superior design and full compatibility with logic process technology. As scaling down continues, present SRAM designs are facing serious challenges it is important to maintain sufficient cell stability margin, optimizing area requirements along with leakage power issues.

In this paper, after basic introduction in section 1, the operation of conventional 6T SRAM bit-cell is given under section 2 followed by basic leakage mechanisms in section 3. Section 4 presents the analysis of subthreshold leakage currents of 6T, P4, P3 and IP3 SRAM bit-cells at varying temperature is given followed by a comparison of the same at 125^0C.

2. Conventional 6T SRAM Cell
As shown in figure.1, an SRAM cell six MOS transistors. It does not need to be refreshed unlike DRAM as the bit is latched in it. It has large noise immunity and operates at lower supply voltages. Although it occupies more space than a DRAM cell which is made up of one transistor and a single capacitor and hence is less complex.



A 6T SRAM cell consists of two CMOS inverters connected back to back (P0, N0 and P1,N1). There are two access transistors N3 and N2 which are controlled by wordline (WL), fig.1. As long as the power is available to the cell, it maintains one of its states i.e '0' or '1'. In deep Sub- Micron level, ideal mode of the memory is becoming the main concern due to its concerns in leakage power and data retention in lower voltages.

2.1 SRAM Bit-Cell Operation
The nMOS and pMOS transistors form a bistable latch. The main states of an SRAM bit cell are as follows:

2.1.1 Data Write Operation
The value to be written is applied to the Bit lines. Thus to write data "0", we assert BL="0", BLB = "1" and to write data "1", the BL = "1", BLB = "0" is asserted when WL="1".

2.1.2 Data Read Operation

Read cycle starts with pre-charging BL and BLB to "1", i.e., VDD. Within the memory cell P0 and N1 are ON. Asserting the word line, turns ON the N2 and N3 and the values of Q and QB are transferred to Bit-Lines (BL and BLB). P0 and N2 pull BL upto VDD, i.e., BL = "1" and BLB discharges through N3 and N1. This voltage difference is sensed and amplified to logic levels by sense amplifiers.

2.1.3 Standby Operation (Hold)

When WL = "0", N2 and N3 disconnect the cell from Bit-Lines (BL and BLB). The two cross-coupled inverters formed by P0-N0 and P1-N1 will continue to reinforce each other as long as they are disconnected from the outside world. The current drawn in this state from the power supply is termed as standby current.

3. Leakage Current Mechanisms

The major reason for power dissipation in CMOS circuits at DSM regime is leakage current. There are various mechanisms that are responsible for leakage current and hence, power dissipation.

In a Deep Sub-Micron (DSM) MOS transistor, majorly, there are six leakage current components. These leakage current components are enlisted below:

1. Sub-threshold Leakage Current,
2. Gate Oxide Tunneling Leakage Current,
3. Reverse-Bias p-n Junction Leakage Current,
4. Gate Leakage Current (due to hot-carrier injection),
5. Gate Induced Drain Leakage (GIDL) and
6. Channel Punch-through Leakage Current.

Here, the sub-threshold leakage current, GIDL current and punch-through leakage current are dominant sources of leakage in the OFF state transistors whereas the reverse-bias p-n junction leakage and gate oxide tunneling current occur in both ON and OFF state transistors. However, gate current due to hot-carrier injection typically occurs during the transistor bias states in transition. Various leakage components in a MOS transistor are shown in Figure 2.

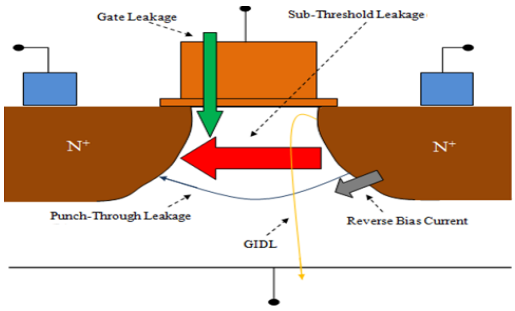


Figure 2. Various leakage components in a MOS transistor

However, in this paper, we will focus on sub-threshold leakage current mechanism.

3.1 Sub-Threshold Leakage Current

Sub-threshold leakage current, also known as weak inversion current flows through the reverse drain terminal when device is in OFF or non-conducting state (i.e $V_g < V_{th}$)[2]. Minority charge concentration in weak inversion mode is considered zero, ideally, but has a finite value practically. the variation of minority charge concentration along the channel in an n-channel MOSFET is illustrated in fugure 3.

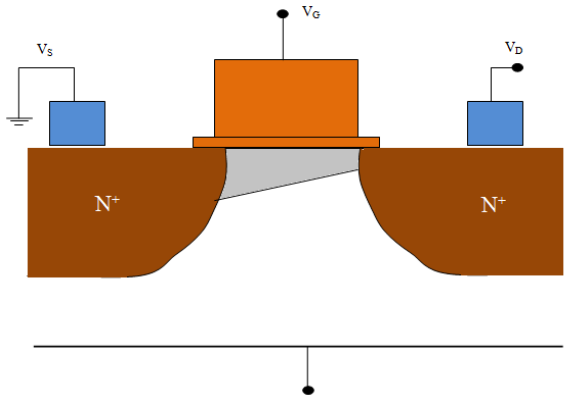


Figure 3. Variation of minority carrier concentration in n-MOS (weak inversion region)

Diffusion current is the major contributing component in sub-threshold leakege current .

3.1.1 Factors affecting sub-threshold leakage current

a) Drain Induced Barrier Lowering (DIBL).

In long channel devices, threshold voltage (V_{th}) is virtually independent of the channel length and drain bias. Whereas, in short channel devices V_{th} and sub-threshold current (I_{DS}) vary with drain bias. This is called DIBL.

b). Body Effect:

Reverse biasing well-to-source junction of a MOSFET transistor leads to widening of bulk depletion region and this increases the threshold voltage[4].

c). Narrow Width Effect:

The threshold voltage changes with the change in the gate width and therefore modulates the sub-threshold leakage.

d). Effect of channel length and roll-off:

The threshold voltage of MOSFET decreases with the decrease in channel length. This reduction of V_{th} with reduction of channel length is known as V_{th} roll-off.

e). Effect of temperature:

The study of temperature dependence of the sub-threshold leakage current is crucial in digital very large scale integration (VLSI) circuits as they usually operate at elevated temperatures having large power dissipation in form of heat generation. Log (I_D) Versus V_G shows a linear change in sub-threshold slope S_t with temperature as shown in figure 4 which is also predicted by the sub-threshold current model [2]. In the DSM technology, the major component of the standby current (I_{OFF}) is the sub-threshold leakage; therefore, the temperature dependence of I_{OFF} represents the temperature dependence of the sub-threshold leakage.

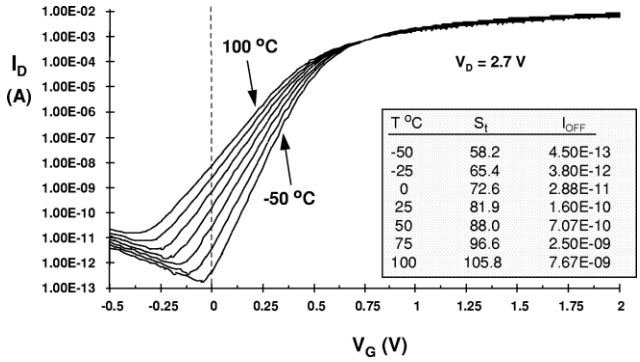


Figure 4 I_D versus V_G showing temperature sensitivity of I_{OFF}[7]

There are two parameters that increase the sub-threshold leakage as temperature is raised. Firstly, sub-threshold slope (S_t) increases linearly with temperature and secondly, the threshold voltage decreases, hence contributing to more leakage current.

4. IP3 SRAM Cell- Simulation And Results

Analysis of leakage current under temperature variations of a novel P3(IP3) SRAM cell is presented in this paper which uses less power than the conventional 6T SRAM cell. In this SRAM bit-cell structure, an integrated approach of two separate sub-cells (read and write) structure is proposed with a pMOS gated ground and drowsy scheme to reduce the active and standby power without losing cell's performance [8]

The sub-threshold leakage current and standby leakage power in IP3 SRAM bit-cell have been analyzed under temperature variations. In the standby mode, the simulations have been performed at VDD=0.7V and 0.8V for 6T, P4, and P3 SRAM cells whereas the for IP3 SRAM cell it is 0.35V.

4.1 Standby leakage power

As mentioned earlier, standby leakage power is significantly reduced in this particular bit-cell structure as drowsy voltage scheme is used i.e a drowsy voltage (V_{DD}= 0.35V) is applied to the memory to retain the data in upper memory sub-cell [8]. The comparison between standby leakage power of various cell structures i.e. 6T SRAM cell, P4 SRAM cell and IP3 SRAM cell is mentioned below.

4.2 Comparison of various SRAM cells at room temperature.

When compared with conventional 6T, P4 AND P3 SRAM bit cell structures, it is observed that the standby leakage power of IP3 SRAM cell is 56.88% at 0.8V and 44.35% at 0.7V less than that of 6T SRAM cell. Whereas, P4 SRAM consumes 70.90% at 0.8V and 86.67% at 0.7V less overall power as compared to IP3 SRAM cell and also P3 SRAM cell consumes 29.81% at 0.8V and 52.401% at 0.7V less overall power than IP3 SRAM cell at room temperature i.e. 25°C. This is illustrated in figure 5. It is to be noted that the operation voltage of IP3 SRAM bit cell is drowsy voltage, i.e, 0.35V[9].

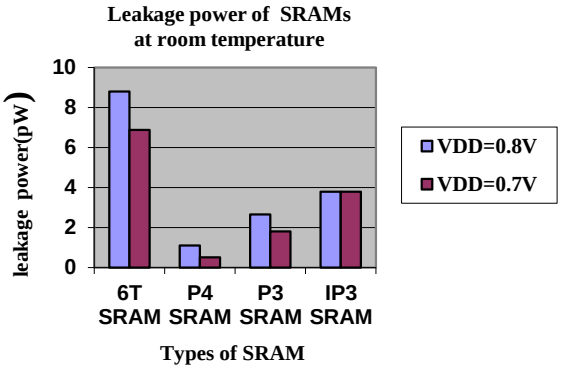


figure 5. leakage power of SRAMs at room temperature.

Figures 6, 7, 8 and 9 show the standby power variation with an increase in temperature starting from 0°C to 125°C of various SRAM bit- cells. It can be observed that the standby leakage current increases almost exponentially when there is an increase in temperature. It is observed that at 125°C, the standby leakage power of IP3 SRAM cell is approximately 77%, 25% and 40% less than that of 6T, P4, P3 bit cells respectively. The standby leakage powers at various temperatures of the earlier mentioned bit cells are illustrated in figure 10, which clearly shows that the standby leakage power of the IP3 SRAM cell is the lowest.

A. 6T SRAM cell.

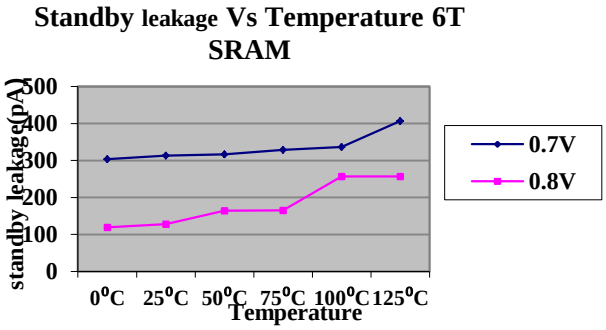


Figure 6. 6T SRAM cell standby leakage Vs temperature

B. P4 SRAM cell

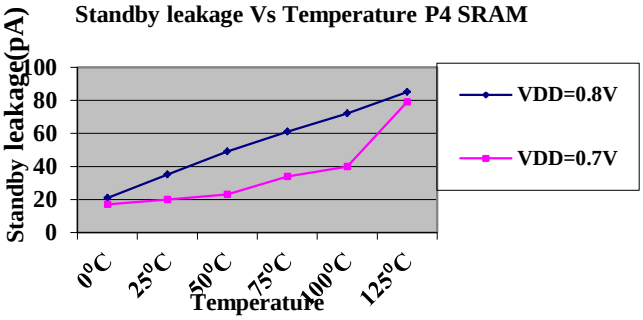


Figure 7. P4 SRAM cell standby leakage Vs temperature

C. P3 SRAM cell

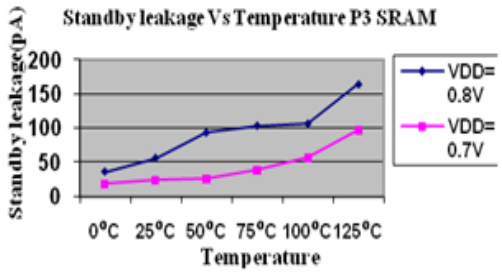


Figure 8. P3 SRAM cell standby leakage Vs temperature

D. IP3 SRAM cell

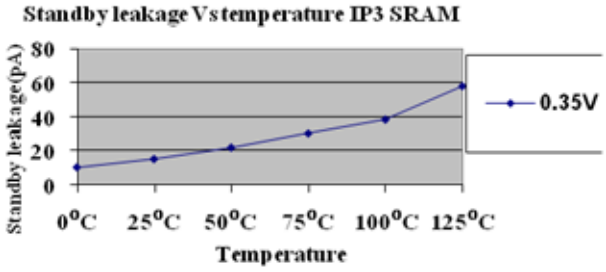


Figure 9. IP3 SRAM cell standby leakage Vs temperature

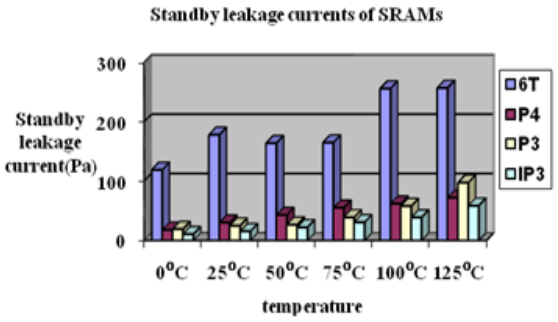


Figure 10. Standby leakage current of SRAMs at various temperatures.

5. CONCLUSION

In the proposed IP3 cell, at a time(read/write), only one half of the cell is working, this reduces power consumption significantly during data write and read operations[8]. During standby mode, an appreciable power reduction is observed. The IP3 cell has 17.65% improved power as compared to 6T cell while performing the data write operation and 94% and 93% improved power consumption as compared to P4 and P3 cells while performing the data read operation [8]. Hence, it can be said that the active power at data read and write operation is the least in IP3 cell[8]. Moreover, the voltage noise margin in IP3 SRAM cell is improved as compared to 6T, P4 and P3 cells[8]. The IP3 cell is hence, the best low power SRAM bit cell amongst all the four cells mentioned. This makes it highly suitable for portable devices as less power consumption means more duration on battery power which is desired in all the portable devices.

REFERENCES

[1] Li-Jun Zhang, Chen Wu,Ya-Qi Ma, Jain-Bin Zheng, Ling-Feng Mao, "Leakage Power Reduction Techniques of 55nm SRAM cells", IETE Technical Review, Vol. 28, Issue 2, pp. 135-145, Mar-Apr 2011.

[2] Fundamentals of Modern VLSI Devices. New York: Cambridge Univ. Press, Ch. 3, pp. 120–128, 1998.

[3] J. M. Rabaey, Digital Integrated Circuits. Englewood Cliffs, NJ: Prentice-Hall, Ch. 2, pp. 55–56, 1996

[4] R. Pierret, Semiconductor Device Fundamentals. Reading, MA: Addison-Wesley, Ch. 18, pp. 680–681, 1996.

[5] D. Fotty, MOSFET Modeling with SPICE. Englewood Cliffs, NJ: Prentice-Hall, Ch. 6, pp. 113–115, 1997.

[6] BSIM Group. MOSFET Model. University, California, Berkeley. Online available at: http://www-device.eecs.berkeley.edu/~bsim3/

[7] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE J. Solid-State Circuits, Vol. SC-9, pp. 256, 1974

[8] R.K Singh, Manisha Pattanaik and Neeraj Kr. Shukla, " Characterization Of a Novel Low Power SRAM Bit-cell Structure at Deep sub-micron CMOS Technology for Multimedia Applications." *Circuits and Systems, Scientific Research, USA*, Vol.3 No.1, pp. 23-28, jan.2012

[9] Neeraj Kr. Shukla, R.K.Singh, and Manisha Pattanaik "Analysis of Gate Leakage Current in IP3 SRAM Bit-Cell under Temperature Variations in DSM Technology" IJET 2012 Vol.4(1): 67-71 ISSN: 1793-8244.