A CMOS Band Gap Reference Generator for Low Voltage Amplification with the Application of a (-ve) Feedback Loop

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ABSTRACT

We all know that the basic building block of any communication system is the reference voltage generator. The objective of reference generation is to establish a DC voltage or current that is independent of the supply and process and has a well-defined behavior with temperature. Band Gap Reference (BGR) is one of the most popular reference generators. In the conventional BGR circuit, the reference voltage V_{ref} is the summation of thermal voltage V_T and the base to emitter voltage of a transistor (V_f).The thermal voltage V_T has a (+Ve) temperature coefficient (TC), whereas V_f has a (-Ve) temperature coefficient (TC).So BGR is independent of temperature .The traditional BGR circuit generates a reference voltage about 1.12V.So this circuit limits a low supply-voltage operation below 1v. In this paper a new BGR circuit in 0.25μm iCMOS technology, and a new BGR in BiCMOS technology is proposed which are containing a extra (-ve) feedback loop to get very low reference voltage as well as to stabilize this reference voltage even when it is operating below 1v supply. The TC of this reference generator is getting even zero by applying a (-ve) feedback loop. For a temperature variation between -40^0 C and 100^0 C,the BGR of CMOS technology, and for a temperature variation between -40^0 C and 60^0 C, the BGR of BiCMOS technology, the produced reference voltages are absolutely independent of temperature variation together with the capability of operating at very low supply voltage (less than 1V).

1. INTRODUCTION

Reference voltage generators are used in A/D converters, D/A converters, DRAM's, flash memories, and so many applications in communication field.

Reference voltages or currents that exhibit little dependence on temperature prove essential in all analog circuits. Temperarure dependence of the reference voltage is definitely one of the most important issue in BGR design, as it directly affects the performance of such circuits. The output voltage of the conventional BGR is 1.25V which limits the operation of the BGR below 1.2V supply. To overcome this problem we use the conception of [12] fig1 to get a CMOS BGR operating below 1V supply .But we modify the OPAMP /Differential Pair by using a current mirror active load to get a better result[6]. The BGR obtained by the combination of these two idea we make a hybrid BGR circuit as shown in fig2.But this Hybrid BGR is also not absolutely temperature independent. To make it absolutely temperature independent we use a (-ve) feedback loop, that feeds a little part of the output voltage to the input in out of phase. We also use the conception of Voltage Divider biasing conception to make the proposed BGR more stable.

We know that BiCMOS technology is one of the leading technologies now a day. So use the same conception of (-ve) feedback to make the existing BiCMOS BGR of Marcovati[8]more stable. Before come to the circuit description and theory we want to go through some important points described below.

2. CIRCUIT DESCRIPTION AND OPERATION AND RESULT OF PROPOSED BGR IN CMOS TECHNOLOGY

The conventional BGR circuit is composed of a CMOS op-amp, diodes and resistors. This circuit is shown in below:

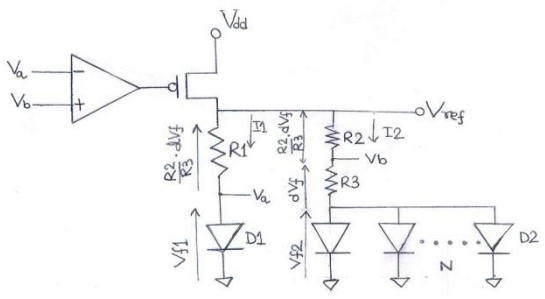

Fig 1.Conventional BGR Circuit

A general diode current versus voltage relationship is expressed as:

$$I = I_S * (e^{\frac{qV_f}{KT}} - 1)$$

$$\approx I_S * e^{\frac{qV_f}{KT}}$$

[As V_f is much greater than $\frac{KT}{q}$]

$$V_f = V_T * \ln \frac{I}{Is}$$

Where K is the Boltzmann's constant ($1.38*10^{-23}$J/K) and q is the electronic charge ($1.6*10^{-19}$C).
In the conventional circuit, a pair of input voltages for the op-amp V_a and V_b, are controlled to be the same voltage. dVf is the forward voltage difference between one diodeD1 and N diodes d2.

$$dV_f = V_{f1} - V_{f2}$$

$$= V_T * \ln(N \frac{R_2}{R_1}) \quad \text{…… …….. (3)}$$

The BGR output voltage V_{ref} then becomes

$$V_{ref} = V_{f1} + \frac{R_2}{R_3} df = V_{ref-con}$$

V_{f1} has a negative temperature coefficient of $-2mv/^0 c$ whereas V_T has a positive temperature coefficient of $0.086mv/^0 c$.

Thus the V_{ref} is determined by the resistance ratio. The value of V_{ref} is about 1.25V which limits the low-voltage design for the CMOS circuit.

The concept of the proposed BGR is that two voltages V_T and V_f are generated by only one feedback loop. The PMOS transistor dimensions of p1, p2 and p3 are the same, and the resistance values of R1 and R2 are same.

We know that if the gates of PMOS transistors are connected they will draw equal currents. For the same reason, $I_1 = I_2 = I_3$

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In this case, $I_{1a} = I_{2a}$ and $I_{1b} = I_{2b}$.

$$dV_f = V_{f1} - V_{f2} = V_T * \ln(N)$$

I_{2a} is proportional to V_T

$$I_{2a} = \frac{dV_f}{R_3}$$

I_{2b} is proportional to V_{f1}

$$I_{2b} = \frac{V_{f1}}{R_2}$$

Here, I_2 is the sum of I_{2a} and I_{2b}, and I_2 is same as I_3,

$$I_3 = I_2 = I_{2a} + I_{2b}$$

Therefore, the output voltage of the proposed BGR, V_{ref}, becomes

$$V_{ref} = R_4 (\frac{V_{f1}}{R_2} + \frac{dV_f}{R_3}) \equiv V_{ref-prop}$$

If the resistor and diode parameters for the proposed BGR are the same as those for the conventional BGR, $V_{ref-prop}$ is simplified as $V_{ref-prop} = \frac{R_4}{R_2} * V_{ref-con}$

Therefore, $V_{ref-prop}$ can be freely changed from $V_{ref-con}$ of 1.25V. V_{ref} For the proposed BGR is determined by the resistance ratio of R_2, R_3 and R_4 and little influenced by the absolute value of the resistance. The transistors M_1, M_2 and M_3 must operate in the saturation region, so that their drain-to-source currents are reduced.
We also modify the OPAMP to operate at low power supply voltage(1v)[6]
Implementation an OPAMP with 1V power supply is challenging. The OPAMP is modified as shown in fig.2.

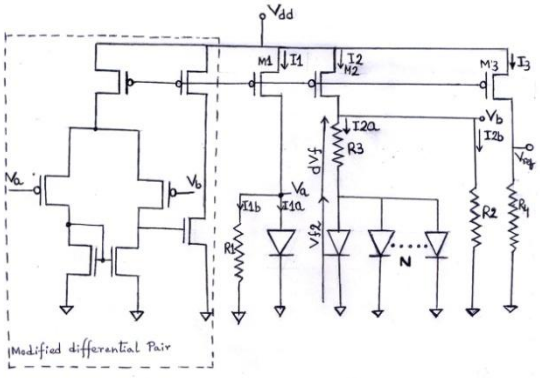

Fig.2 Hybrid BGR

Using this modified OPAMP and the theory explained above the BGR circuit generated is named as Hybrid BGR is shown in Fig2. This Hybrid BGR can operate definitely in sub 1V supply and can generate a reference voltage much lower than 1V, but the TC of the BGR output voltage is not zero. The BGR voltage varies with temperature ,though this variation is very low.

What we modify again in the Hybrid BGR of fig2 is that we apply a feedback loop at the out put of BGR to the (-Ve) input terminal of the modified OP-AMP. The modified BGR with the using of a feedback loop is shown in fig3, and is called Proposed BGR.

We all are familiar with the (-ve) feedback amplifier. In (-ve) feedback technique a very little part of output voltage or current are feeding to the input of the amplifier in out of phase. As a result the variation of the output voltage with the variation of the temperature reduces. And as a result we used to get a stable output even at the variation of the temperature in a large scale. This conception is used in this Proposed BGR circuit as well.

In the Hybrid BGR, we get a low voltage at the output of BGR, but this voltage varies with temperature. When we add the feedback loop at the output of the same BGR we get a fully constant output with respect to the variation of temperature. The new Proposed BGR with feedback loop is shown in fig.3.

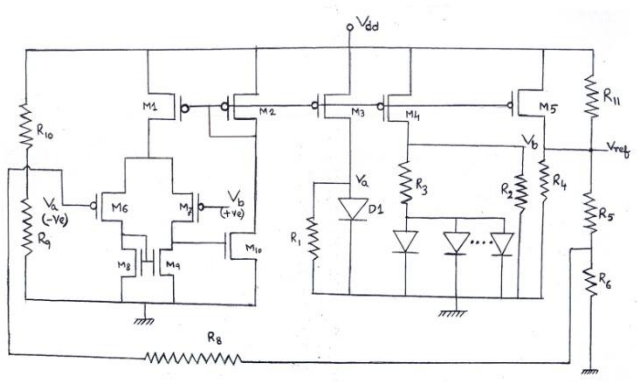

Fig.3 Modified Hybrid BGR

The output of the proposed BGR is lower than the Hybrid BGR at the same supply voltage for every equal conditions. So we can say that the feed back is a voltage series feedback

We also used the voltage divider biasing circuit to stabilize the operating point of the proposed BGR.

We also used the conception of voltage divider biasing to stabilize the proposed BGR circuit. In proposed BGR there is no change of BGR voltage when the temperature is changing from -40 degree centigrade to 100 degree centigrade. The BGR voltage is absolutely constant with Zero(0) TC.

3. OBSERVATIONS AND RESULT

In proposed BGR we not only get a absolutely stable voltage , the range of operation also becomes wider The comparison between the Hybrid BGR and the proposed BGR is shown in tabular form in Table1

Table1 According to the reading we can calculate the TC and PSRR as

T C in ppm/^{0} C.	**-40 ^{0} C**	**-20^0 C**	**0 ^{0} C**	**27 ^{0} C**	**50 ^{0} C**	**70 ^{0} C**	**90 ^{0} C**	**100^0 C**
0	0	0	0	0	0	0	0	0

PSRR in DB	**-40 ^{0}C**	**-20 ^{0}C**	**0^0 C**	**27 ^{0}C**	**50 ^{0}C**	**70 ^{0}C**	**90 ^{0}C**	**100^0 C**
7.660	7.660	7.660	7.660	7.660	7.660	7.660	7.660	7.660

From the comparison Table1 it is clear that the proposed BGR is much more better than the Hybrid BGR is all aspects.

4. PROPOSED BICMOS BGR

What is BiCMOS technology?

When both npn and pnp bipolar transistors can be added to a CMOS process, which is then called a BiCMOS process. These processes tend to be used for specialized analog or high-voltage circuits. In a regular n-well process, a parasitic pnp transistor is present that can be used for circuits such as Band gap voltage references. This transistor is shown in Fig4 with the p-substrate collector, the n-well base, and the p-diffusion emitter.

CIRCUIT AND THEORY:

Two components build up the output voltage of a band gap reference one is the voltage across a directly biased diode and other is a term proportional to the absolute temperature. The (-ve) temperature coefficient of the former tern compensates the (+ve) temperature coefficient of the latter. If $V_T = kT / q$ is used to obtain a PTAT voltage we have to multiply V_T by approximately 25 to compensate for the temperature dependence of the diode voltage. If this condition is satisfied, the generated band gap voltage becomes approximately 1.2v.Using a supply voltage (V_{DD}) as low as 1v,obviously 1.2v cant be produced, we can generate a fraction of 1.2v with similar temperature features. Since the Band Gap voltage is given by

$$V_{BG} = V_{BE} + n\frac{kT}{q} \quad \text{.....(1)}$$

We achieved a fraction of the traditional band gap voltage by scaling both terms of Eqn.(1),using currents terms proportional to V_{BE} and to V_T, respectively. These currents are suitably added and transformed into a voltage with a resistor.

The temperature dependence of the resistors used is compensated by fabricating them always with the same kind of material. Fig 1shows the block diagram of the BGR in BiCMOS technology by Malcovati. diode connected bipolar transistors drain the same current given the used emitter area ratio, N, ΔV_{BE} is equal to $V_T \ln(N)$ .Therefore, the current in R_0 is PTAT.The operational amplifier forces the two voltages V_A and V_B to be equal, thus producing a current in the equal resistors R1 and R2 proportional to V_{BE}. As a result the current in M1,M2 and M3 ($I_1=I_2=I_3$) is given by

$$I_1 = \frac{V_T}{R_0}\frac{\ln(N)}{} + \frac{V_{BE}}{R_1} \quad \text{.....(2)}$$

The output voltage is given by

$$\text{.....} \quad V_{out} = I_1 R_3 = V_T\left(\frac{R_3 \ln(n)}{R_0}\right) + V_{BE}\left(\frac{R_3}{R_1}\right) \quad \text{.....(3)}$$

The temperature coefficient of resistor is cancelled if resistors are made withthe same resistive layer. The compensation of the temperature coeffof V_T and V_{BE} is ensured by a proper choice of N and of the R_0 / R_1 ratio By I Inspection of the circuit we observe that the minimum supply voltage is determined by the V_{BE} plus a saturation voltarange of a p-channel transistor. Therefore, 1v can be enough to opera initiate the circuit.

OPERATIONAL AMPLIFIER DESIGN

Theband gap circuit needs an operational amplifier whose input common mode voltage is around 0.65v (the V_{BE}).also since the output nodedrives p-channel current sources, its quiescent voltage should be belo $V_{DD} - Vth, p.$ Assuming V_{DD}=1v and $V_{th,p}$ =0.7v the output volt resulis as low as 0.15-0.2v.Moreover, the gain of the Opamp must be arou 60dB without any bandwidth constraints. The above design cond itionstion lead to the following considerations[8]

Malcovati designs the OPAMP for low voltage operation amplifier is shown below in Fig4

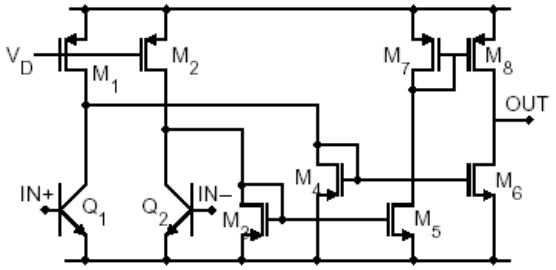

Fig 4.Malcovati design of OpAmp

The considerations for design of OPAMP in BiCMOS technology for low voltage power supply are:

1. The input common mode voltage makes it difficult to accommodate an n-channel input differential stage. Possible, a level shift of the input voltages by 150-200 mv is necessary.

2. The low output voltage prevents the use of cascode configurations. Therefore, two-stage architectures should be used.

3. The required biasing conditions can lead to a significant offset, which can become the key limit to the correct operation of the Band Gap circuit.

A careful analysis of the above issues shows that we can use a CMOS technology with a supply only if the thresholds of the n-channel and p-channel devices are 0.5v or below. However, a BiCMOS technology (or a CMOS with lateral BJT) allows us to design an Operational amplifier suitable for 1v operation even with threshold voltages 0.7v.So according to Malcovati,and after the modification of the OPAMP the BGR circuit achieves 5ppm/k degree of accuracy.

The new OPAMP circuit does not use an differential stage but two grounded bipolar transistors.

The combination of the diode connected BJT in the band gap and the BJT of the input stage constitutes a current mirror. Therefore, the currents in the input stage of the operational amplifier do not need control, being a replica of the current in the band gap structure. Two diode connected MOS devices receive the signal current and lead to the following differential gain

$$A_d = \frac{g_{m,BJT}}{g_{m,MOS}} = \frac{I_{BJT} / V_T}{2I_{MOS} / (V_{GS} - V_{Th,n})} \quad \text{....(4)}$$

Where the suffix BJT refers to the input BJT and the suffix MOS refers to the diode loads M3 and M4.Assuming ($V_{GS} - V_{TH,n}$) = $4V_T$ and using I_{BJT} =$4I_{MOS}$ with a gain of 16. Since the input gain stage is fully symmetrical its systematic offset is zero. Moreover, a possible offset from the second stage is divided by 16.The second stage is a push-pull circuit. Since the quiescent value of the output voltage is one $V_{GS,p}$ below V_{DD} , the V_{DS} voltages of M7 and M8 match and the systematic offset of the second stage is zero as well. The bias current used is kept at a very low level,since we want to maximize the gain and bandwidth is not important. However, since the bias current of the circuit has a PTAT feature power consumption will increase proportionally to the absolute temperature. This variation is irrelevant even when using the circuit in the range from -20^0c to 120^0c.The operational amplifier was designed using a 0.8um BiMOS technology.

What we do new, we add a (-ve) feedback loop at the output of Muscovite's BiCMOS BGR ,and get a Absolutely stable BGR voltage at the temperature range *of* -40^0 C to 60^0 C .So we also get aBiCMOS BGR with 0TC with the help of a (-ve) feedback loop. The proposed BGR of Bi CMOS which we named as 'Optimum BGR'is shown in Fig5.

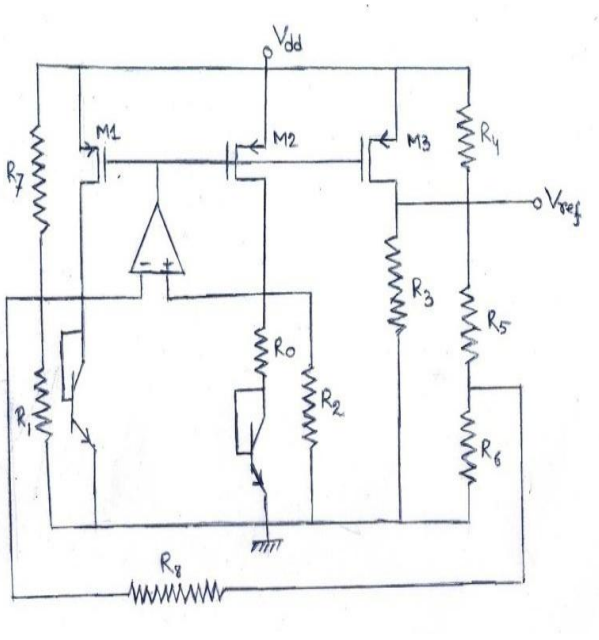

Fig.5 Optimum BGR

5. RESULT

According to the reading we can calculate the TC and PSRR as

T C in	**-**	**-**	**0**	**27**	**50**	**70**	**90**	**10**

ppm/0 C.	**40 0 C**	**20^0 C**	**0 C**	**0 C**	**0 C**	**0 C**	**0 C**	**0^0 C**
0	0	0	0	0	0	0	0	0

PSRR in DB	**-40^0 C**	**-20^{0}C**	**0^0 C**	**27^0 C**	**50^0 C**	**70^0 C**	**90^0 C**	**100^0 C**
.1716	.1716	.1716	.1716	.1716	.1716	.1716	.1716	.1716

It is clear from the above table that the output of the BGR is absolutely constant for the temperature range shown above. But the drawback of the circuit is that it can not give a constant output beyond this temperature range. Also the PSRR of both the circuits are very low.

6. CONCLUSSION

The proposed BGR in CMOS and Bi-CMOS technology can give a constant output voltage with the variation of temperature from -400c to 1000c with the supply voltage variation as lower as possible to as higher as possible .we can say that it is a versatile achievement. But the drawback of these circuits are that ,their stability is very much dependent on the resistance values and their PSRR are very low. So in future we will try to get BGRs having higher PSRR and lesser dependency on resistance values.

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