Circuit-Level Design of a Power Supply Unit with Extra Low-Noise Output for Portable Integrated SoCs

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ABSTRACT

Switch-mode voltage regulators are considered as the dominant choice for low-power integrated power supplies. Employing the advantages of a switch-mode voltage regulator in 0.18μm CMOS technology, a power supply has been designed for a complete System-on-Chip (SoC). While offering enough drive capability for the entire system, the supply provides an extra highly-regulated output for noise-sensitive analog blocks. At first, a front-end buck regulator converts the time-variant unregulated input voltage to an initially-regulated general voltage. To further regulate this voltage for noise-sensitive blocks, a new continuous-time buffered voltage source has been added to the circuit. To maximize power efficiency and to benefit from an initially-regulated input, this source is connected to the front-end switch-mode regulator output. For proper operation, the minimum input voltage to the supply is 1.3V. With this minimum input voltage, the 1.1V switching regulator sources up to 1A output current. The continuous-time 0.9V- buffered source provides up to 100*m*A for noise-sensitive units. It converts the 1.1V regulated voltage to a 0.9V smooth output.

General Terms

Low-dropout regulators, switch-mode regulators, voltage reference

Keywords

Frequency compensation, linear regulators, low-dropout regulators, output noise, power-supply rejection, stability, switch-mode regulators, voltage reference.

1. INTRODUCTION

Switching mechanism is essential for designing power supplies capable of driving heavy resistive and capacitive loads with high power efficiency. As a result, switching regulators achieve a wide variety of applications for portable systems some of which are cell phones, laptops, and wireless transceivers. When optimized properly, they can efficiently convert a time-variant battery voltage to a pre-determined, stable, and moderately-regulated output. In these regulators, the periodic mechanism of transferring and storing energy, from magnetic in an inductance into electrical in a capacitor, is carried out using switches regularly connecting and disconnecting the input voltage to the output. Unfortunately, switching injects noise to the output. Recent studies to model this noise show that its magnitude can be considerably higher than the value predicted by available simulators [1]. Hence, switching regulators are avoided when noise level is of main concern. For such cases, a design approach based on solely linear regulators is adopted at the cost of lower efficiency [2].

A general-purpose power supply with 1.3V minimum input voltage, a 1.1V moderately-regulated voltage with 1A driving capability for digital units and at last 0.9V-100*m*A smooth and highly-reliable voltage for certain analog noise-sensitive blocks has been designed in this work. To realize the 0.9V-100*m*A output node, a modified architecture with numerous advantages with respect to the conventional low-dropout regulators is devised [3].

2. SWITCHING REGULATOR OF THE DESIGN

Fig 1 shows system-level architecture of the regulator used to convert the input voltage to a 1.1V-1A output [4-9]. The structure of this DC-DC converter, with more details, is depicted in Fig 2. The power line, consisting of *L* and *C* and

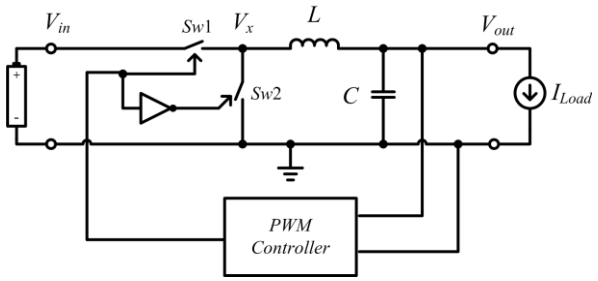


Fig 1: System-level architecture of the converter

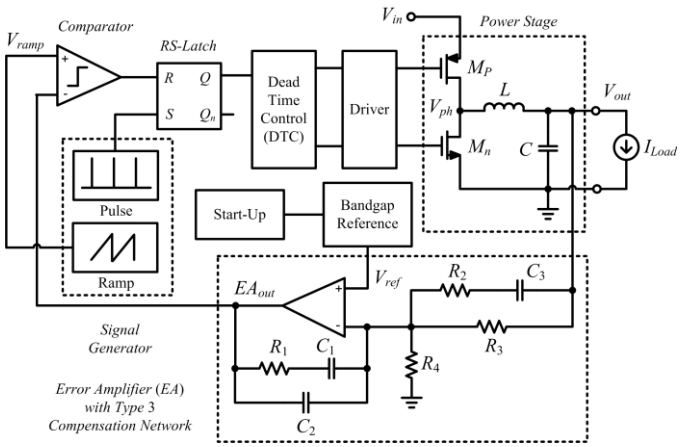


Fig 2: The structure of the switching buck regulator, with more details

power switches *Sw*1 and *Sw*2, periodically stores and transfers energy from input supply voltage (V_{in}) to the load (I_{Load}). The controller unit based on pulse-width-modulated control signal (*PWM Controller*) adjusts the output voltage to a pre-determined value. By periodically exciting the two switches labeled as *Sw*1 and *Sw*2, the state of V_x does change between supply and ground. The average value of this voltage passes through an ideally lossless *LC* filter to generate the output voltage (V_{out}). To maintain regulation, V_{out} is made a function of the duty cycle of *Sw*1 (*D*). The duty cycle is automatically controlled by a *PWM* control signal to compensate the effects of load current and temperature on V_{out}. Denoting T_{on} as the interval *Sw*1 is on, T_{off} as the interval the switch is off, T_S as switching period and f_S as switching frequency, we will obtain [4]

$$D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{T_{on}}{T_S} = T_{on} f_S, \quad (1)$$

$$V_{out} = V_{in} D. \quad (2)$$

In practice, as $0 < D < 1$, V_{out} is always smaller than V_{in} . By dynamically adjusting *D* with a feedback mechanism, it is always possible to regulate output, regardless of the value of V_{in}. Fig 2 represents a circuit-level implementation of this mechanism. Here, the *Power Stage* block has two power switches (M_P and M_n), one inductance *L* and one capacitance *C*. To maintain regulation, each of the blocks tagged as *Error Amplifier* and *Compensation Network*, *Comparator*, *Signal Generator*, *Bandgap Reference* with *Start-Up*, *Driver* and, *Dead Time Control* (*DTC*) operate properly based on a mechanism described as follows.

By periodically switch on or off devices M_P and M_n, V_{out} can be regulated. For this to happen, modulation of *D* based on a parallel-feedback mechanism is necessary. This mechanism operates as follows. A ratio of the output voltage R_4V_{out} / (R_3+R_4) is initially compared with a reference voltage (V_{ref}). After comparison, a low-frequency error signal is generated by the error amplifier (EA_{out}). Comparing the error signal with a periodic ramp signal (V_{ramp}), a pulse-width modulated voltage thus is generated that determines the interval each power switch should stay on.

Table 1 shows the system-level specifications of the switching regulator that is designed for this power supply unit. Using off-chip *LC* components with intrinsic resistance of 10*m*Ω, the magnitude of the output-transferred spikes should not exceed from 100*m*V. With 1MHz switching frequency, transient load- and line- regulations should be also smaller than 5%.

Table 1. Device sizes and element values of the design

Technology	0.18μm CMOS Technology
Output Voltage	1.1V
Minimum Input Voltage	1.3V
Maximum Load Current	1A
Switching Frequency	1 MHz
Worst Case Output Ripple	< 100*m*V
Transient Line Regulation (1.3V, 1.8V)	< 5%
Transient Load Regulation (0A, 1A)	< 5%
C, ESR	470 μF, 10*m*Ω
L, DCR	3.9 μH, 10*m*Ω

To achieve a wide bandwidth while maintaining stability, the regulation loop of Fig 2 has been stabilized using an advanced compensation network. Shown in Fig. 3, the error amplifier is a two-stage Miller-compensated opamp [10]. The output stage of this amplifier is a class-AB that efficiently sources and sinks the required load current under different load conditions. The input-output transfer function of Fig 3 is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s(R_1/C_1 + R_2/C_3 + R_3/C_1) + s^2 R_2(R_1+R_3) + 1/C_1C_3}{s^2(R_1R_2C_2/C_3 + R_1R_3C_2/C_1 + R_1R_3) + s(R_1C_2/C_1C_3 + R_1/C_3) + s^3 R_1R_2R_3C_2}. \quad (3)$$

With wide track bandwidth, this method proves to be useful for achieving high-speed transient line- and load- regulations [6]. Resistors and capacitors can be optimized to push the speed/stability envelope away as much as possible.

The feedback path of Fig 2 also contains a continuous-time comparator for comparing EA_{out} - V_{ramp}. Simplicity and small propagation delay between input and output are the two fundamental requirements of this block. The employed comparator of this design combines both features simultaneously [11]. To generate pulse and ramp signals of Fig 2, a design approach based on digital flip-flops was developed [8]. At last, low-voltage architecture of [12] was employed to generate a stable bandgap reference voltage.

A. System-level simulation of the switching regulator

Unlike linear regulators, numerous number of cycles and consequently a long period is required to characterize the behavior of a switching regulator under different transient load-, line- and start-up conditions. Additionally, almost all the building blocks of a switching regulator have their role on the output response. When all these factors are included into a circuit-level simulator, every single simulation of the regulation loop becomes a time-consuming process. This complicates the design and optimization of the regulator and makes it difficult to specify an optimized structure within a due course. To speed up the process and to investigate the system-level behavior of a switching regulator under transient conditions, VHDL behavioral models are developed to be replaced with real circuits [4,13]. When modeled carefully, while simulation speed is getting dramatically higher than the circuit-level simulator, the accuracy of the results is comparable.

In this design, regarding the need to study the stability of the regulator under different conditions, a system-level prototype is implemented within *Matlab Simulink*. The initial model was designed with the aim to achieve the specifications of Table 1. With this model, it is made possible to optimize the system-level key parameters such that stability is guaranteed. Fig 4

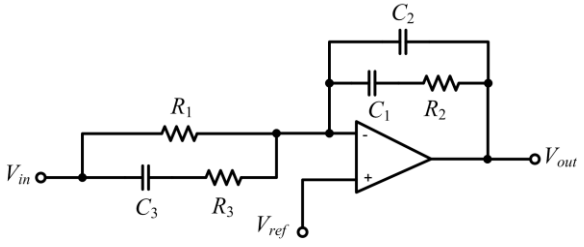


Fig 3: Circuit-level implementation of the compensation network along with the error amplifier of Fig 2

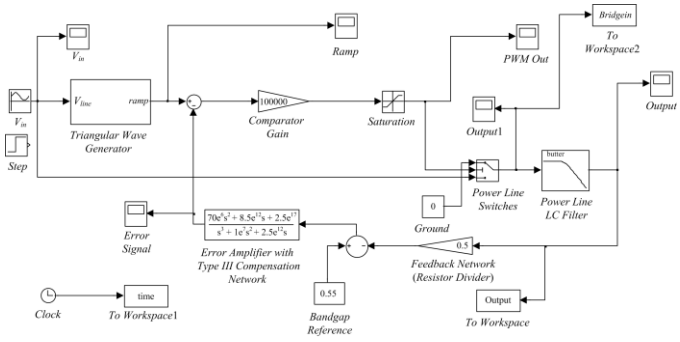


Fig 4: Simulink model of the switching regulator in Fig 2

illustrates the employed system-level model of Fig 2. As it is clear, linear behavioral model of all blocks is available in this environment. For instance, a second-order filter is replaced with *LC* pair of the power-line. A two-state voltage-controlled switch is replaced with power-line switches. The transfer function of (3) is used to model the behavior of error amplifier and compensation network and so on. Using this model, both start-up response and stability of the regulator are optimized.

B. Circuit-level simulation of the switching regulator

In this research, the voltage regulator shown in Fig. 2 is simulated in TSMC 0.18μm CMOS technology. The solid-line in Fig 5 depicts the start-up response of the result with 1.3V supply voltage and 0.1A output current. As it is seen, the start-up response of the circuit is similar to the result of the system-level simulation shown as a dotted line. The difference is between moments the output response settles down to its final value. This originates from the fact that system-level model does not account for second-order and non-linear effects such as limited slew-rate and load current drive capability. However, system-level representation succeeds to accurately predict the regulation loop stability. Fig. 6 shows the bandgap reference output curve against temperature. This voltage maintains the switching output to its predetermined value, i.e. 1.1V. For 1.3V voltage supply, steady-state power consumption of the reference is roughly 44μW. Fig 7 illustrates the required ramp and pulse signals of the feedback path. The steady-state switching frequency is approximately 1MHz. For 1.3V supply voltage, the current drawn by this

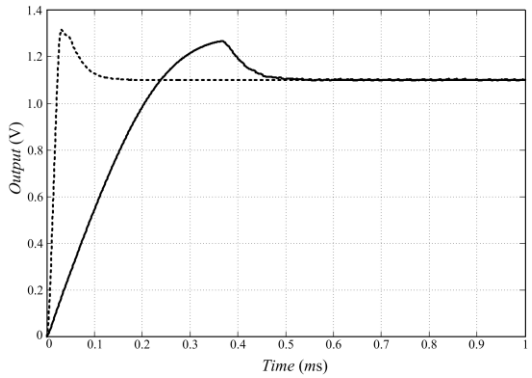


Fig 5: Start-up transient response of the regulator for 1.3V line voltage
Solid: circuit-level simulation
Dotted: system-level simulation

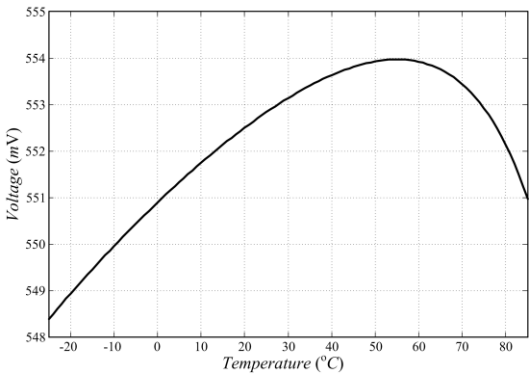


Fig 6: Reference voltage output curve against temperature

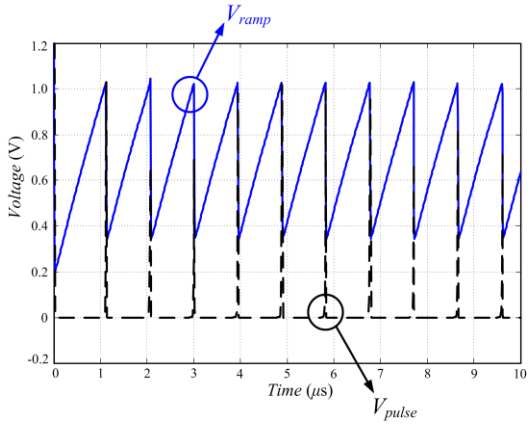


Fig 7: Ramp and pulse signals generated by the feedback controller

block is 100μA. For 1A maximum load current and 1.8V maximum input supply, Fig 8 presents the current consumption of the entire switching regulator. The average value of this current, including static and dynamic harmonics, is 947μA. For 0A and 0.1A load currents, this value decreases to respectively 939μA and 941μA. For 1.3V line voltage and 1A load current, the average current is 650μA.

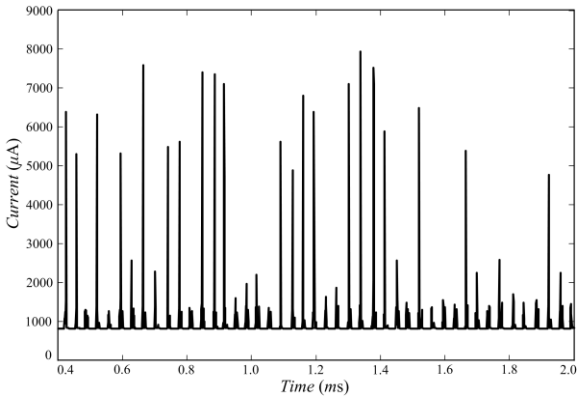


Fig 8: Current drawn from 1.8V power supply through switching regulator in case of maximum load current (1A)

3. LINEAR VOLTAGE SOURCE OF THE DESIGN

Fig 9 shows the proposed architecture susbstituted with conventionally-used low-dropout regulators (LDOs). The circuit is capable of supplying high load currents. Besides, its absolute value can typically be chosen smaller, equal, or larger than the silicon bandgap voltage, 1.2V. As another advantage over LDO, the temperature-sensitivity of the proposed reference can be smaller for identical area and power. In this configuration, the negative input terminal of error amplifier is biased via a simple complementary-to-absolute-temperature (CTAT) voltage source. In order to directly compensate for the temperature dependence of the output voltage, a PTAT current source has also been added. Assuming a high DC gain for the amplifier, the reference voltage (V_{ref}) can be calculated from

$$V_{out} = (1+\frac{R_2}{R_1})V_{CTAT} + R_2 I_{PTAT}. \quad (4)$$

The two temperature-dependant signal sources can directly cancel out each other in the output. The result is therefore a buffered voltage source with low-sensitivity to temperature variations. Fig 10 depicts a possible circuit-level implementation of this approach [3]. In 0.18μm CMOS technology, the circuit is simulated for 1.1V minimum line voltage, and 0.9V output voltage. The design always consumes less than 50μA of current. Its temperature-coefficient equals 36ppm/^{o}C for T = [-25^{o}C, 85^{o}C] of temperature range. Fig 11 illustrates the output voltage curve as a function of load current and temperature.

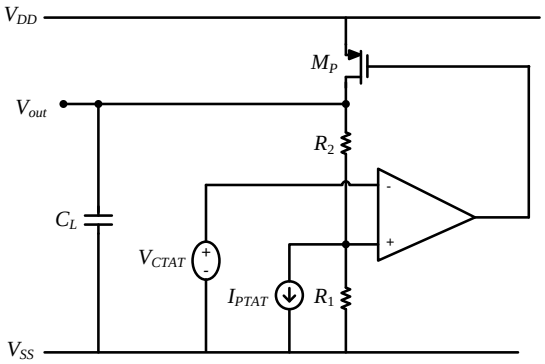


Fig 9: Proposed structure to implement a buffered voltage reference

4. CIRCUIT-LEVEL IMPLEMENTATION OF THE SUPPLY

The described power supply, with switching regulator described in Section 2 and voltage reference of Section 3 is simulated in this research (Fig 12). The switching regulator output is 1.1V while the output of the linear voltage source is 0.9V. This makes it possible to permanently maintain the proposed voltage reference at the edge of its dropout voltage, thereby maximizing power efficiency. The maximum load current of the switching regulator is 1A. A small portion of this current is drawn by the 100mA voltage reference. With no further regulation required digital logics, as the main part of the system, directly supply from the switching output. Fig 13 illustrates the transient-line regulation of the switching output. This happens when the line voltage is a pulse stepping from 1.3V to 1.8V and from 1.8V to 1.3V. It proves the fact that the variations of the main supply, when transferred to reference reference output, are highly attenuated.

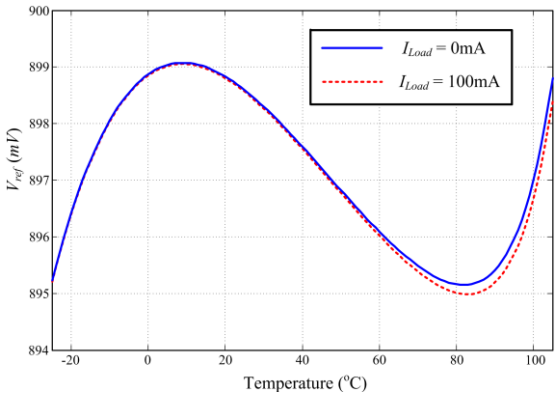


Fig 11: Reference voltage as a function of load current and temperature

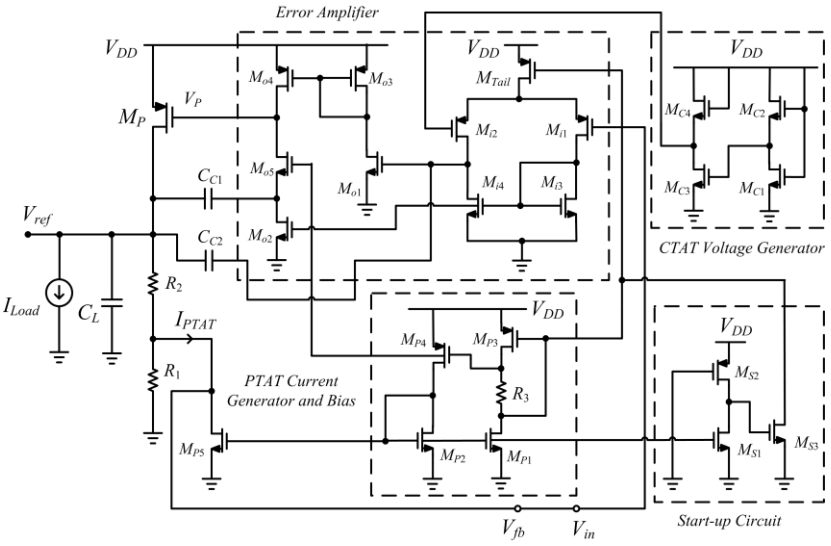


Fig 10: A possible implementation of the reference of Fig 9

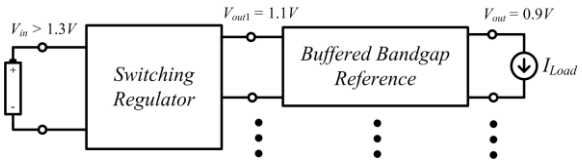


Fig 12: The simulated power supply

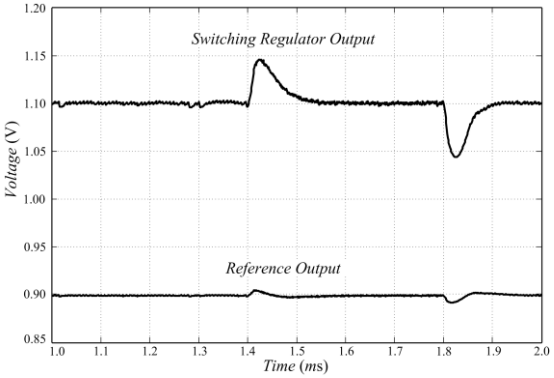
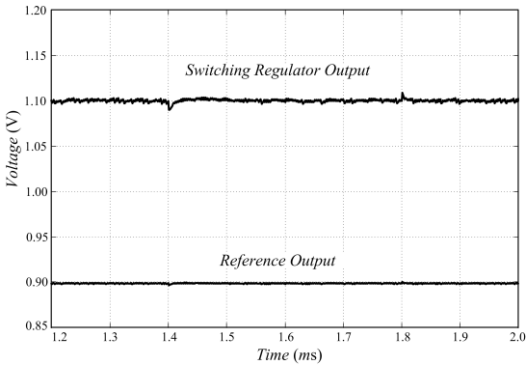


Fig 13: Transient-line regulation of the regulator and its effect on the reference output, input voltage steps from 1.3V to 1.8V and aand from 1.8V to 1.3V

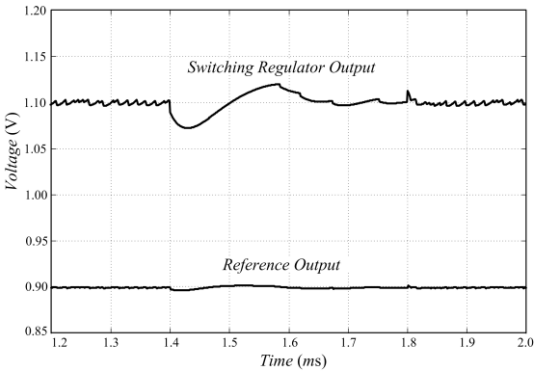
To further investigate the behavior, the effect of switching regulator transient-load regulation is considered on buffered reference. For 1.3V and 1.8V supply voltages, a 1A pulse current was applied to the switching output. Fig 14 presents the results. As it is clear, the fluctuations of switching output are suppressed when propagated to reference output.

5. CONCLUSIONS

In general, there are two options to regulate a noisy variable input supply to a pre-determined value; linear regulation and switching regulation. Linear regulators are continuous-time with high power-supply rejection, and less complicated compared to switching regulators. In contrast, switching regulators are more power-efficient and propagate less heat. For portable applications although high power-conversion efficiency increases battery life-time, the generated electrical and magnetic noise level usually becomes unacceptable for analog and RF applications. Simulation procedures of a buck DC-DC converter are discussed in this paper. By designing of a switching regulator in 0.18μm technology, simulation results of a complete power supply are presented. The linear voltage regulator of the architecture is a modified voltage reference with more operational advantages.



(a)



(b)

Fig 14: Transient-load regulation of the switching regulator and its effect on the reference output, load current steps from 0A to 1A and from 1A to 0A (a) 1.8V supply voltage (b) 1.3V supply voltage

6. REFERENCES

[1] V. Binet, Y. Savaria, M. Meunier, and Y. Gagnon, "Modeling the Substrate Noise Injected by a DC-DC Converter," *Proc. IEEE Int. conf. on Circuits and Systems* (*ISCAS* 2007), pp. 309-312, 2007.

[2] V. Gupta, and G. A. Rincon-Mora, "A Low Dropout, CMOS Regulator with High PSR Over Wideband Frequencies," *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 4245-4248, K Japan, 2005.

[3] H. Aminzadeh, R. Lotfi, and K. Mafinezhad, "Low-Dropout Voltage Reference: An Approach to Low-Temperature-Sensitivity Architectures with High Drive Capability," *Electronics Letters*, Vol. 45, Issue 24, pp. 1200,1201, Nov. 2009.

[4] H. P. Forghani-Zadeh and G.A. Rincon-Mora, "Fast and Reliable Top-Level Simulation Strategy for Mixed-Signal Integrated Circuits and its Application to DC–DC converters," *IET Circuits Devices Syst.*, 2007, pp. 143–150, Jan. 2007.

[5] H.P. Forghani-Zadeh, and G.A. Rincon-Mora, "Low-Power CMOS Ramp Generator Circuit for DC-DC Converters," *J. Low Power Electronics*, vol. 2, pp. 1-5, 2006.

[6] B. Sahu, and G. A. Rincón-Mora,"A Low-Voltage, Dynamic, Noninverting, Synchronous Buck-Boost Converter for Portable Applications," *IEEE Trans. Power Electronics*, vol. 19, Mar 2004.

[7] M. D. Mulligan, B. Broach, and T. H. Lee, "A 3MHz Low-Voltage Buck Converter with Improved Light Load Efficiency," *Int. Solid State Circuit Conf. (ISSCC), Dig. Tech. Papers*, pp. 528-529, 2007.

[8] K. Schulmeyer, *A Sigma-Delta Based DC-DC Converter*, MSc. Dissertation, Texas Tech University, Dec. 2007.

[9] C. F. Lee and P. K. T. Mok, "A Monolithic Current-Mode CMOS DC-DC Converter with On-Chip Current-Sensing Technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 3-14, Jan. 2004.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

[11] Y. Bing, L. Xinquan, Y. Qiang, and J. Xinzhang, "A Novel Compact Soft-Start Circuit with Internal Circuitry for DC-DC Converters," *Proc. 7th Int. Conf. on ASIC* (*ASICON*'07), pp. 450-453, 2007.

[12] K. N. Leung and P. K. T. Mok, "A Sub-1-V 15ppm/°C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device," *IEEE J. Solid-State Circuits*, pp. 526-530, Apr. 2002.

[13] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Analysis of Buck Converters for On-Chip Integration with a Dual Supply Voltage Microprocessor," *IEEE Trans. VLSI Syst.*, vol. 11, pp. 514–522, June 2003.