DVCC based Readout Circuitry for Water Quality Monitoring System

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ABSTRACT
A new configuration realizing water quality monitoring device using ISFET involving CMOS differential voltage current conveyor (DVCC) based low pass filter free from trans-conductance variation using Low-voltage PMOS bulk-driven cascade current mirror (P MOS BDCCM) current mirrors is proposed. The circuit uses four DVCCs as active elements and together with two capacitors and five resistors as passive elements, only one current mirror. The use of this active component makes the implementation simple and attractive. The functionality of the circuit is tested using Tanner simulator version 15 for a 70*nm* CMOS process model also the transfer function realization is done on MATLAB R2011a version, the Very high speed integrated circuit Hardware description language(VHDL) code for the same scheme is simulated on Xilinx ISE 10.1 and various simulation results are obtained. Simulation results are included to demonstrate the results.

General Terms
Capacitor, Simulation, Resistor, Active Component.

Keywords
Water quality monitoring, Ion Sensitive Field Effect Transistor (ISFET), Differential Voltage Current Conveyor (DVCC).

1. INTRODUCTION
As population is increased exponentially, monitoring the pH of water resources and sewage system for water pollution is typical and necessary task in today's overdeveloped scenario. Now a day's we have Semiconductor based micro sensors which are easily available and economical and able to react with the ion concentration, in other words activity of the ions. The ISFET has many feature like small size, high sensitivity and single chip integration, also it can be implemented by CMOS technology. These features make it, first choice for VLSI electrochemistry biomedical applications. ISFET has been modeled and has been found several drawbacks related to thermal dependency, long-term drift, linearity, dynamic range [1]. To improve the accuracy in the biomedical applications, it is necessary to find the compensation method to make the applications free from these effects. In order to capture the output response of the ISFET sensors, a readout interface is necessary. In this paper a new readout interface circuit having greater linearity, low power consumption, large bandwidth, by using current mode circuits (CMC's) is proposed.

Conventional water quality monitoring applications are made up of voltage mode circuits (VMC) based on op-amps and OTA's. These applications are suffer from low band widths (BW's) arising due to stray and circuit capacitances. Also the need for low voltage, low power circuits makes these circuits not suitable for water quality monitoring as these circuits required the minimum bias voltage depends on the threshold voltage of the MOSFETs. However, with the advancement in the analog VLSI new analog devices are based on currents are developed called current mode circuits (CMC's). These circuits have a significant advantage of low power, low voltages and can operate over wide dynamic range. These circuits, CMC can offer to the designer large bandwidths, greater linearity, wider dynamic range, simple circuitry and low power consumption. Current feedback op-amps (CFOAs), operational floating conveyors (OFCs) and current conveyors (CCs) etc. are popular CMC configuration and most widely used structure among them is DVCC, extension of the second-generation current conveyor (CCII). Hence, we decided to use the DVCC in the proposed scheme.

2. DVCC
The differential voltage current conveyor (DVCC) is an extension of the second-generation current conveyor (CCII) introduced by Sedra and Smith [2]. Recently, the CCII has been realized using MOS transistors, with the intention to integrate the different CCII circuit applications on one chip [3-4]. The CCII proves to be a versatile building block that can be used to implement a variety of high-performance circuits which are simple to construct. The DVCC is a five-port building block as shown in fig. 1. It has two voltage input terminals: Y1 and Y2, which have high input impedance. The terminal X is a low impedance current input terminal. There are two high impedance current output terminals: Z1 and Z2.

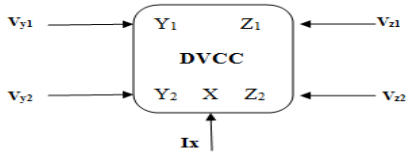

Fig. 1 Electrical symbol of DVCC

Its input-output terminal relations are given by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix}$$

The DVCC is a versatile building block for applications demanding floating inputs. The CMOS realizations of this

block are given. The proposed circuits are insensitive to the threshold voltage variation caused by the body effect. This minimizes the layout area and makes the circuit compatible with standard CMOS processes. The output currents (I_{Z1} and I_{Z2}) follows the input current through terminal X. I_{Z1} has the same polarity as I_X, and I_{Z2} is in the opposite polarity as I_X. The voltage of X terminal is related by the two input voltages:

$$V_X = V_{Y1} - V_{Y2} \quad (1)$$

2.1 CMOS realization of DVCC

The circuit realization of the proposed DVCC(Fig. 2) is based on equalizing the output currents of two wide linear range trans conductors, formed by transistors(M1–M18).In addition, (M19–M22) comprise Class-AB output stage, providing current swings up to ±1mA.Moreover, the cur- rent at the X terminal is transferred to the Z terminal with the aid of(M23,M24), which must be–for a unity current gain matched with (M21,M22), respectively.[5] All transistors are assumed to be operating in saturation. The operation of a wide linear range trans conductor relies mainly on biasing along tail differential pair (M1–M2).

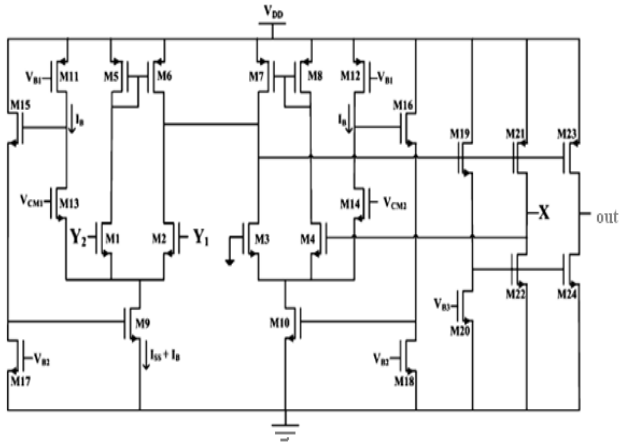

Fig2. Circuit diagram of CMOS based DVCC

3 DEVICE DESCRIPTION

The proposed scheme is consists of (1) ISFET (2) DVCC based device (3)Current follower (4)Current mirror circuit for the proper biasing of current conveyors (5)LCD display to show the output thus obtained. The circuit diagram of the proposed scheme is shown below, in fig.3 it consists of four DVCC, two capacitors, five resistors, ISFET, Current Mirror One of the drawbacks of the Current conveyor device is that its trans conductance (gm) varies often with the I_{bias}. To make the device free from trans conductance variation we used current mirrors along with the current conveyors which are capable of providing the constant I_{bias} and thereby, making the device free from change of trans conductance effect. Various kinds of Current mirrors are found but, to make the design low power PMOS bulk-driven cascade current mirror is used. The topology of the low-voltage PMOS bulk-driven cascade current mirror is used to control the gm of the DVCC.

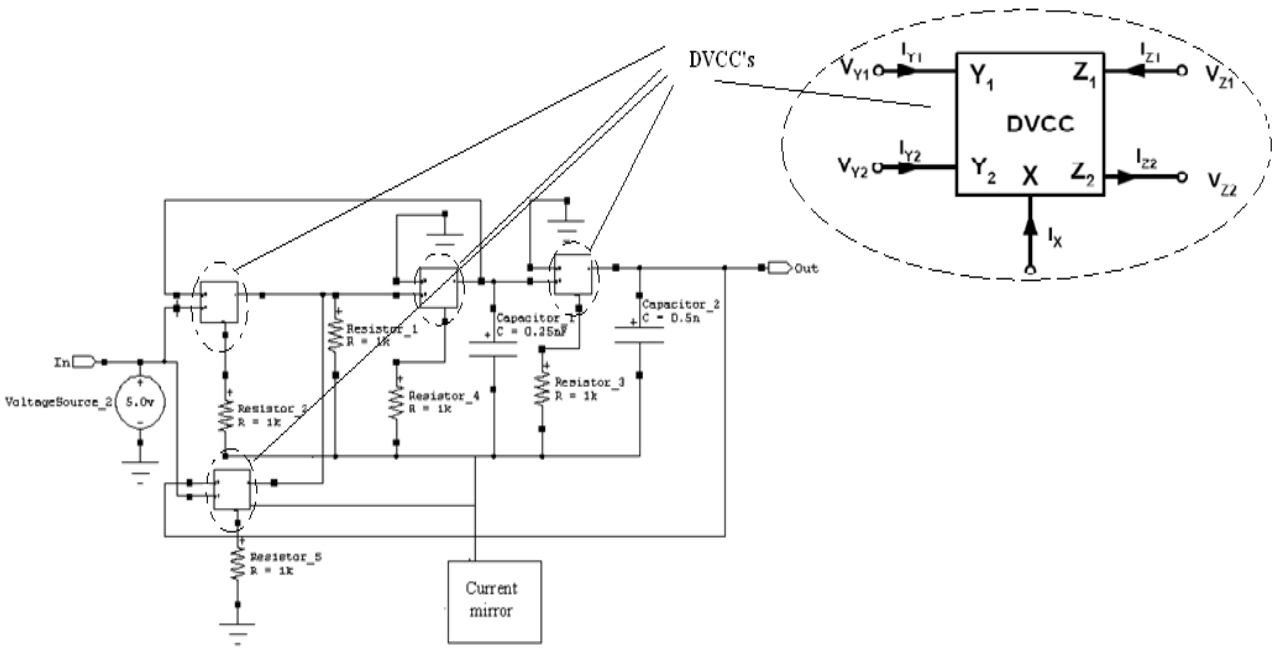

Fig.3 Circuit diagram of LPF using four DVCC and passive components

3.1 ISFET

An ISFET is an ion-sensitive field-effect transistor which has a property of measuring ion concentrations in solution; when the ion concentration (such as H^+) changes, the current through the transistor will change accordingly [6]. Here, the solution is used as the gate electrode. A voltage between substrate and oxide surfaces arises due to an ions' sheath. The ISFET has the similar structure as that of the MOSFET except that the poly gate of MOSFET is removed from the silicon surface and is replaced with a reference electrode inserted inside the solution, which is directly in contact with the hydrogen ion (H+) sensitive gate electrode [7].

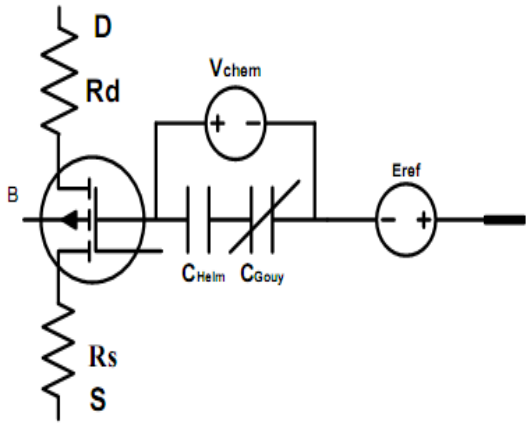

Fig.4 Sub circuit block of ISFET macro model

At the interface between gate insulator and the solution, there is an electric potential difference that depends on the concentration of H+ of the solution, or so called, pH value. The variation of this potential caused by the pH variation will lead to modulation of the drain current [8]. As a result, the Id-Vgs transfer characteristic of the ISFET, working in triode region, can be observed similar with that of MOSFET:

$$I_{ds}= \frac{\mu C_{ox} W}{L} [(V_{gs}-V_{th\_isfet}) V_{DS} - \frac{1}{2} (V_{ds})^2] \quad (2)$$

The threshold voltage is only different in case of MOSFET. In ISFET, defining the metal connection of the reference electrode as a remote gate, the threshold voltage is given by:

$$V_{th(ISFET)}=E_{Ref}+\Delta\phi^{1j}-\Psi_{eol}+\chi^{sol}+\frac{-\phi_s}{q}-\frac{Q_{ox}+Q_{ss}}{C_{ox}}+\gamma\{2\varphi£\}^{1/2}+2\phi_{£} \quad (3)$$

Where E_{Ref} is Potential of reference electrode, $\Delta\phi^{1j}$ is the potential drop between the reference electrode and the solution, which typically has a value of 3mV [9]. Ψ_{eol} is the potential which is pH-independent; it can be viewed as a common-mode input signal for an ISFET interface circuit in any pH buffer solution and can be nullified during system calibration and measurement procedures with a typical value of 50 mV [10]. χ^{sol} is the surface dipole potential of the solvent being independent of pH., the terms in the parentheses are almost the same as that of the MOSFET threshold voltage except that of absence of the gate metal function. The other terms in above equation are a group of chemical potential, among which the only chemical input parameter shown has to be a function of solution pH value. This chemical dependent characteristic has already been explained by the Hal and Eijkel's theory [11] which is elaborated using the general accepted site-binding model and the Gouy-Chapman-Stern model.

3.2 Mathematical Modeling

The transfer function of the proposed scheme is calculated as below

$$\frac{V_L}{V_i} = \frac{(R(R_3+R_4)/R_1C_1R_2C_2R_3R_4)}{D(S)} \quad (4)$$

$$D(S) = S^2 + S\frac{R}{C_1R_1R_4} + \frac{R}{C_1C_2R_1R_2R_3} \quad (5)$$

$$A_{vLP} = 1 + \frac{R_3}{R_4}$$

From (5) ω_O and Q of the proposed circuit is given as

$$\omega_O = \sqrt{\frac{R}{R_1R_2R_3C_1C_2}} \quad Q = R_4\sqrt{\frac{R_1C_1}{RR_2R_3C_2}}$$

$$\frac{V_L}{V_i} = \frac{(R(R_3+R_4)/R_1C_1R_2C_2R_3R_4)}{S^2+S\frac{R}{C_1R_1R_4}+\frac{R}{C_1C_2R_1R_2R_3}} \quad (6)$$

Take the typical values of Passive elements R =R1=R2=R3=R4=1k Ω C1=0.25nF, C2=0.5nF we get,

$$\frac{V_L}{V_i} = \frac{16\ X10^{12}}{S^2+4\ X\ 10^6S+8\ X\ 10^{12}} \quad (7)$$

The nyquist and Bode plot of the above transfer function is plotted with the help of MATLAB.

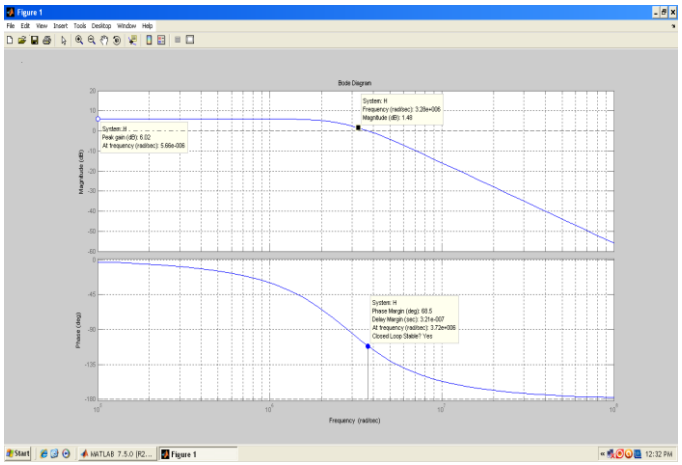

Fig.5 bode plot of the above transfer function

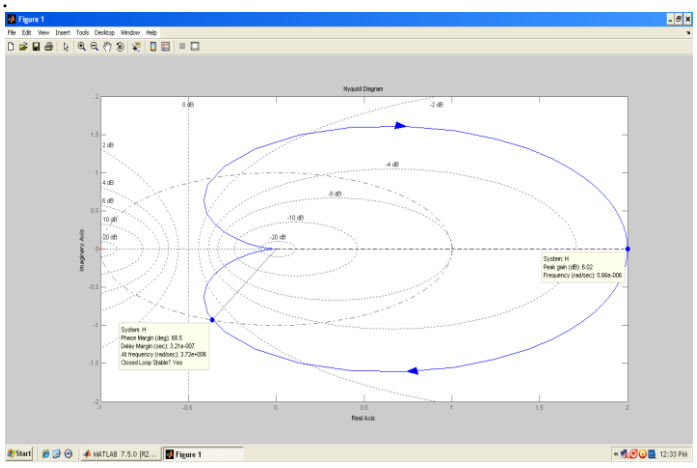

Fig.6 nyquist plot of the above transfer function

Figure 5-6 shown above justify that the transfer function of the system is closed loop stable with phase margin of 68.5 degree.

3.3 Current Mirror

One of the drawbacks of the Current conveyor device is that its trans-conductance (gm) varies often with the I_{bias}. To make the device free from trans-conductance variation we used current mirrors along with the current conveyors which are capable of providing the constant I_{bias} and thereby, making the device free from change of trans-conductance effect. To make the design low power PMOS bulk-driven cascade current mirror (PMOS BDCCM) is used. The topology of the low-voltage PMOS bulk-driven cascade current mirror is shown in Fig.7.

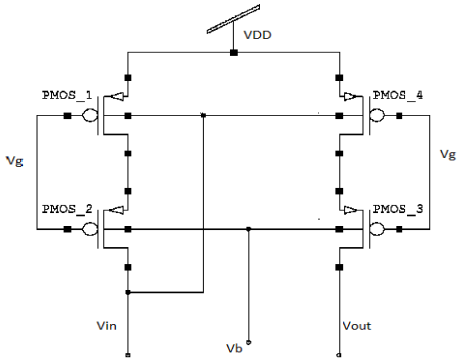

Fig.7. PMOS bulk-driven cascade current mirror

Minimum input output voltage drops may be described as

$$|V_{dd} - V_{in}|_{(min,\ BD)} = V_{SB1} = V_{SD1} + V_{SD2}$$

$$|V_{dd} - V_{out}|_{(min,\ BD)} = V_{SD3} + V_{SD4}$$

$$|V_{dd} - V_{in}|_{(min,\ GD)} = V_{SG} = V_{on} + V_T$$

$$|V_{dd} - V_{out}|_{(min,\ GD)} = 2V_{SD,sat}$$

The input voltage drop of BDCCM is

$$|V_{dd} - V_{in}|_{(min,\ GD)} = V_{SB1} \leq 0.3\ V$$

This is much lower than GDCCM

Consequently M1 and M2 are forced to work in linear region

$V_{SG1} > V_{SG2}$

$I_{SD1} = I_{SD2}$

Forcing $\frac{W_2}{L_2} > \frac{W_1}{L_1}$

$V_{SB} => V_{DD}-V_{SD1}-V_b \leq 0.3$

Hence $V_b \geq V_{DD} - V_{SD1} - 0.3$

for $V_{SB1} = V_{SB3}$ and $V_{SG1} = V_{SG3}$ then $I_{SD1} = I_{SD3}$

If M3 also were in linear region $V_{SD1} = V_{SD4}$

Since the source drain voltage of M4 is unrestricted M4 may work in linear or saturation region obviously minimum output voltage drop BDCCM is lower than GDCCM.The bulk-driven technique may eliminate the limitation of the threshold voltage on the signal channel effectively, thereby reducing the supply voltage required by CMOS analog IC. Compared with the normal gate-driven CMs, the low-voltage BDCCM reduces the input/output voltage drop greatly and has a good input/output resistance characteristic along with a better current driving ability.

4. SIMULATION AND RESULTS

Simulation of a readout interface circuit for water quality monitoring device using ISFET involving DVCC have been carried out on Tanner simulator version 15 for a 70*nm* CMOS process model. In the proposed circuit, following typical values for passive components were chosen Figure 3: $R_1=R_2=R_3=R_4=1K\Omega$, C1=0.25nF, C2=0.5nF.

The proposed readout circuit is modelled using Tanner Tool Version 15 in 70 nm technology and shown in Fig 8.The output response of the device with respect to the time i.e transient analysis shown in Fig. 9 justify the device is highly linear.

The power results obtained when the device is simulated 70nm technology is shown in the appendix at the end of the paper and it is found that the device consumes the average power of 5.613851e-001 watts.

The device is found stable as shown in the mathematical modelling by the analysis of the transfer function and by bode and nyquist plot.

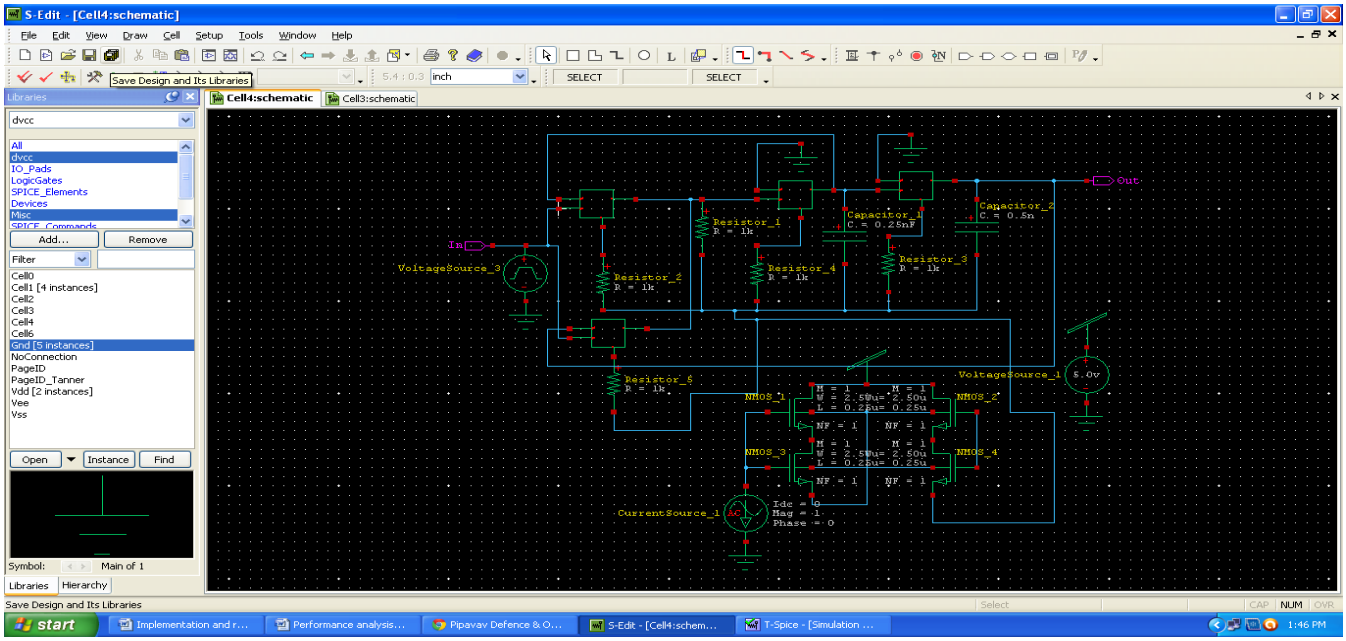

Fig.8 Circuit diagram of proposed scheme

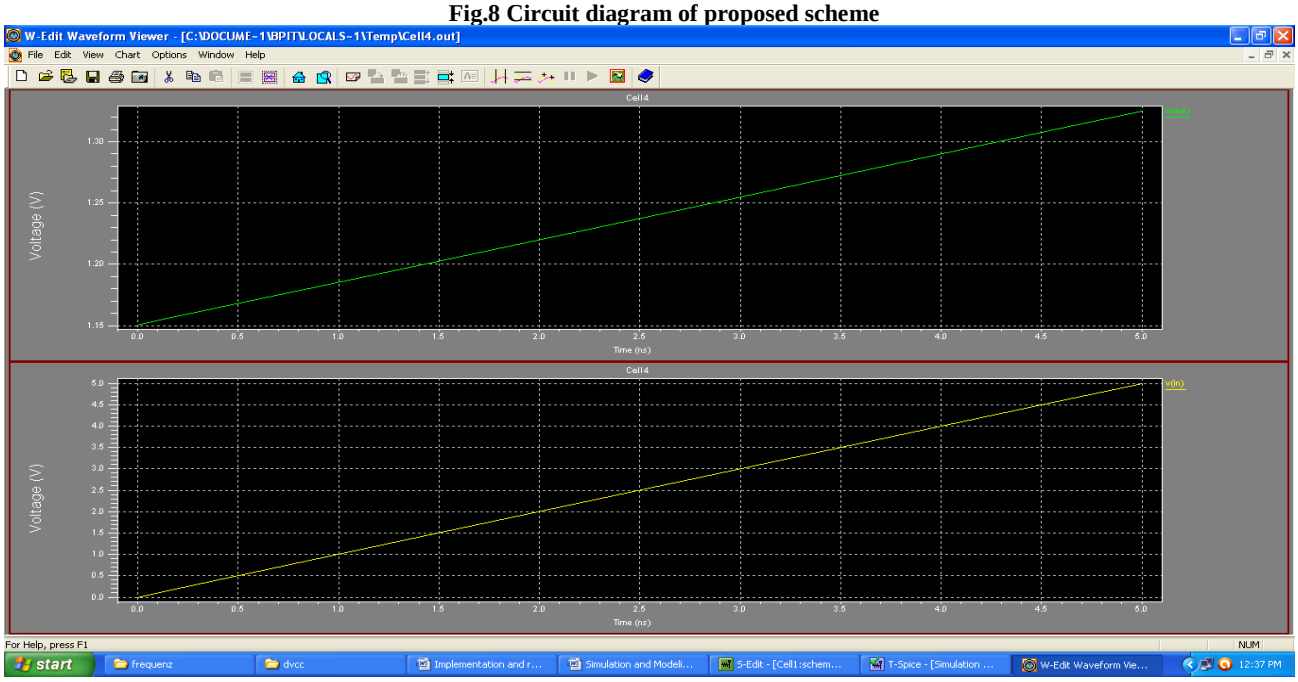

Fig.9 Transient analysis

5. CONCLUSION

In this paper, a new interface readout circuit employing CMOS differential voltage current conveyor (DVCC) is proposed. The second-generation current conveyor introduced is a convenient building block that provides a simplified approach to the design of linear analog systems. The bulk-driven technique used to control the trans-conductance effect of DVCC may eliminate the limitation of the threshold voltage, thereby reducing the supply voltage required by CMOS analog IC. Results of computer simulations and the comparison with experimental data and with transistor-level simulation demonstrated an accuracy of the approach. All the results are in good agreement with the theoretical analysis.

6. FUTURE WORK

This device has a simple architecture, and hence is very suitable for the water quality monitoring application. A significant advantage of this design is that, this circuit is insensitive to the body effect and highly as demonstrated in this circuit. This study can be extended and more improvement in terms of power and size can be achieved at layout level and thus more effective results can be obtained.

Table1: specifications of DVCC

Parameters	DVCC
CMOS technology(nm)	70
Power supply(VDD,GND)	5V-0V
No. of Mosfets	32
Average power dissipation	5.337467e-001 watts
Max power	5.352302e-001
Min power	5.315526e-001
X terminal input resistance	9 ohm

Table2: Transient Analysis

Time<s>	v(in)<V>	v(out)<V>
0.000000e+000	0.0000e+000	1.1508e+000
1.250000e-010	1.2500e-001	1.1550e+000
1.375000e-009	1.3750e+000	1.1983e+000
2.926462e-009	2.9265e+000	1.2525e+000
4.578586e-009	4.5786e+000	1.3102e+000
5.000000e-009	5.0000e+000	1.3253e+000

7. REFERENCES

[1] P.Bergveld,(2000) "Thirty years of ISFETOLOGY what happened in the past 30 years and what may happen in the next 30 years,'Sens.Actuators B, Vol . 88,pp1-20.

[2] A Sedra, K. A Smith (1970). second-generation conveyor and its applications,IEEE Transconductions on Circuit Theory. 1970, CT-17,pp: 132-134.

[3] W Chiu, S I Liu, H W Tsao, J J Chen(1996). CMOS differential difference current conveyors and their applications. IEEE Proceedings G: Circuits Devices Systems, 1996, 43(2),pp:91-96.

[4] H O Elwan, A M Soliman(1997). Novel CMOS differential voltage current conveyor and its applications. IEEE Proceedings G: Circuits Devices Systems, 1997, 144(3),pp: 195-200.

[5] EI-Adawy A A, Soliman A M, Elwan H O(2000). A novel fully differential current conveyor and applications for analog VLSI. IEEE Transaction on circuits and systems-II:Analog and digital signal processing, 2000, 47(4),pp: 306~313.

[6] P.Bergveld (1970), Development of an Ion-sensitive Solid-state Device for Neurophysiologic Measurements, IEEE Trans. Biomed. Eng.pp: 70-71.

[7] Sergio Martinoia and Giuseppe Massobrio (2002), A Behaviour Macro-Model of the ISFET in SPICE, Sensors and Actuators B, pp: 182-189.

[8] B. Palan, F.V.Santos, and J.M.Karam (1999), New ISFET Sensor Interface Circuit for Biomedical Applications, Sensors and Actuators B, pp: 63-68.

[9] Arkadiy Morgenshtein, Liby Sudakov-Boreysha and Uri Dinnar (2004), CMOS Readout Circuitry for ISFET Micro-systems, Sensors and Actuators B, (97):122-131.

[10] Pawan Whig, S. N. Ahmad, (2011) Performance analysis and frequency Compensation Technique for Low Power Water Quality Monitoring Device Using ISFET Sensor. International Journal of Mobile and Adhoc Network. pp 80- 84.

[11] R. E. G. Van Hal, J. C. T. Eijkel and P. Bergveld (1995), A Novel Description of ISFET Sensitivity with the Buffer Capacity and Double-layer Capacitance as Key Parameters, Sensors and Actuators B, pp: 201-205.

[12] Cecilia Jimenez-Jorquera, Jahir Orozoo, Antoni Baldi (2010), ISFET based Microsensors for Environmental Monitoring, Journal of Sensors ISSN 1424-8220, pp: 61-83.

[13] Pawan Whig, S. N. Ahmad, (2011) On the Performance of ISFET-based Device for Water Quality Monitoring, Int'l J. of Communications, Network and System Sciences ISSN 1913-3715, pp:709 -719.

[14] Copp, J.B.; Belia, E.; Hubner, C.; Thron, M.; Vanrolleghem, P.; Rieger, L.; "Towards the automation of water quality monitoring networks ." Automation Science and Engineering (CASE), 2010 IEEE Conference on 2010 , pp: 491 – 496.

Appendix

```
=======================================
*              Synthesis Options Summary          *
=======================================
---- Source Parameters
Input File Name                    :"Cell4.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "Cell4"
Output Format                      : NGC
Target Device                      : xc3s100e-5-vq100
---- Source Options
Top Module Name                    : Cell4
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : YES
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : auto
Automatic Register Balancing       : No
---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 24
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
```

```
Use Clock Enable                    : Yes
Use Synchronous Set                 : Yes
Use Synchronous Reset               : Yes
Pack IO Registers into IOBs         : auto
Equivalent register Removal         : YES
---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Library Search Order                : Cell4.lso
Keep Hierarchy                      : NO
Netlist Hierarchy                   : as_optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
Verilog 2001                        : YES
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=====================================
*                Final Report       *
=====================================
Final Results
RTL Top Level Output File Name      : Cell4.ngr
Top Level Output File Name          : Cell4
Output Format                       : NGC
Optimization Goal                   : Speed
Keep Hierarchy                      : NO

Design Statistics
# IOs                               : 4

Cell Usage :
# BELS                              : 1
# GND                               : 1
# IO Buffers                        : 4
# IBUF                              : 1
# OBUF                              : 3
# Others                            : 105
# Capacitor                         : 2
# NMOS                              : 56
# PMOS                              : 40
# Resistor                          : 5
# Voltage Source                    : 2
=====================================
```

Power result

```
* Device and node counts:
* MOSFETs - 100          MOSFET geometries - 4
*BJTs - 0                JFETs - 0
* MESFETs - 0                Diodes - 0
* Capacitors - 2             Resistors - 5
* Inductors - 0              Mutual inductors - 0
* Transmission lines - 0   Coupled transmission lines - 0
*Voltage sources - 22      Current sources - 1
* VCVS - 0                  VCCS - 0
*CCVS - 0                  CCCS - 0
*SEDIT: Alter=0
*SEDIT: Analysis types DCOP 0 ACMODEL 0 AC 0
TRANSIENT 1 TRANSFER 0 NOISE 0
*WEDIT: .tran   2e-009   5e-009
TRANSIENT ANALYSIS
Time<s>              v(in)<V>           v(out)<V>
 0.000000e+000       0.0000e+000        1.1508e+000
 1.250000e-010       1.2500e-001        1.1550e+000
 1.375000e-009       1.3750e+000        1.1983e+000
 2.926462e-009       2.9265e+000        1.2525e+000
 4.578586e-009       4.5786e+000        1.3102e+000
 5.000000e-009       5.0000e+000         1.3253e+000
* BEGIN NON-GRAPHICAL DATA
Power Results
vdd from time 0 to 5e-009
Average power consumed -> 5.613851e-001 watts
Max power 5.949921e-001 at time 5e-009
Min power 5.242404e-001 at time 0
* END NON-GRAPHICAL DATA
** Parsing                  0.01 seconds
* Setup                     0.02 seconds
* DC operating point        0.01 seconds
* Transient Analysis        0.01 seconds
* Overhead                  0.94 seconds
* ----------------------------------------
* Total                1.00 seconds
* Simulation completed
* End of T-Spice output file
```