Galeorstack- A Novel Leakage Reduction Technique for Low Power VLSI Design

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ABSTRACT
Leakage power consumption plays a significant role in current CMOS technology. International Technology Roadmap for semiconductors reports that leakage power consumption dominates the total chip power consumption as technology advances to nano scale. Most of the battery operated applications such as cell phones, Laptops etc requires a longer battery life, which can be made possible by controlling leakage current flowing through the CMOS gate. This paper presents leakage current mechanisms and different leakage reduction techniques to reduce leakage power consumption. We propose a novel leakage reduction technique named "Galeorstack" which can achieve better leakage reduction by maintaining exact logic state than the other techniques discussed in this paper. The proposed technique has been verified and compared with the other techniques for NOR and EXOR logic circuits and implemented using standard cells of 90nm CMOS process from CADENCE TOOLS. GaleorStack technique would be the best choice to the designer for the low leakage and less delay while achieving exact logic state.

Keywords—
leakage power, low power design, Galeorstack technique.

1. INTRODUCTION
Power consumption has become one of the major concerns of VLSI circuit design with the rapid launching of battery operated applications. VLSI fabrication technology is still in the process of evolution which is leading to smaller feature size and to higher packing density of circuitry on a chip. CMOS technology feature size and threshold voltage have been scaling down for decades in order to achieve high performance. Scaling down the feature size and threshold voltage increases sub threshold leakage current. This leads to short channel effects which increases sub threshold leakage current exponentially [1]. This Sub threshold leakage current ultimately increases the leakage power.

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching and static power is consumed regardless of transistor switching. As CMOS feature size shrinks, static power has become a great challenge for current and future technologies [2].

This paper is organized as follows: Different types of transistor leakage mechanisms are discussed in section 2. Section 3 discusses about leakage reduction techniques. Section 4 gives proposed technique. In section 5 experimental results of various techniques along with Galeorstack technique are presented. Finally section 6 gives conclusions.

2. TRANSISTOR LEAKAGE MECHANISMS
There are six short channel leakage mechanisms in MOS transistors as illustrated in Figure 1. They are :

1. Reverse Bias Junction Leakages (I_1)
2. Subthreshold Leakage (I_2)
3. Gate Oxide Tunneling (I_3)
4. Current due to Injection of Hot Carriers (I_4)
5. Gate Induced Drain Leakage (I_5)
6. Channel Punch Through Current (I_6)

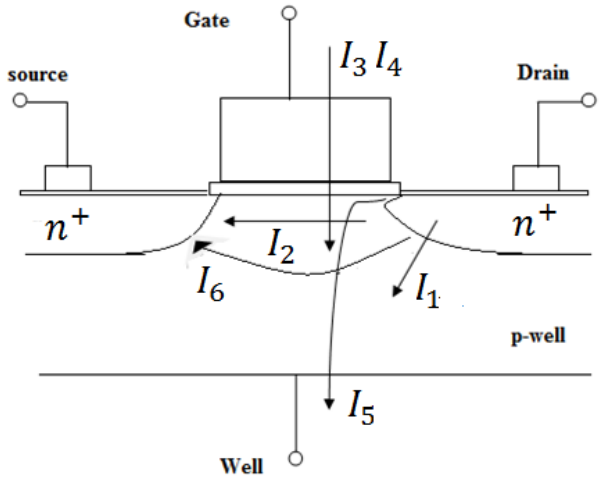

Figure 1. Leakage current mechanisms of MOS transistors

2.1 Reverse Bias Junction Leakages(I_1)
The reverse bias junction leakage is from the source or drain to the substrate through the reverse biased diodes. A reverse biased PN junction leakage has two components. One is minority carrier diffusion/drift near the edge of depletion region, the other is due to electron-hole pair generation in the depletion region of the reverse biased junction [3]. PN junction reverse bias leakage (Irev) is a function of junction area and doping concentration .If both P and N regions are doped heavily, Band To Band Tunneling (BTBT) dominates the PN junction reverse bias leakage.

2.2 Subthreshold Leakage (I_2)
Scaling down the threshold voltage (VTH) increases sub threshold leakage current. Sub threshold conduction current between source and drain in a MOS transistor occurs when gate voltage is less than VTH. Sub threshold leakage is the drain to source current of a transistor operating in the weak inversion region. The drain to source current in a transistor is the combined effect of drift and diffusion mechanisms. In the

strong inversion region, drift current dominates where as in the weak inversion region the sub threshold conduction is dominated by diffusion current. This sub threshold current depends exponentially on both gate to source voltage VGS and threshold voltage VTH. Sub threshold current in a MOS transistor can be expressed as

$$I\,sub = Io\, e^{\left[\frac{V_{GS}-V_{TH}}{nV_T}\right]}\ [1 - e^{-\frac{V_{DS}}{V_T}}\ ]$$

Where Io=(W µo Cox VT2 e 1.8)/L , VT = KT /q is the thermal voltage, VTH is the threshold voltage, VGS is the gate to source voltage, VDS is the drain to source voltage, W and L are the transistor width and length respectively. Cox is the gate oxide capacitance, µo is the carrier mobility and n is the sub threshold swing coefficient.

2.3 Gate Oxide Tunneling Leakage (I_3)

Scaling down the gate oxide thickness results in increase in the field across the oxide. This increase in field causes electron tunneling from gate to substrate and from substrate to gate. This tunneling results in gate oxide tunneling current . The mechanism of tunneling can be divided in to two parts. First is Flower-Nordheim (FN) tunneling and second is direct tunneling. The current density in the FN tunneling is given by [4]

$$J_{FN} = \frac{q^3 E_{ox}^2}{16\,\pi^2\, h\emptyset_{ox}}\ e^{\left(\frac{-4\sqrt{2m^*}\emptyset_{ox}^{1.5}}{3h\,qE_{ox}}\right)}$$

Where Eox is the field across the oxide, Øox is the barrier height for electrons in the conduction band, m* is the effective mass of an electron in the conduction band of silicon, q is the electron charge, h is the Plank's constant. This FN equation is valid for Vox> Øox, where Vox is the voltage drop across the diode. Leakage current due to FN is negligible since short channel devices operating at Vox< Øox. Second mechanism is direct tunneling which dominates in short channel devices. In this case, electron tunnels directly to the gate through the forbidden energy gap of the Sio2 layer. The resulting current is called the gate tunneling leakage current.The current density of the direct tunneling is given by[4]

$$J_{DT} = AE_{ox}^2 \exp\left[-B\left[1-\left[1-\frac{V_{ox}}{\emptyset_{ox}}\right]^{3/2}\right]E_{ox}^{-1}\right]$$

$$A = \frac{q^3}{16\pi^2 h\emptyset_{ox}}\ ;\ B = \frac{4\sqrt{2m^*}}{3hq}\ \emptyset_{ox}^{3/2}$$

Where Vox< Øox. Eox is the field across the oxide, Øox is the barrier height for electrons in the conduction band, m* is the effective mass of an electron in the conduction band, q is the electron charge, h is the Plank's constant.

2.4 Current due to Injection of Hot Carriers (I4)

In short channel devices, due to high electric field near the Si-Sio2 interface, electrons or holes can gain sufficient energy from the electric field to cross the interface potential barrier and enter in to the oxide layer. This effect is known as hot carrier injection. As electrons have lesser effective mass than holes, electrons can inject more from Si to Sio2 interface. Scaling down the supply voltage with the device dimensions is one possible way of controlling this leakage [4].

2.5 Gate Induced Drain Leakage (I_5)

Gate Induced Drain Leakage(GIDL) is due to high field effect in the drain junction of MOS transistor [5]. For a MOS transistor with a drain potential, band bending in the drain causes carrier generation through avalanche multiplication and band to band tunneling. As the holes are rapidly swept out to the substrate a deep depletion condition is created. At the same time electrons collected by the drain results in GIDL current. Transistor scaling has led to increasingly steep halo implants, where the substrate doping at the junction interfaces is increased, while the channel doping is low. This is mainly to control punch- through and drain induced barrier lowering with minimal effect on the mobility of the carriers in the channel. The steep doping profile that results at the drain edge increases the band-to-band tunneling currents there, especially as drain bulk voltage (Vdb) is increased. Thinner oxide and higher supply voltage increases GIDL current. GIDL can be reduced by rolling the doping concentration in the drain.

2.6 Channel Punch Through Current (I_6)

In short channel devices, the depletion regions at the drain-substrate and source-substrate injections extend in to the channel. When length of the channel is reduced with constant doping, the separation between the depletion edges decreases. An increase in reverse bias across the junctions also makes the depletion region edges to be nearer to each other. All these effects leads to the merging of the depletion regions, which is known as punch through.

3.LEAKAGEREDUCTION TECHNIQUES

3.1 Base Case

Base case is the conventional CMOS technique represented with pull up and pull down networks. Desired Boolean function can be implemented using this base case approach with few transistors in pull-up and pull-down networks. Figure 2 shows inverter circuit using base case.

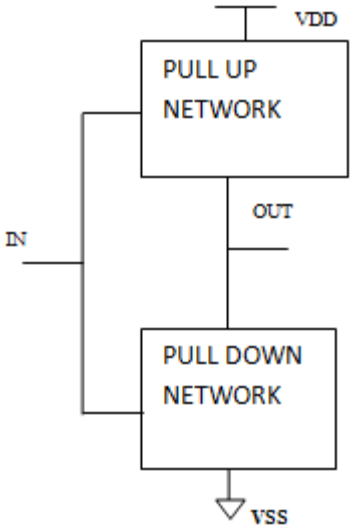

Figure 2. Base Case inverter circuit

3.2 Forced Stack Technique

Another technique to reduce leakage current is Forced stack technique in which each transistor is replaced by two half size transistors. As shown in Figure 3, both PMOS & NMOS Transistors in pull-up and pull-down networks are replaced as two half size transistors. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly.

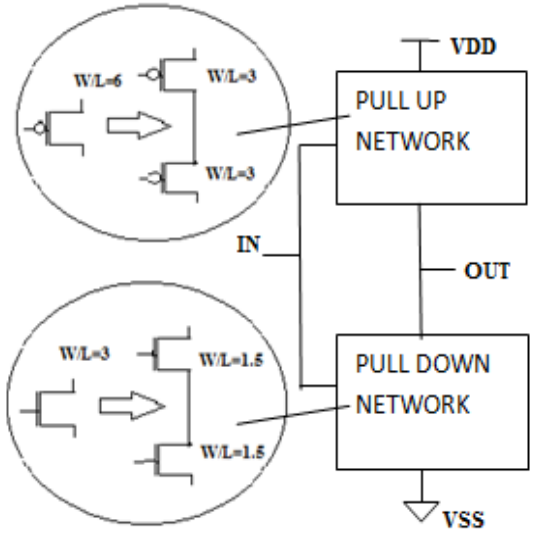

Figure 3. Forced stack technique applied to inverter circuit

3.3 Galeor Technique

In the Galeor technique two gated leakage transistors are inserted between pull-up and pull-down networks of CMOS circuit. Gated leakage NMOS transistor is placed between output and pull-up circuit and a gated leakage PMOS transistor is placed between output and pull-down circuitry. The gates of these additional transistors are controlled by the drain voltages. Gated Leakage transistors cause increase in resistance of the path from V_{dd} to ground since one of the leakage transistors is always near its cutoff region, thereby decreasing leakage current. Even though Galeor technique reduces the leakage current to some extent compared with the above techniques, it suffers from a significant problem of low voltage swing. In this technique the logic low level is very much higher than 0 volts and logic high level is much lower than V_{dd}, which makes voltage swing to be lowered. This reduced voltage swing increases the propagation delay through the circuit. Figure 4 shows the Galeor technique applied to CMOS inverter circuit.

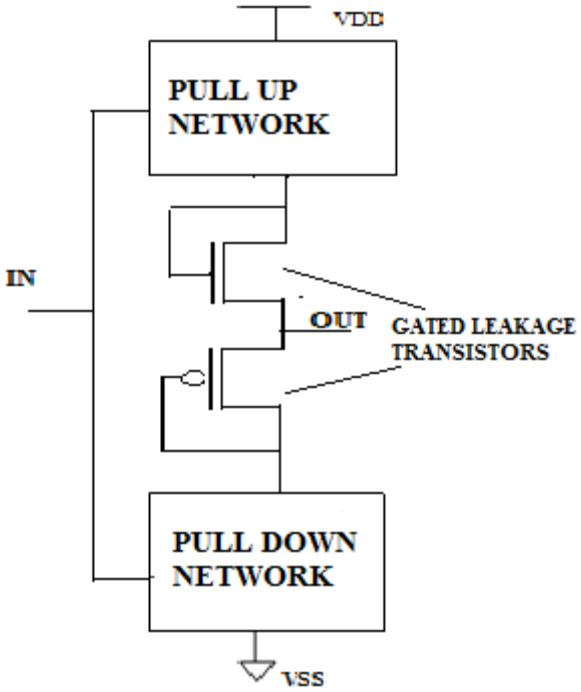

Figure 4. Galeor technique applied to inverter circuit

4. PROPOSED METHOD

4.1 GaleorStack Technique

In this section we introduce a new leakage current reduction technique for CMOS circuit design. Figure 5 shows Galeorstack technique which combines the Galeor and Forced stack techniques. As it combines the features of the above mentioned techniques, two gated leakage transistors are introduced between pull up and pull down networks with high threshold voltage, then stack effect is added to pull up and pull down networks by dividing each transistor in to half size transistors (i.e., W/2). As more stack effect can be introduced, due to high threshold voltage gated leakage transistors and half size stacked transistors, ultimately more leakage current reduction can be achieved with the proposed technique. Though the leakage reduction techniques discussed in section 3 could achieve leakage current reduction with the penalty of delay but the proposed technique can achieve more leakage current reduction without delay penalty.

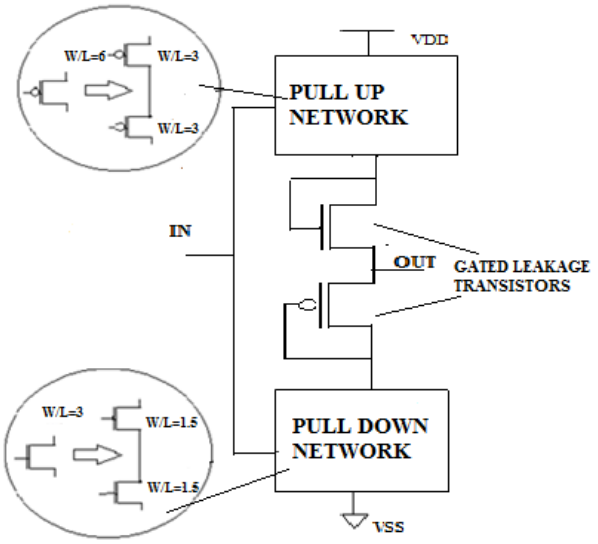

Figure 5. Galeorstack technique applied to inverter circuit

5. EXPERIMENTAL RESULTS

Two input NOR and two input EX-OR gates are selected to compare the techniques discussed in section 3 and 4. Figure 6, 7 and 8 shows Base case, Forced stack and Galeor techniques respectively applied to the two input NOR gate. Figure 9 shows the Galeorstack technique applied to 2 input NOR gate. Table 1 gives the tabular data showing static and dynamic powers along with the propagation delay for the various techniques. Similarly, Figure 10, 11, 12 and 13 shows the various techniques applied to two input EX-OR gate and Table 2 gives the summary of results showing static and dynamic powers along with the delay. From Table 1 and 2 we can observe how less leakage power consumption can be achieved with the proposed Galeorstack technique compared with the other mentioned techniques. In addition, the delay also can be reduced to very much extent which improves the speed of the circuit tremendously unlike the delay penalty in the other mentioned techniques. All the techniques are implemented with the standard cell library of TSMC 0.09um using CADENCE TOOLS.

6. CONCLUSIONS

Scaling down the CMOS technology feature size and threshold voltage has increased leakage power tremendously. In this paper we have presented a novel technique called Galeorstack which can achieve more leakage current reduction without penalty for the delay. The implementation of the other techniques like base case, forced stack and Galeor techniques are also presented. Forced stack and Galeor techniques can also achieve good leakage current reduction with the delay penalty. When the speed is not the criteria, then definitely designers can choose the other techniques like stack and Galeor. From the experimental results shown, the proposed Galeorstack technique is best in terms of speed and leakage power consumption.

7. ACKNOWLEDGMENTS

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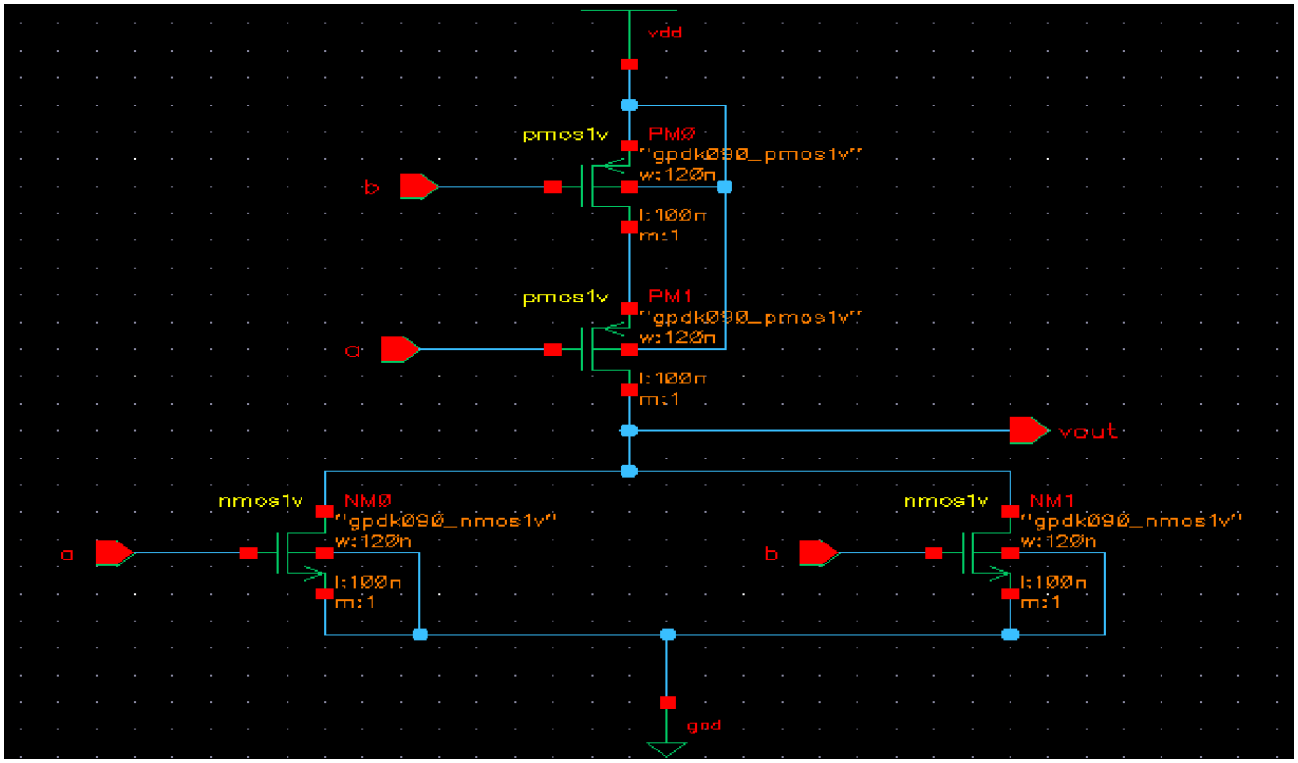

Figure 6. Schematic of 2 input NOR Base Circuit

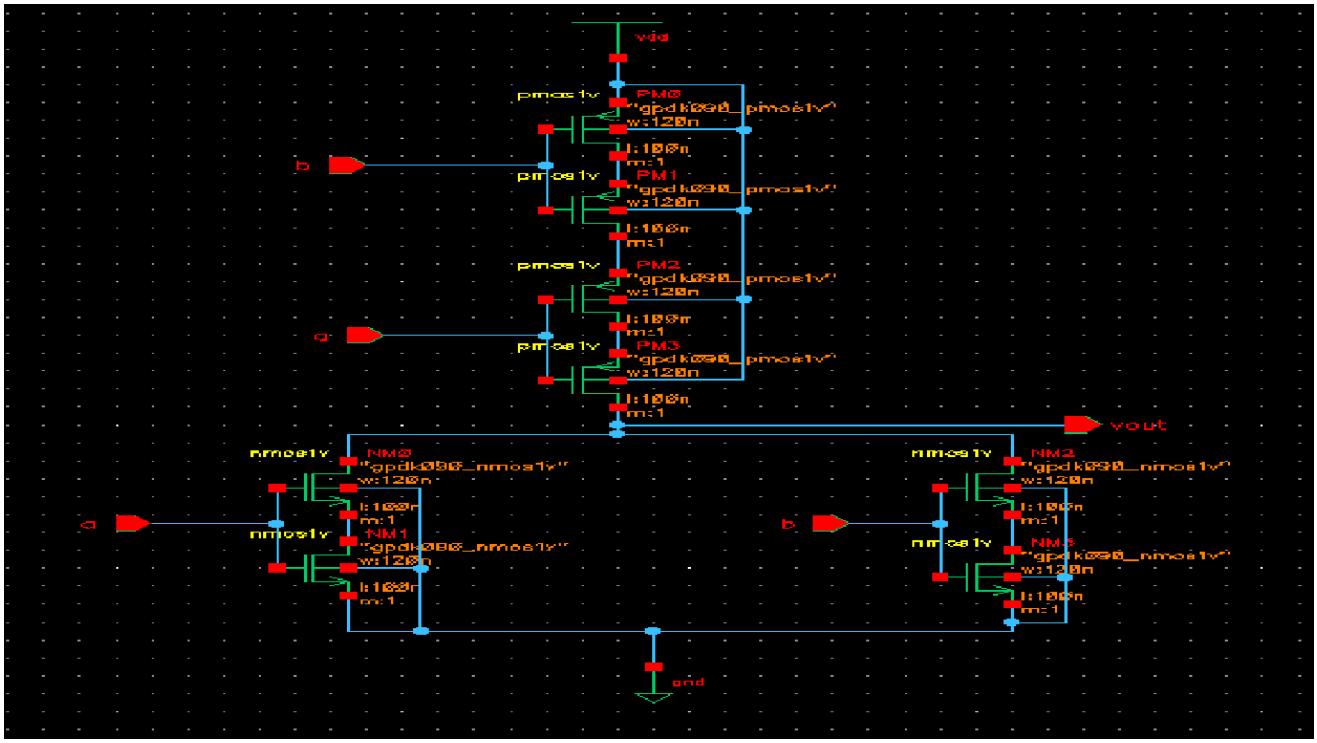

Figure 7. Schematic of 2 input NOR gate applied with Forced Stack

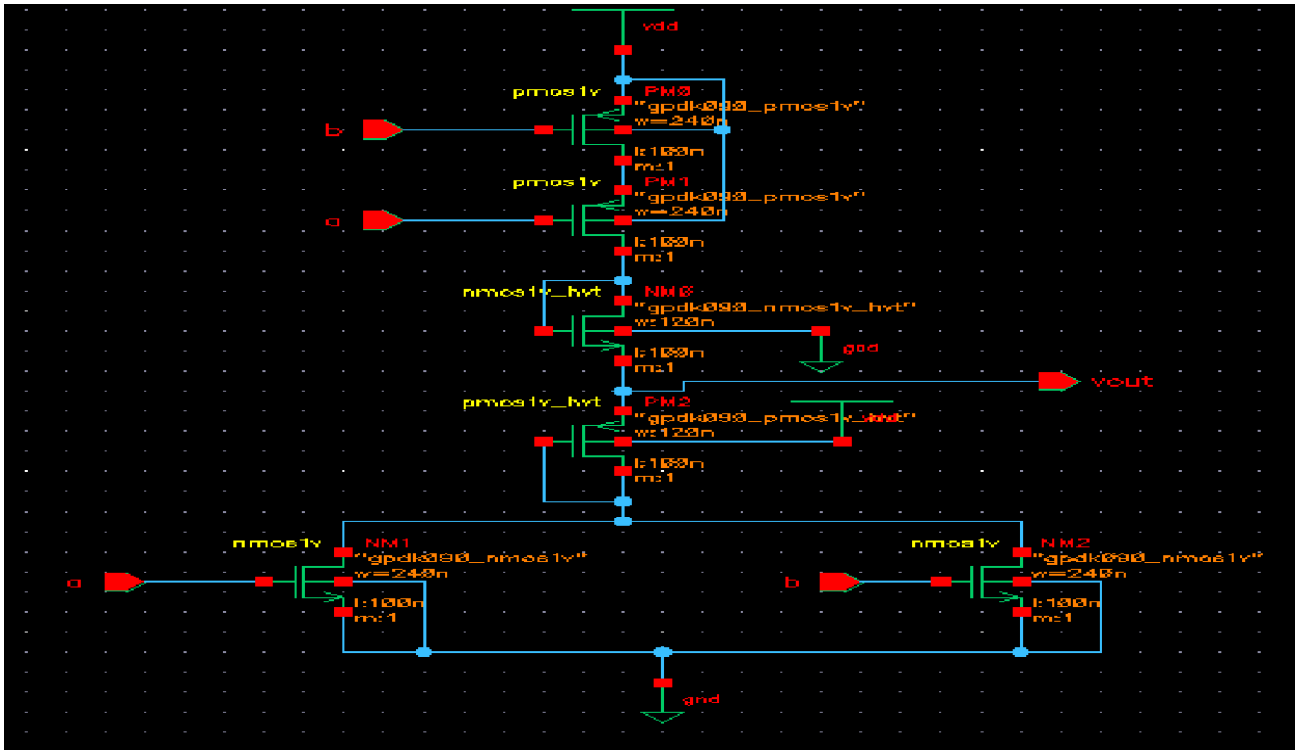

Figure 8. Schematic of 2 input NOR gate applied with Galeor Technique

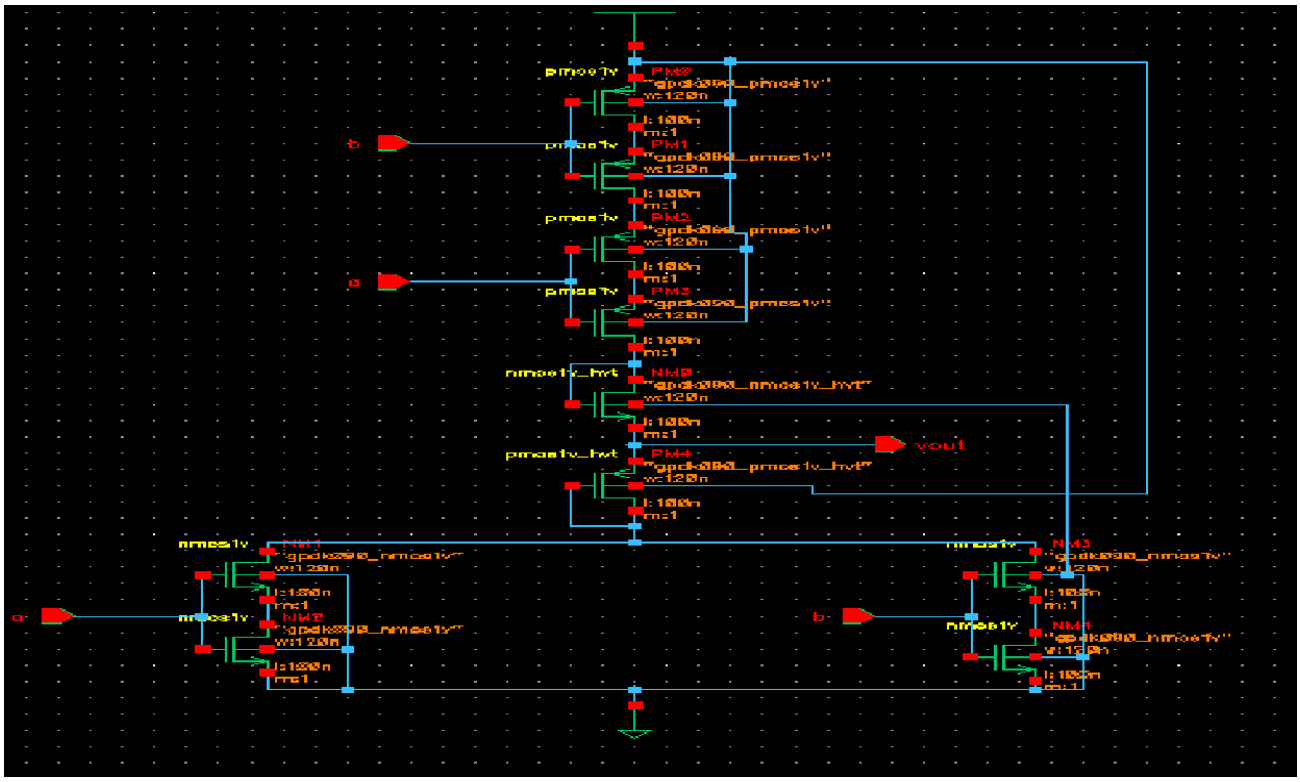

Figure 9. Schematic of 2 input NOR gate applied with GaleorStack

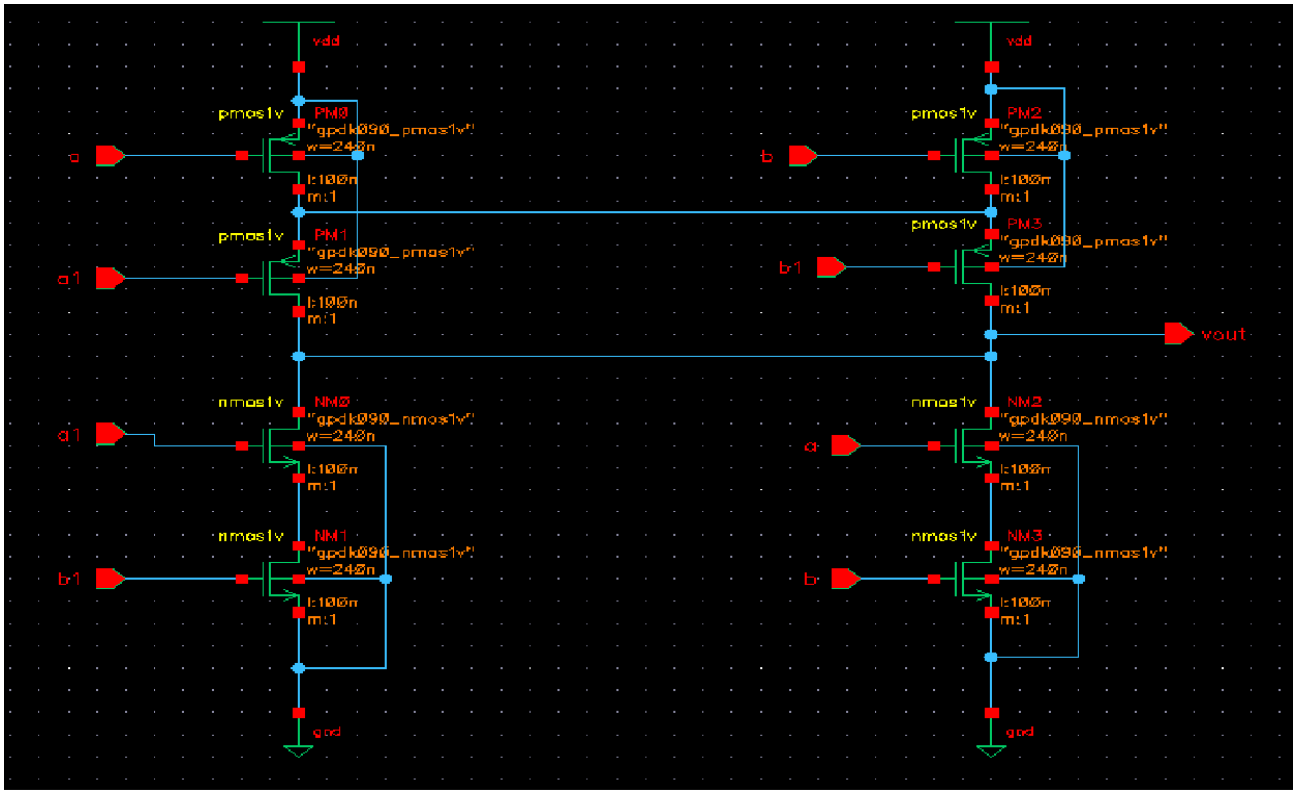

Figure 10. Schematic of 2 input EX-OR gate Base circuit

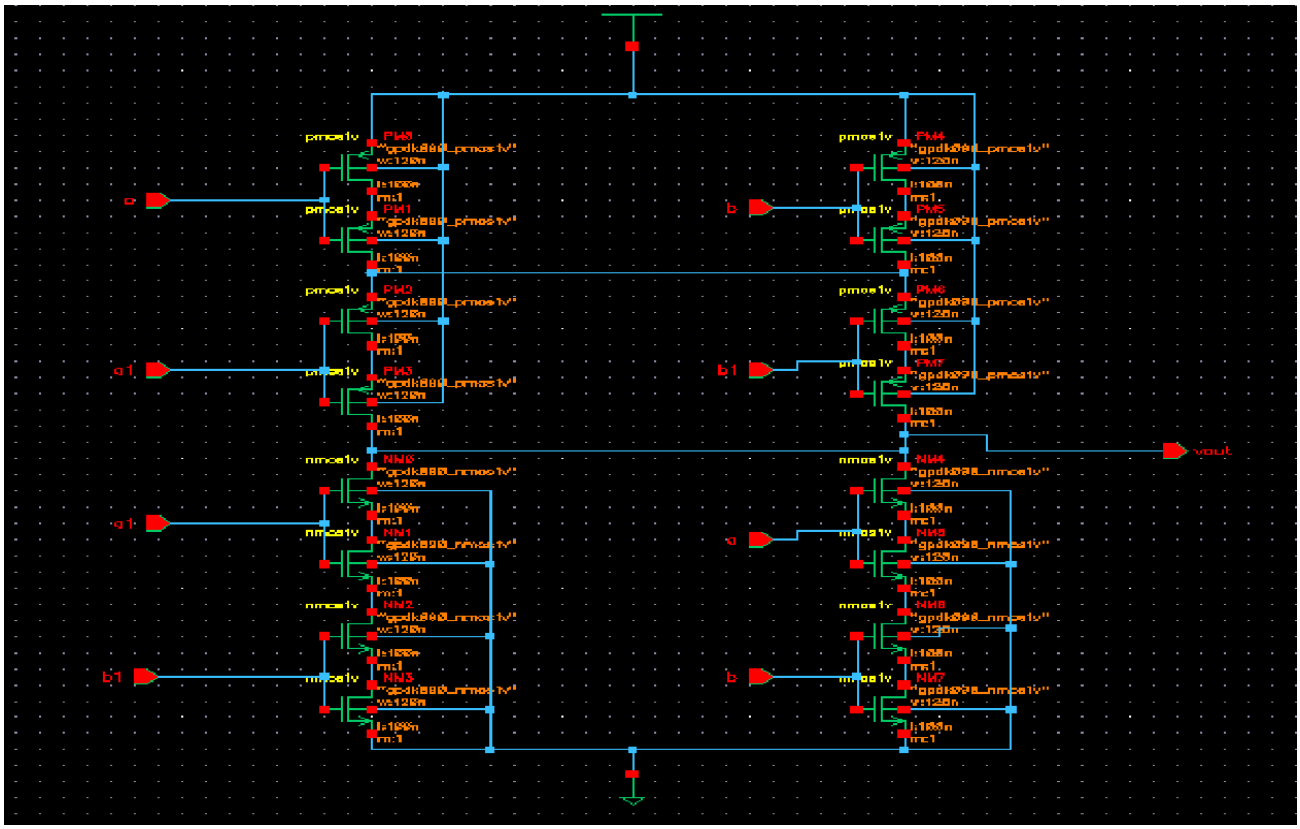

Figure 11. Schematic of 2 input EX-OR gate applied with Forced Stack Technique

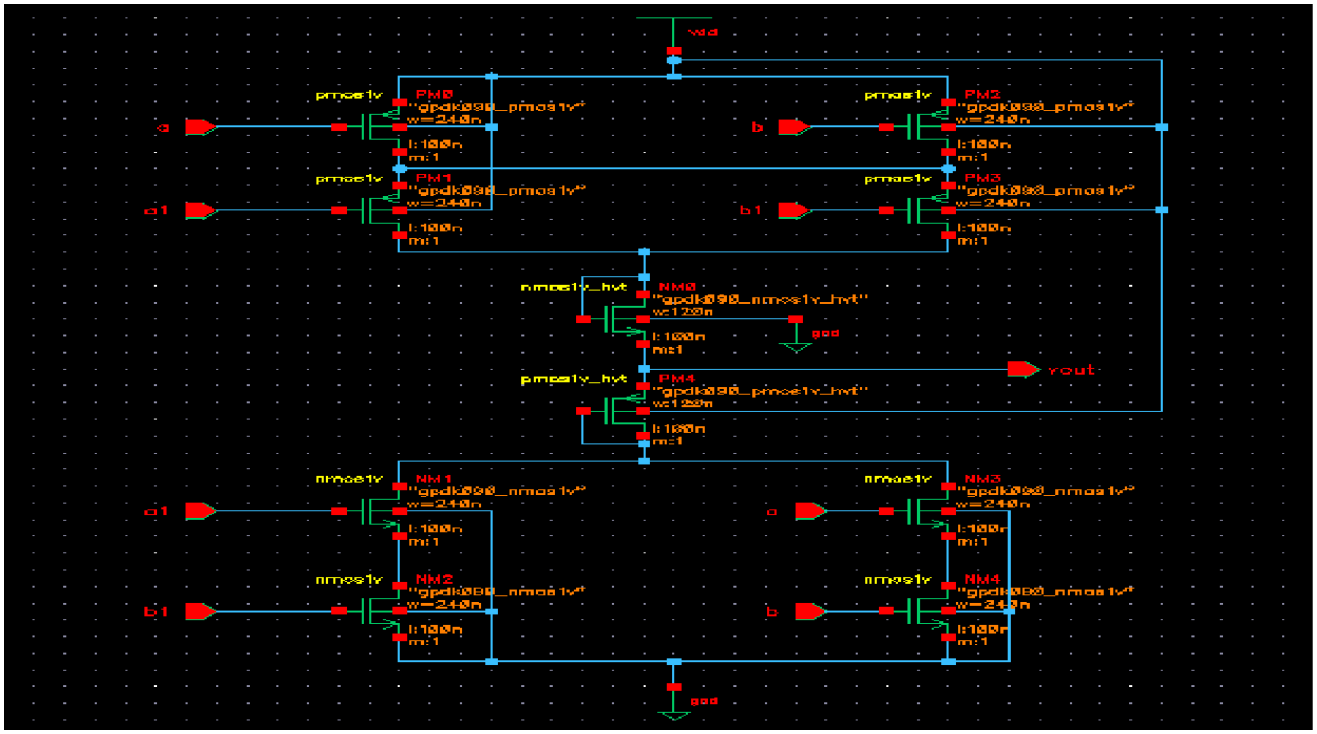

Figure 12. Schematic of 2 input EX-OR gate applied with Galeor Technique

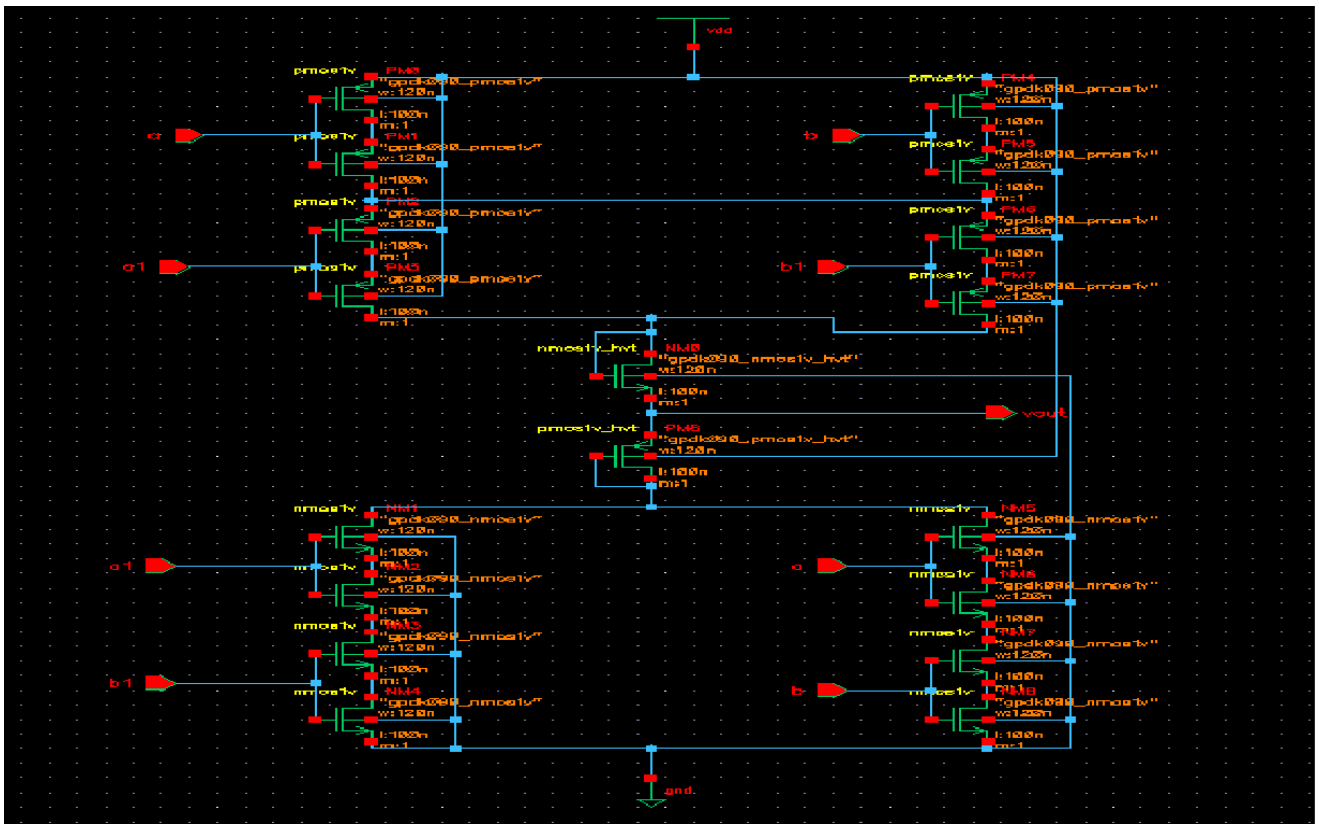

Figure 13. Schematic of 2 input EX-OR gate applied with GaleorStack Technique

Table 1. Summary of 2 input NOR gate

Technique	Average power (w)	Static power(w)	Dynamic power(w)	Delay(s)
BASE CASE	**3.659838662e-06**	**8.393p**	**3.659830e-06**	**2.54298e-10**
STACK	**7.09612151e-07**	**1.549p**	**7.096106e-07**	**1.95984e-10**
GALEOR	**9.03407165e-07**	**15.9p**	**9.033912e-07**	**1.70709e-10**
GALEORSTACK	**4.12667655e-07**	**1.728p**	**4.126659e-07**	**7.73276e-11**

Table 2. Summary of 2 input EXOR gate

Technique	Average power (w)	Static power(w)	Dynamic power(w)	Delay(s)
BASE CASE	**6.8000690e-06**	**34.7p**	**6.80004e-06**	**2.01491e-08**
STACK	**1.474386e-06**	**6.084p**	**1.47437e-06**	**2.024913-08**
GALEOR	**1.7650766e-06**	**27.96p**	**1.76504e-06**	**2.24178e-10**
GALEOR STACK	**8.8380750e-07**	**6.61p**	**8.38068e-07**	**9.16559e-11**