# DVCC-based Electronically Tunable First-Order Current-mode Filters

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## ABSTRACT

The advent of differential voltage current conveyor (DVCC) has opened up new avenues in analog circuit design. In the present work, a DVCC has been employed to design current-mode first-order continuous-time analog filters. Parameter tunability is achieved by the use of a two-MOSFET electronic resistor which exhibits variation in resistance in accordance with a control voltage. The proposed circuits are amenable for monolithic integration by virtue of the fact that only MOSFETs and grounded capacitors are utilized. Circuit simulations using PSPICE yielded promising results.

## General Terms

Differential Voltage Current Conveyor, Electronically Tunable Circuits

## Keywords

Differential Voltage Current Conveyor, DVCC, Electronic Filters, Electronically Tunable Circuits, MOSFET-based Resistor.

## 1. INTRODUCTION

The continuous-time analog filter is a ubiquitous circuit component in a vast variety of applications including, butnot limited to, noise rejection & signal separation in industrial and measurement circuits, feedback of phase & amplitudecontrol in servo loops, smoothing of digitally generated analog signals, audio signal shaping & sound enhancement, channel separation & signal enhancement in communication electronics [1]–[9].

Active filter design generally employs one (or more) active building block and passive components like capacitors and resistors; inductors being avoided due to their incompatibility with the standard CMOS fabrication process. The active element may be one of the following: operational amplifier, second generation current conveyor (CCII) [5], operational trans-conductance resistance amplifier (OTRA) [4], fully differential current conveyor (FDCCII) [1], third generation current conveyor (CCIII) [7], differential voltage current conveyor(DVCC) [2], [3], [9], etc. Circuit design using each of these building blocks has its own associated advantages and limitations with the DVCC offering the highest amount of flexibility and simplicity in analog electronic circuit design.

Current-mode signal processing has received considerable research attention in the recent past due to associated advantages like extended bandwidth, higher dynamic range, suitability of operation in reduced power supply environments, possibility of simpler circuit realizations and low power consumption[2], [6]–[9]. In this paper, DVCC based implementations for current-mode first-order high pass filter (HPF) and low pass filter (LPF) are presented. A MOSFET-based circuit for emulating a grounded resistor is employed to ensure electronic tunability [10].

This paper is organized as follows. A brief review of existing analog filter design approaches appears in Section–II. Section–III contains an explanation of the operation of the DVCC and a MOSFET-based electronically tunable resistor. Section–IV deals with details of the proposed first-order filter configurations along with the design equations. Section–V presents the results of computer simulations of the proposed circuits using the PSPICE program. Non-ideal analysis and discussion on VLSI implementation of the proposed circuit appears in section–VI. Some conclusive remarks appear in section–VII.

## 2. EXISTING METHODS

Analog filter design using a variety of active building blocks has been an active area of research for the past two decades. Operational amplifier was the active element of choice during the earlier stages of development. Later, the advent of current conveyors signaled the era of mixed-mode and current-mode signal processing. Since there has been a significant amount of technical literature available on the subject, it is not possible to attempt a thorough review of all the related works. Therefore, a survey of some of the recently published works is presented in this section.

The DVCC was introduced by Elwan & Soliman and its application in continuous-time filters was also discussed [5]. Adawy, Soliman & Elwan later proposed another analog building block *viz*. the Fully Differential Current Conveyor (FDCCII) and several applications in electronic filters were also presented [3].One significant feature of the filters designed using FDCCII was the possibility of obtaining fully differential processing. Cakir, Cam & Cicekoglu put forward an all pass configuration employing a single OTRA [4]. Minaei & Ibrahim employed the DVCC for implementing a general topology for obtaining current-mode first-order APF [6]. A third-generation current conveyor (CCIII) was utilized to yield a trans-admittance type first-order filter [7]. Maheshwari reported current-mode all-pass, high-pass and low-pass filter sections based on DVCC, which forms the background for the present work. [9]. Minaei & Ibrahim presented a mixed-mode universal filter based on the KHN-biquad topology employing DVCCs [8]. Another voltage mode all-pass filter using DVCC as the building block is attributed to Minaei & Yuce [2]. More recently, Maheshwari *et al*. used the FDCCII to realize cascadable all-pass/notch filters employing only grounded capacitors as the passive elements [1].

## 3. DVCC & ELECTRONIC RESISTOR

Since its introduction by Sedra & Smith in 1970, the Current Conveyor (CCII) has proved to be a very versatile analog

building block that can be used to implement a wide variety of analog signal processing applications.

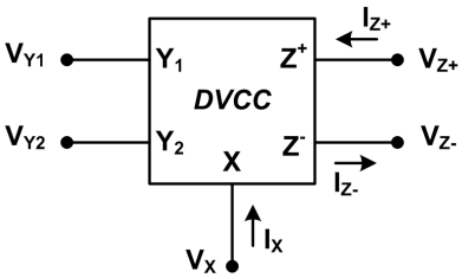


**Fig. 1. Electrical symbol of DVCC**

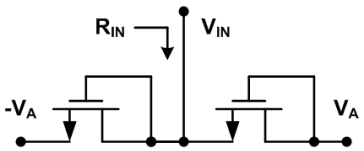


**Fig.2.: Voltage controlled MOSFET-based grounded resistor**

However, when it comes to applications demanding differential or floating inputs like impedance converters and quadrature oscillators which require two high-input impedance terminals, a single CCIIis not generally sufficient. To overcome this shortcoming, the Differential Voltage Current Conveyor (DVCC) was first introduced by Pal, and later developed by Elwan & Soliman[5].The DVCC, shown in Figure 1,is essentially a 5-terminalblock defined by the following relations:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z_+} \\ I_{Z_-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z_+} \\ V_{Z_-} \end{bmatrix} \quad (1)$$

While the X terminal voltage follows the voltage difference of terminals Y1 and Y2, a current injected at the X terminal is being replicated to the Z+ (same phase) and Z– (inverted phase) terminals. An ideal DVCC would exhibit zero input resistance at X terminal and infinite resistance at all the remaining terminals.

A MOSFET-based circuit to emulate the functionality of a grounded resistor is presented next. As can be seen from Figure 2, two transistors can be connected in a manner such that the control voltage ($V_A$) governs the resistance offered at the output terminal shown. The resistance $R_{IN}$, as shown in Figure 2 is given by:

$$R_{IN} = \frac{L}{2\mu_n C_{ox} W(V_A - V_T)} \quad (2)$$

where $\mu_n$ is the electron mobility in the MOSFET, $C_{ox}$ is the gate capacitance per unit area, Wand L are the width and length of the transistor respectively, $V_T$ is the threshold voltage of the NMOS transistors and $V_A$ is the control voltage.

## 4. PROPOSEDCIRCUITS

This section presents the proposed DVCC-based current-mode first-order continuous-time filters with electronic control of filter parameters like gain and cut-off frequency. Figure 3shows a current-mode high-pass filter employing one DVCC, one grounded capacitor and one grounded resistor (realized using MOSFETs).

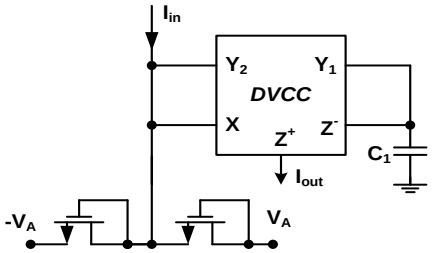


**Fig. 3:Proposed DVCC-based current-mode electronically tunable HPF**

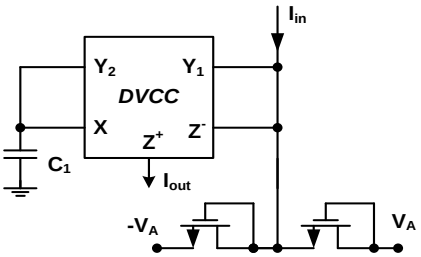


**Fig. 4:Proposed DVCC-based current-mode electronically tunable LPF**

The input is fed at the node marked $I_{in}$ and the output is available at the Z+ terminal of the DVCC. The filter parameters can be controlled by varying the control voltage $V_A$. Similarly, Figure 4 presents a first-order realization of the proposed DVCC-based first-order low-pass filter. Figure. 5and Figure 6 further demonstrate that slight modifications in the HPF and LPF circuit presented earlier result in inverting HPF and LPF functionalities. Routine analysis of the proposed circuits for obtaining the current-mode transfer functions for the filters yields the entries presented in Table 1.

**Table 1. Current-mode transfer functions for the various first order filters**

| Filter Type | Current-mode Transfer Function |
|---|---|
| **LPF:** | $\frac{I_{OUT}}{I_{IN}} = \frac{1/2CR_{IN}}{s+1/2CR_{IN}}$ (3) |
| **HPF:** | $\frac{I_{OUT}}{I_{IN}} = \frac{s}{s+2/CR_{IN}}$ (4) |
| **Inverting HPF:** | $\frac{I_{OUT}}{I_{IN}} = -\frac{s}{s+1/2CR_{IN}}$ (5) |
| **Inverting LPF:** | $\frac{I_{OUT}}{I_{IN}} = -\frac{2/CR_{IN}}{s+1/2CR_{IN}}$ (6) |

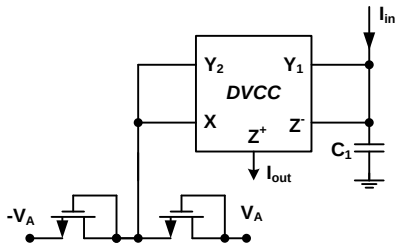


**Fig. 5. Proposed DVCC-based current-mode electronically tunable inverting HPF**

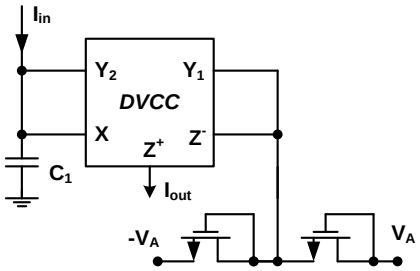


**Fig. 6. Proposed DVCC-based current-mode electronically tunable inverting LPF**

## 5. SIMULATION RESULTS

The proposed circuits were simulated in PSPICE to ensure that the expected functionality is indeed obtained. Figure 7 shows a plot depicting the variation of resistance with control voltage which signifies a fairly linear variation of resistance. Two different values of the transistor width, 1.25 µm and 2.5µm were considered keeping the channel length fixed at 0.5µm. The control voltage is varied from 1V to 2.5 Vin increments of 0.1 V. For the proposed filters, the control voltage was varied from 1V to 2.5 V keeping the value of the capacitor at 1 nF. The CMOS realization of DVCC shown in Figure 8 was utilized [9].

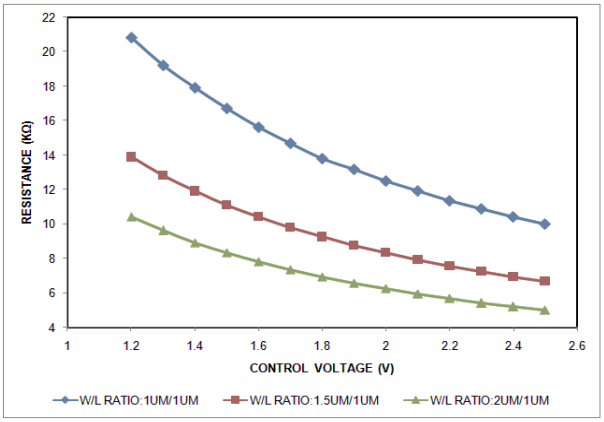


**Fig. 7: Voltage control of resistance**

The resultant waveforms as obtained for the high-pass and low-pass filters are shown in Figure 9 and Figure 10 from where it can be seen that the filter responses vary with changing control voltage. The variation in cut-off frequencies for the filters is shown separately in Figure 11 and Figure 12, from where linear control of cut-off frequency with control voltage is exhibited. For the high-pass filter, the cut-off frequency with control voltage is exhibited. For the high-pass filter, the cut-off frequency is found to vary from 280 KHz to 450KHz. by increasing the control voltage from 1 V to 2.5 V. Similarly for the LPF, same variation in the control voltage resulted in cutoff frequency changing from 16 KHz to 44 KHz.

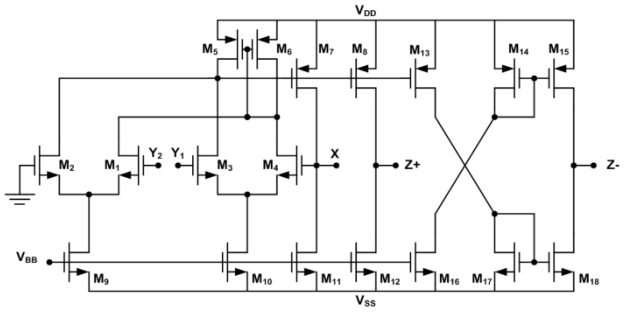


**Fig. 8: CMOS realization of DVCC**

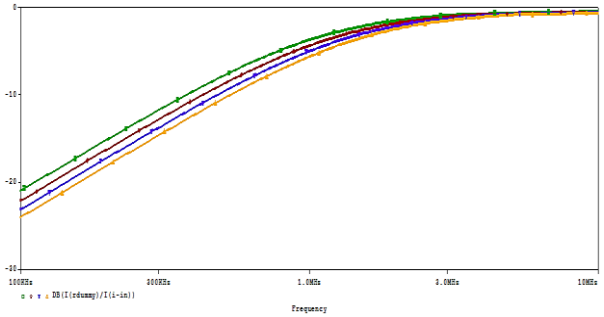


**Fig.9: PSPICE simulation result for the proposed electronically tunable current-mode HPF**

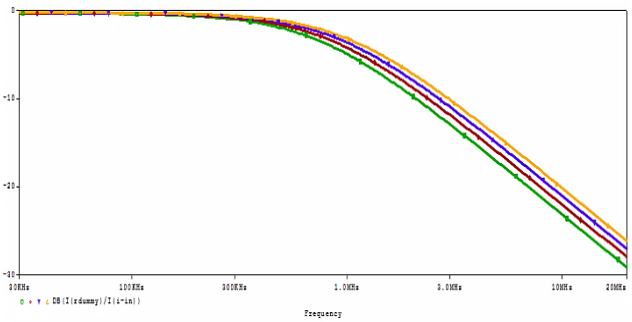


**Fig.10: PSPICE simulation result for the proposed electronically tunable current-mode LPF**

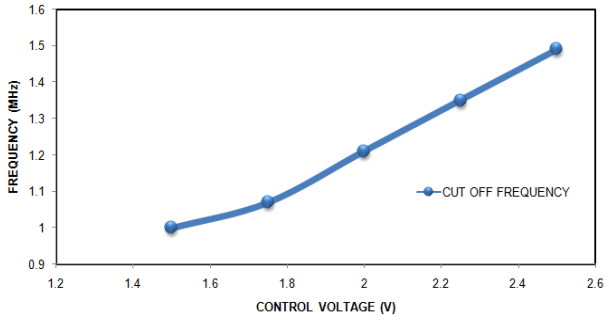


**Fig. 11: Variation of cut-off frequency of the proposed**

**HPF with control voltage**

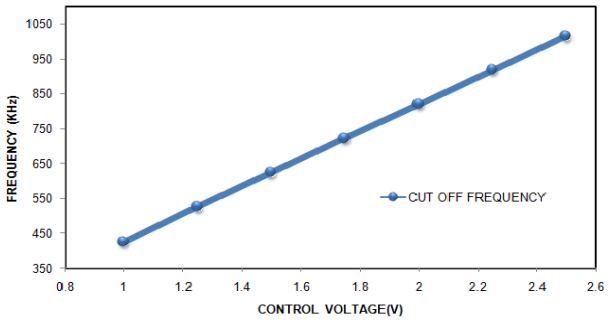


**Fig. 12: Variation of cut-off frequency of the proposed LPF with control voltage**

## 6. DISCUSSION

Actual monolithic integrated circuit implementation issues of the proposed circuit are discussed in this section. The analysis presented in the previous section assumed that the DVCC is ideal, and therefore, analysis is required to determine how deviations from this assumption affect the performance of the circuit. The realistic, non-ideal defining equations for the DVCC are given as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z_+} \\ I_{Z_-} \end{bmatrix} = \begin{bmatrix} 0 & \beta_1 - \beta_2 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_1 & 0 & 0 & 0 \\ -\alpha_2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z_+} \\ V_{Z_-} \end{bmatrix} \quad (7)$$

The non-ideal current-mode transfer functions corresponding to (3), (4), (5) and (6) can be given as:

**LPF:**
$$\frac{I_{OUT}}{I_{IN}} = \frac{\beta_1/(1+\beta_2)CR_{IN}}{s + \beta_1\alpha_2/(1+\beta_2)CR_{IN}} \quad (8)$$

**HPF:**
$$\frac{I_{OUT}}{I_{IN}} = \frac{1}{\alpha_2}\left[\frac{s}{s + (1+\beta_2)/\beta_1\alpha_2 CR_{IN}}\right] \quad (9)$$

**Inv. HPF:**
$$\frac{I_{OUT}}{I_{IN}} = -\frac{s}{s + \beta_1\alpha_2/(1+\beta_2)CR_{IN}} \quad (10)$$

**Inv. LPF:**
$$\frac{I_{OUT}}{I_{IN}} = -\frac{(1+\beta_2)/\beta_1\alpha_2 CR_{IN}}{s + 1/(1+\beta_2)CR_{IN}} \quad (11)$$

Furthermore, all the proposed circuits are compatible with con-temporary CMOS processes as only MOSFETs and grounded capacitors are employed. The absence of passive resistors (floating and/or grounded) and floating capacitors serves to lower the chip area and reduce fabrication costs.

## 7. CONCLUSION

In this paper, four new electronically controllable first-order current-mode filters based on DVCC were presented. Tunability by means of a control voltage was achieved by employing a MOSFET-based implementation of a grounded passive resistor. Standard low-pass and high-pass filter functions were obtained, besides inverting low-pass and high-pass first-order transfer functions which were readily available with small modifications. PSPICE simulations were carried out to ascertain the working of the proposed filters and the results are found to match with the theoretical results.

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