Application of Analog IC Testing Circuit

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ABSTRACT

This paper presents application of Neural classifier with High pass filter(HPF) to examine its own functional health, to speed up test time and to facilitate fault diagnosis Here we presents an application to insert a built in test block to test any complicated analog circuit in terms of performance while considering tolerance factor. Testing block which is to be added in the chip contains Synapse, Common mode canceller and current to voltage converter along with that a simple operational High pass filter (HPF) is taken as a CUT.

Keywords

Synapse, Neuron, Neural Classifier and Common Mode Canceller.

1. INTRODUCTION

The focus of this paper is the neural classifier, which is a component of BIST The neural classifier compares the result of test stimulus and applied stimulus and is classified as a valid or invalid code-word pointing to a functional or faulty operation respectively. With help of very simple HPF as analog circuit to future neural classifier role is described.

2. HIGH PASS FILTER (HPF)

A simple HPF (High pass filter) is shown in Fig.1. Fig.2 shows characteristics of two high pass filter which is having same cut of frequency but output voltage slightly various from actual voltage by +0.6V or -0.6V. To test analog circuits required circuits considering tolerance factor of +0.6 or -0.6 as no fault. For this neuron based circuits are required which have taken idea from reference paper [1].

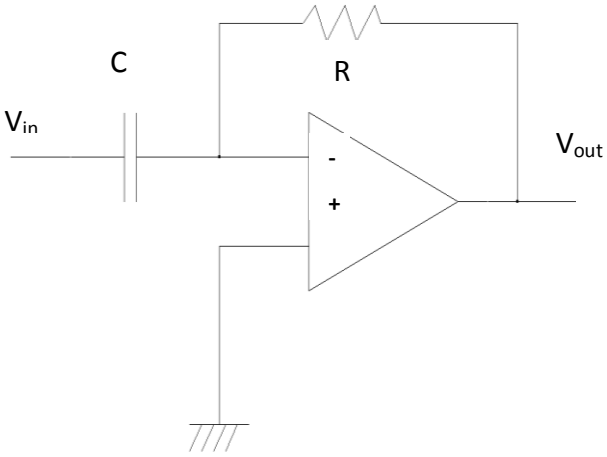

Fig 1: Simple High Pass Filter

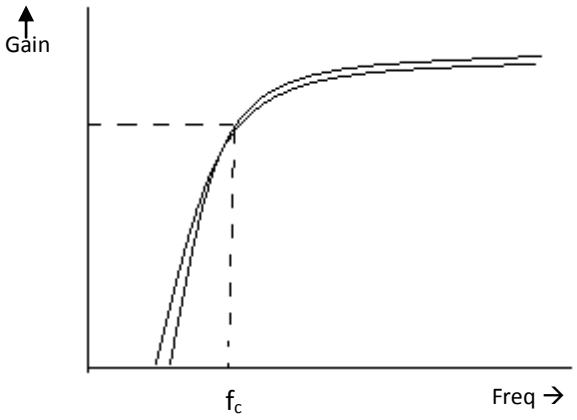

Fig 2: Characteristics of HPF

3. SYNAPSE CIRCUIT

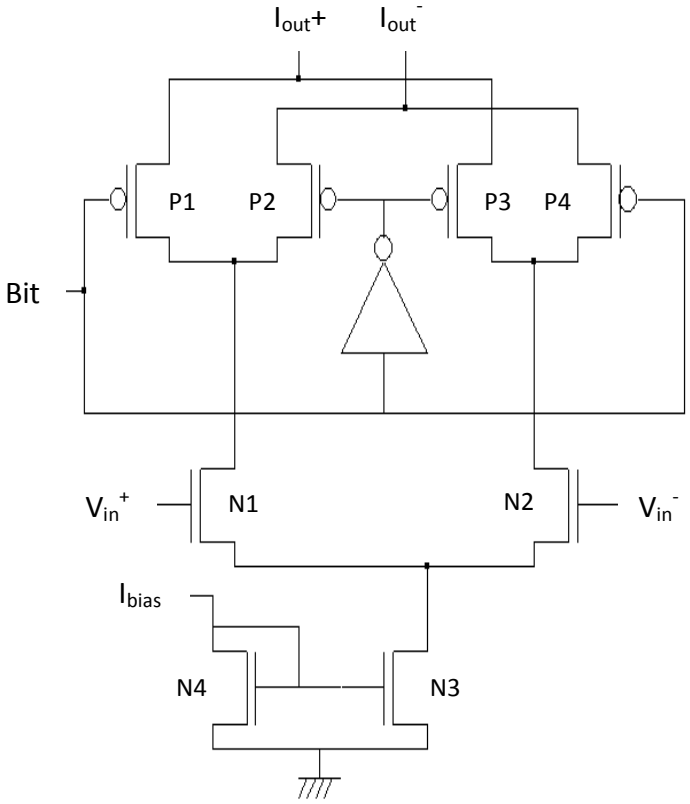

Fig.3: Schematic of the Synapse Circuit

The basic function of a synapse is multiplication. A synapse circuit[2],[3] is shown in Fig.3.It consists of 4 PMOS and 2 NMOS and takes voltage difference of expected voltage (V_{IN}^{+}) and actual voltage (V_{IN}^{-}) of output of CUT and provide output in the form of current(I_{OUT}^{+} , I_{OUT}^{-}).To a certain value of input difference voltage (0.6V), output current also varies linearly which is called linear multiplication, but if the input voltage difference increased 0.6V it gives a constant output current as is clear from the fig. 4.

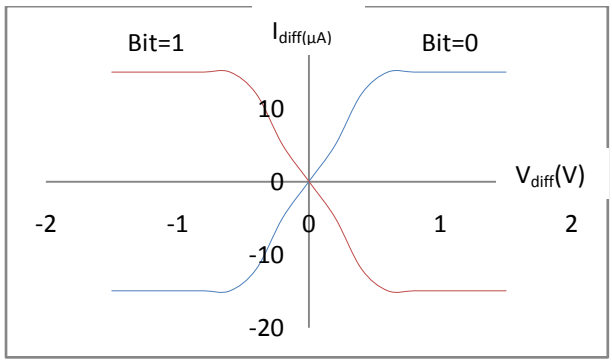

Fig.4: Synapse input voltage diff Vs output current diff

BIT is used to control the characteristics of Synapse. When BIT is low, P_1 and P_4 will be on resulting I_{OUT}^{+} and I_{OUT}^{-} which are taken from P_1 and P_4 respectively. Now when BIT is high P_3 and P_2 will be on resulting I_{OUT}^{+} and I_{OUT}^{-} which are taken from P_3 and P_2 respectively. Hence, inversion in BIT value results in inversion of characteristics, as is clear from Fig.4.

4. COMMON MODE CANCELLER

It takes output of Synapse as input and provide output current MAX (0, I_{OUT}^{+} - I_{OUT}^{-}). Common mode canceller is shown in fig. 5. It consists of 4 PMOS and 4 NMOS forming 4 pair of current mirror circuit. As per the concept of current mirror I_{IN}^{-} and drain current of P_2 will be same, which further

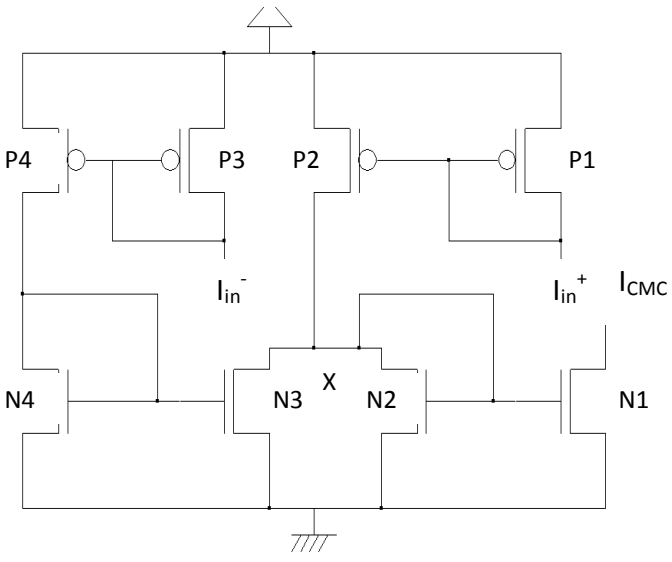

Fig.5: Schematic Common mode canceller

be equal to source current of N_2 and hence incoming current towards node X. On the other hand I_{IN}^{+} will be same as drain current of P_3 and constituting again outgoing current at node X. Difference of I_{IN}^{+} and I_{IN}^{-} will be the resultant current of node X which will further be equal to drain current of N_4 and final output I_{CMC}.

5. CURRENT TO VOLTAGE CONVERTOR WITH LEVEL SHIFTER

As name says, P_1 and P_2 convert current (I_{CMC}) coming from Common Mode Canceller into voltage which further forward to level Shifter formed by P_3 and P_4. Finally, V_{out} which will say about functional health of CUT i.e., Low pass filter. Current to voltage converter with level shifter is shown in Fig.6. It takes I_{CMC}, i.e. output of Common Mode Canceller as input and gives equivalent voltage at the output end (V_{OUT}).

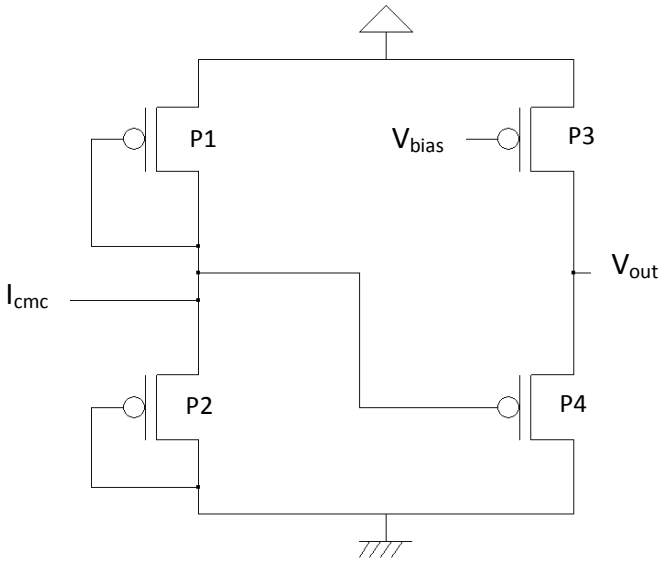

Fig.6: current to voltage converter with level shifter

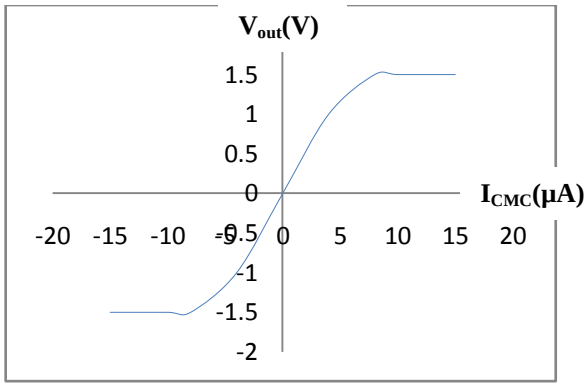

Fig.7: Input current(I_{CMC}) Vs Output voltage(V_{out})

6. HPF WITH TEST BLOCK

In fig.8, When Test Pin is high, MUX produce test stimulus to High pass filter. Their corresponding output is applied to the Synapse for comparison with actual value which is further forward to common mode canceller. Output current (I_{CMC}) is converted into voltage with Current to Voltage converter with Level Shifter.

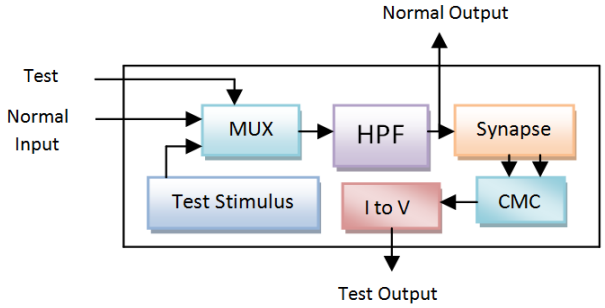

Fig.8. Block Diagram of TEST BLOCK

7. REUSLT

By applying different voltages to synapse circuit, outputs observed in all circuits are shown in Table.II and corresponding waveforms are shown in fig.9.

Table 1. Outputs of each stage of Test Block

Bit	V_{in}^+	V_{in}^-	$V_{in}^+ - V_{in}^-$	$I_{out}^+ - I_{out}^-$	I_{cmc} Max(0, $I_{out}^+ - I_{out}^-$)	V_{out}	Result
0	1V	1V	0V	0µA	0µA	0	Pass
1	1V	1V	0V	0µA	0µA	0	
0	1.2 V	1V	0.2V	5µA	5µA	1.1	Pass
1	1.2 V	1V	0.2V	5µA	0µA	0	Pass
0	1V	1.3 V	-0.3V	-7µA	0µA	0	Pass
1	1V	1.3 V	-0.3V	7µA	7µA	1.3	
0	1.7 V	1V	0.7	15µA	15µA	1.5	Fail
1	1.7 V	1V	0.7	-15µA	0µA	0	
0	1V	1.8 V	-0.8V	-15µA	0µA	0	Fail
1	1V	1.8 V	-0.8V	15µA	15µA	1.5	

8. CONCLUSION

Neural classifier which is added to HPF is able to examine its functionality, while considering the tolerance factor. In this way we are able to test any complex analog circuitry at the cost of slight increase in chip area.

Future work will focus on the replacing current mirror with floating gate and its advantages and disadvantages. Constitute of floating gate synapse is an elegant solution for long term nonvolatile memory storage and precise weight updates and local learning.

9. ACKNOWLEDGMENTS

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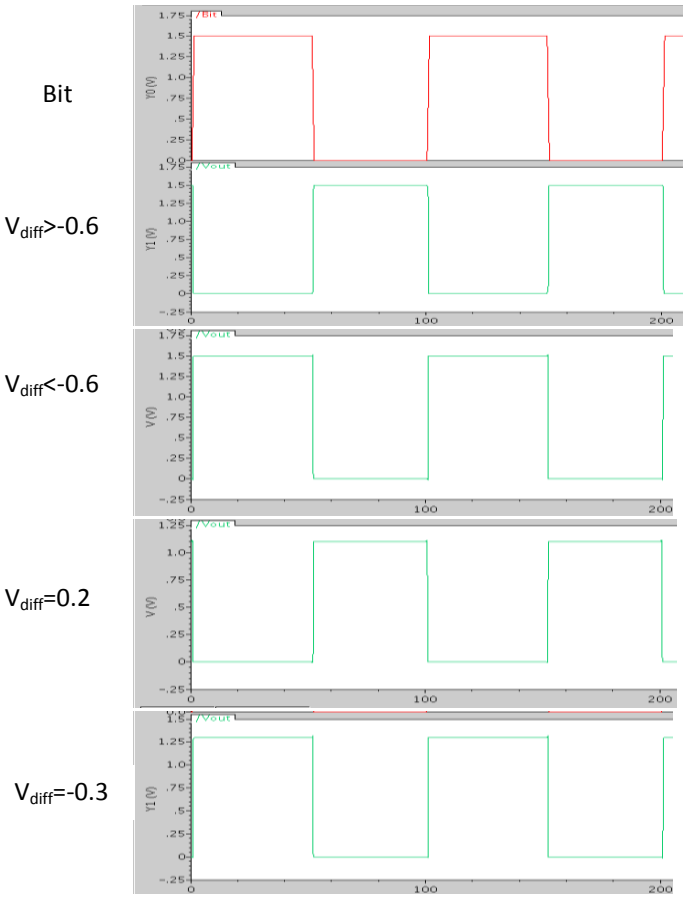

Fig.7 Waveforms for different conditions to Test Block

10. REFERENCES

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