Low Power Low Noise Tunable Active Inductor for Narrow Band LNA Design

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ABSTRACT
This paper presents a low power, low noise and high quality factor tunable single ended active inductor suitable for designing multiband RF front end circuits. The active inductor circuit uses differential configuration as positive transconductor and PMOS cascode structure as negative transconductor of a gyrator to reduce the noise voltage. It uses MOS transistor as a feedback resistor to provide possible negative resistance to reduce the inductor loss to enhance the quality factor. Also this structure provides wide inductive bandwidth and high resonance frequency. The tuning of center frequency and quality factor for multiband operation is achieved through the controllable current source. The center frequency tuning range of the active inductor varies from 3.9 GHz to 12.3 GHz. The designed active inductor and LNA are simulated in 180nm CMOS process using HSPICE simulation tool. Simulation results of the active inductor shows an inductive bandwidth varies from 6.45 MHz to 6.3 GHz with the center frequency 6.3 GHz. The inductance value ranges from 5nH to 550nH respectively. It has the less noise voltage of 12nV/√Hz to 5.6nV/√Hz for the designed tuning range and consumes less power of 0.65mW. The Low noise amplifier achieves the gain of 19dB, low noise figure of 2.1dB and consumes low power of 4.2mW.

Keywords
Active inductor, Quality factor, Centre frequency tuning, PMOS cascode pair, tuning range, MOS resistor, Multiband RF front end.

1. INTRODUCTION
The great demand for multiband wireless communication systems is increasing the requirement of integrated CMOS products for high performance RF front end circuits. Using CMOS process, the RF systems can be realized with low power consumption, high frequency range (GHz) and high reliability. Tunable and high quality inductor plays a vital role in the realization of low power multiband wireless transceivers. Though the on-chip spiral inductors are good passive devices, it is difficult to realize it for larger inductance values, high quality factor and smaller chip area [1-2]. Active inductors, on the other hand, provide large inductance value with high resonance frequency, high quality factor, small chip area and wide range of tuning ability [4-6].

The active inductor is realized using gyrator-C topology. There are several techniques for designing tunable active inductor using gyrator circuit. The possible two transistor structures of gyrator shown in [3] have some disadvantages. The structures involving a common drain stage has greater restrictions on the voltage levels required to properly bias the transistors, which has negative impact on the inductance tuning range. The circuits involving a common gate stage have a wide tuning range, but require negative resistance for high quality inductors. It is also possible to form active inductors using three or more transistors [9] and the quality factor can be improved by boosting the loop gain through feedback [10].

Low noise amplifier (LNA) is the first block of the receiver to amplify the received signal with little noise [14-15]. To prevent the reflections of the incoming signal between antenna and LNA, the input impedance of the LNA needs to be matched to the antenna impedance. In the same way, the output impedance of LNA to be matched with the load impedance for maximum power transfer. To perform this, matching networks are needed at the input and output side of LNA as shown in Fig.1.

LNAs can be designed using active inductors [13]. Active inductors can be used in the input matching network or at the load side [12]. There are four different input matching techniques used in the design of narrow band CMOS LNA are discussed in [11], they are SID, PLC, SL and PL methods.

This paper discusses the design of an active inductor with high resonance frequency, better tuning capability, less noise, less power dissipation and better linearity.

Section 2 describes the design of the proposed active inductors, circuit parameters using small signal equivalent circuit. Section 3 describes the design of LNA using Active inductor based impedance matching network. The simulation results and the discussions are presented in Section 4. and the concluding remarks are given in Section 5.

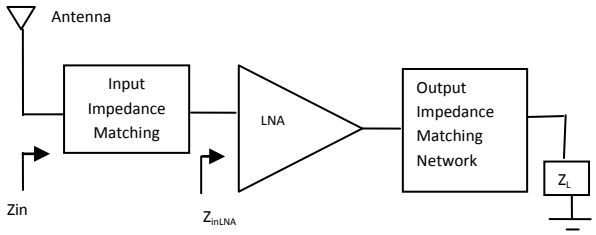

Fig 1: Block diagram of LNA with input and output matching networks

2. DESIGN OF THE ACTIVE INDUCTOR

2.1 Circuit Diagram Description
An active inductor is realized using gyrator-C topology [2] which transforms intrinsic capacitance in to inductive behavior. The proposed single ended active inductor is shown in Fig. 2. It consists of differential pair m1 and m2 which represents the positive transconductor G_{m1} between the input (node 1) and the

output (node 3). The cascode pair m3 and m4 represents the negative transconductor $-G_{m2}$ between the input (node 3) and the output (node 1). Thus the G_{m1} and $-G_{m2}$ forms the gyrator which converts the parasitic capacitance C_3 at node 3 to an equivalent inductance Leq $=C_3/G_{m1}G_{m2}$. The passive equivalent circuit of the gyrator structure is as shown in Fig. 3.

The proposed active inductor uses PMOS cascode structure as negative transconductor, which can lead to possible negative resistance in series with the equivalent inductor to compensate the inductor loss. The p-channel transistors are preferred for cascode structure as they have low noise and they can be placed in separate n-wells, thus eliminating the non- linear body effect [3]. Thereby, it enhances the quality factor of the active inductor. It also achieves high resonance frequency and better inductive bandwidth.

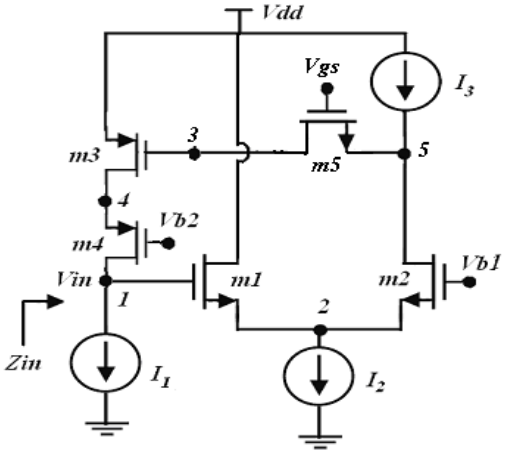

Fig. 2: Circuit diagram of proposed single ended active inductor

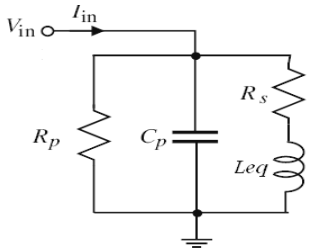

Fig. 3: Equivalent circuit of the proposed active inductor

To further improve the quality factor, series resistance R_s has to be reduced. This can be done by adding the transistor m5 between the positive transconductor and the negative transconductor of the active inductor. The transistor m5 act as feedback resistor enhances the loop gain and increases the quality factor of the active inductor. The transconductance of the transistor is controlled through the Vgs supply at the gate of the transistor m5, which is turn varies the loop gain and the center frequency of the active inductor. It also reduces the noise contributed by the m2 transistor.

2.2. Parameters of the Active Inductor

The equivalent input impedance Z_{in}, can be obtained from the small signal analysis circuit shown in Fig. 4.

$$Z_{in}(s) = g_1 + sC_1 - \frac{gm_5gm_4gm_3gm_2gm_1}{(G+sC_2)(g_3+sC_3)(gm_4+g_4+sC_4)(gm_5+SC_4+g_5)} \quad (1)$$

Where $G= gm_1+gm_2+g_2$.

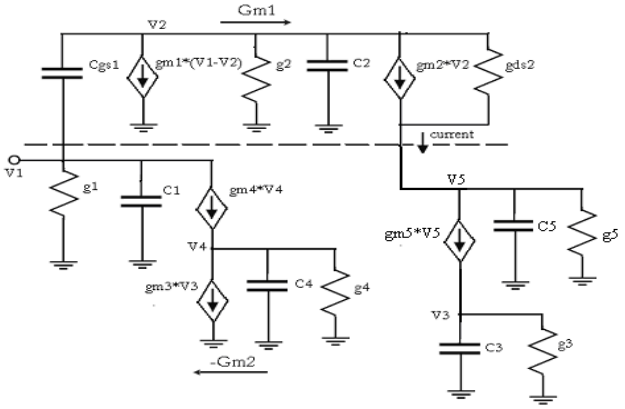

Fig. 4: Small signal equivalent circuit of the active inductor

The equation (1) is simplified and using the equivalence $s^3 = -\omega^2 s$[2], it is given as,

$$Z_{in}(s) \approx \frac{\frac{sg_4g_5}{C_1} + \frac{g_3\, g_4g_5}{C_1C_3}}{s^2 + sXg_4g_5 + Y} \quad (2)$$

Where X and Y are,

$$X = \frac{g_1}{C_1} + \frac{C_2g_1g_3}{GC_1C_3} + \frac{g_3}{C_3} - \frac{\omega^2C_2}{G}Y$$
$$= \frac{gm_5gm_4gm_3gm_2gm_1 + Gg_1g_3\,[gm_4+g_4][gm_5+g_5]}{GC_1C_3}$$

The format of Z_{in} shows that it is equivalent to a RLC network, as shown in Fig. 3. The 's' term in the numerator of equation (2), indicates the equivalent inductance and the real term indicates a resistor in series with the inductor. From equation (2), L_{eq} and R_s can be written as,

$$L_{eq} = \frac{C_3Gg_4g_5}{gm_5gm_4gm_3gm_2gm_1 + Gg_1g_3\,[gm_4+g_4][gm_5+g_5]} \quad (3)$$

$$R_s = \frac{Gg_3g_4g_5}{gm_5gm_4gm_3gm_2gm_1 + Gg_1g_3\,[gm_4+g_4][gm_5+g_5]} \quad (4)$$

The parallel capacitance $C_p = C_1$ and the parallel resistance $R_p = 1/g_2$. The resonance frequency ω_o and the quality factor Q_o are given as,

$$\omega_0 = \sqrt{\frac{gm_5gm_4gm_3gm_2gm_1 + Gg_1g_3\,[gm_4+g_4][gm_5+g_5]}{GC_1C_3}} \quad (5)$$

$$Q_0 = \frac{\sqrt{\frac{gm_5 gm_4 gm_3 gm_2 gm_1 + Gg_1g_3\left[gm_4 + g_4\right]\left[gm_5 + g_5\right]}{GC_1C_3}}}{\left[\frac{g_1}{C_1} + \frac{C_2 g_1 g_3}{GC_1C_3} + \frac{g_3}{C_3} - \frac{\omega^2 C_2}{G}\right] g_4 g_5} \qquad (6)$$

3. DESIGN OF LNA USING ACTIVE INDUCTOR IN THE INPUT MATCHING NETWORK

The design of low noise amplifier comprises two stage amplifiers with resistive feedback as shown in Fig.5. The first stage of the amplifier is the common source configuration with source inductive degeneration and gate inductance. Lg ,Ls and cgs of M1 forms input impedance matching network of the LNA. Ls is the source degenerative inductance which can be replaced by the tunable active inductor which is used to make the input impedance matched to the antenna impedance to prevent the incoming signal reflections between antenna and the LNA. The second stage of the amplifier is also the common source amplifier with resistive feedbacks to obtain low noise and high stable output. Rf1 is voltage current feedback used to lower the transimpedance of the network and Rf2 is the voltage-voltage feedback which is used to stabilize the output voltage amplitude in spite of load variations.

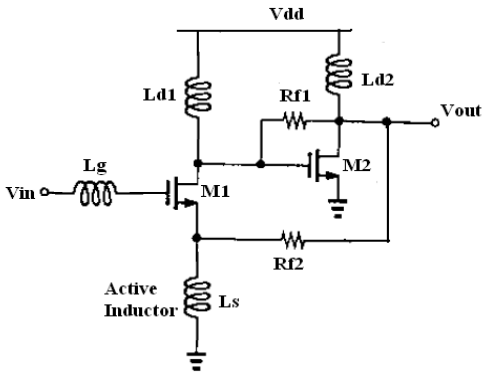

Fig.5: Circuit diagram of LNA with input matching network

From the small signal analysis of the LNA, the input impedance is calculated using the equation (7) as given below,

$$Z_{inLNA} = j\left[\omega\left(L_s + L_g\right) - \frac{1}{\omega C_{gs}}\right] + \frac{g_{mL_s}}{C_{gs}} \qquad (7)$$

The resonance frequency is given as,

$$\omega_o = \frac{1}{\sqrt{\left(L_s + L_g\right)C_{gs}}} \qquad (8)$$

The closed loop gain of the amplifier is expressed as,

$$Av = \frac{\frac{(j\omega L_{d1} \parallel R_{in2})(-g_{m2}R_{f2} + 1)j\omega L_{d2}}{\left(j\omega L_s \parallel R_{f1} + \frac{1}{g_{m1}}\right)(j\omega L_{d2} + R_{f2})}}{1 + \left(\frac{j\omega L_s \parallel R_{f1}}{R_{f1}}\right)\left(\frac{j\omega L_{d1}}{j\omega L_s \parallel R_{f1} + \frac{1}{g_{m1}}}\right) X \left(\frac{(-g_{m2}R_{f2} + 1)j\omega L_{d2}}{j\omega L_{d2} + R_{f2}}\right) X \left(\frac{j\omega L_s}{j\omega L_s + R_{f1}}\right)} \qquad (9)$$

4. SIMULATION RESULTS

4.1 Active Inductor

The simulations are carried out in 180nm CMOS process using HSPICE simulator. The transistor sizes (W/L in µm) of Fig. 1 are m1 (1.49 /0.18), m2 (2.7/0.18), m3 (3/0.18), m4 (4.95/0.18) and m5 (1.49/0.18). The supply voltage Vdd is given as 1.2V. The gate bias voltages are kept as Vb1=0.2V, Vb2=137mV and Vgs=0.3V. The controllable current sources are I_1=90µA, I_2=60µA and I_3=50µA. The current sources are realized using MOS current sources operating with the bias voltage of 0.8V. The small signal parameters gm_1 = 156µS, gm_2 = 566µS, gm_3 = 250µS, gm_4 = 1.3mS, gm_5 = 60.5mS, g_1= 22µS, g_2= 80µS, g_3= 669µS, g_4= 94µS, g_5= 45µS, C_1=270.66aF, C_2=621.3aF, C_3=2.35fF, C_4= 3.45fF,C_5= 592.78aF and G= 802µS are found from the operating points. Using these parameters in the equations (5) and (6) the resonance frequency and quality factor are calculated to be f_o=6.3GHz and Q_o=723 respectively. To verify the designed equations, the circuit of Fig. 2 was simulated.

4.1.1 Input Impedance

The simulated frequency response of Z_{in} is shown in Fig. 6. The magnitude of Z_{in} is nearly 160dB and the phase change is from +90◦ to -90◦. The magnitude response shows that it has real term and imaginary term. It is constant at 55dB up to 6.45 MHz which is equivalent to the real term. The real term is the series resistance R_s, which is calculated to be 123Ω.

The response is increased from 6.45 MHz to 6.3 GHz which is equivalent to the imaginary term, the equivalent inductance L_{eq}. The value of inductance ranges from 5nH to 550nH. Since it has less series resistance, the inductor loss is reduced.

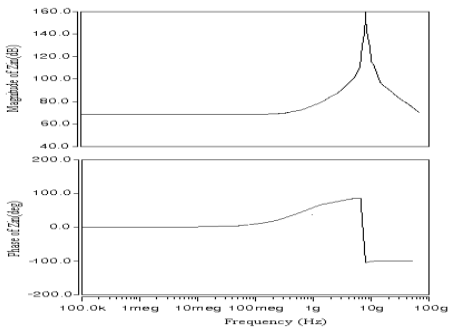

Fig. 6: Simulated Frequency Response of Input Impedance

4.1.2 Noise *Voltage*

The proposed active inductor also features low power dissipation of 0.65mW. The noise output voltage varies from 12nV/√Hz to 5.6nV/√Hz for the tuning range 3.99 GHz to 12.3 GHz. Fig. 7 shows the noise voltage(V^2/Hz).

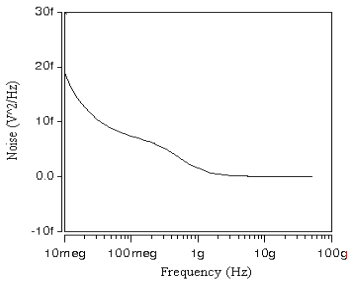

Fig . 7: Noise Voltage of the Active Inductor

4.1.3 Quality Factor Tuning

From the real and imaginary values of the simulation results, the quality factor Q_o is calculated to be 1067 at the frequency f_o=6.3GHz. Fig. 8 shows the variation of Z_{in} for different values of controllable current source I_2. When I_2 is varied from 65µA to 120µA, the Z_{in} brings corresponding changes in R_s and L_{eq} which in turn changes the quality factor. Hence, the quality factor can be tuned through the controllable current source I_2. The better quality factor of nearly 1067 for frequency 6.3 GHz is attained, when I2 is 65 µA.

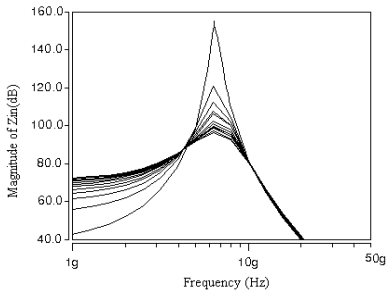

Fig. 8: Quality factor Tuning

4.1.4 Center Frequency Tuning

The center frequency f_o is tuned through the controllable current source I_3 of Fig 2. Fig. 9 shows the tuning of the active inductor for various center frequencies. The controllable current source I_3 is varied between 35µA and 55 µA for tuning the center frequency of the active inductor. The designed active inductor has wide tuning range of 3.99 GHz to 12.3 GHz. For better gain Vgs has to be fixed to the different voltage for various center frequencies.

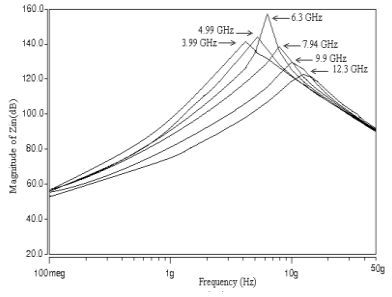

Fig. 9 : Center Frequency Tuning

Table 1 compares the performance of the proposed active inductor with the results in the literatures [2, 6, and 7]. The performance comparison shows that the proposed active inductor has good quality factor, wide inductive bandwidth, and low power consumption, very less noise, wide tuning capability and better linearity.

Table 1: Comparison of Active Inductor Performances

Parameter	**Ref. [2]**	**Ref. [7]**	**Ref. [8]**	**This work**
Technology	0.20µm /1.8V	0.13µm/ 1.2V	90nm/ 1.2V	0.18µm/ 1.2V
Inductive BW	n.a	300MHz - .32GHz	600MHz - .8GHz	6.45MHz – 6.3GHz
L(nH)	29	38-144	165-530	5-550
Q_L(max)	n.a	3900@5.7 GHz	120@3 GHz	1067@6.3 GHz
P_{dis}(mW)	4.4	1	1.2	0.65
Noise	0.8µV/ √Hz	69.31µV*	43.37nV*	8.3nV/ √Hz

4.2 Low Noise Amplifier

The simulation results of Low noise amplifier shows that it has the forward transfer gain S21 of 19dB as shown in figure 10 and consumes power of 4.2 mW. The designed LNA has better input impedance matching with S11 of less than 11. Figure 12 shows the designed LNA has low noise figure of 2.1 dB for the frequency range 1GHz to 5GHz. Table 2 compares the performance of the designed LNA with the results in the literatures [15].

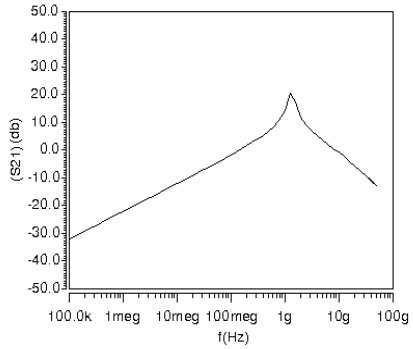

Fig. 10: Gain S21 of LNA

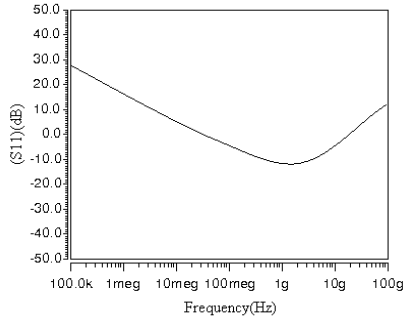

Fig 10: Input impedance matching S11 of LNA

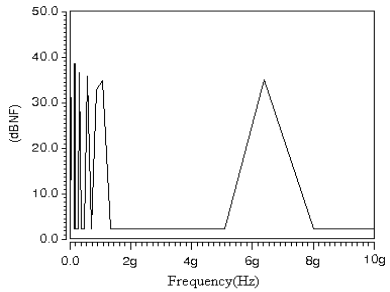

Fig. 11: Noise Figure of LNA

Table 2. Comparison of LNA performances

Parameter	Ref. [16]	This Work
Technology	0.13µm	0.18µm/1.2V
Gain (S21)	16.4dB	19dB
S11	<-13dB	<-10dB
Power dissipation (mW)	3.2mW	4.2mW
Noise Figure	3.5dB	2.1dB

5. CONCLUSION

A Tunable CMOS active inductor and LNA simulated in 180nm CMOS process was presented. The simulation results of active inductor show that the circuit has wide inductive bandwidth, high resonance frequencies, low noise and low power consumption. The designed active inductor is used in input impedance matching network of LNA, for narrow band design. It has achieved high gain, low noise figure and low power consumption which is suitable for designing RF front end circuits.

5. ACKNOWLEDGEMENT

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