Low Power Variable Gain Amplifier with Bandwidth Of 80–300 MHz Using For Sigma-Delta Analogue to Digital Converter in Wireless Sensor Receiver

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ABSTRACT
Variable-gain amplifier (VGA) is one of the basic building blocks of many communication systems. In this paper we present a novel structure of VGA with 22 db of gain range and 220 MHz of bandwidth frequency variation. This circuit combines a voltage to current (V-I) converter and two-stage CMOS amplifier to achieve programmable gain and bandwidth .The gain is varied by changing the input voltage (V_{in}) from -1V to 0V. The maximum bandwidth is about 300 MHz. The gain can be varied from 38 dB to 60 dB in 1 dB gain steps. The overall circuit draws current from 10µA to 150µA at ±1.5V power supply. The noise figure of the system at maximum gain is 18dB, and the third-order intermodulation intercept point (IIP3) at minimum gain is -8 dBm. Simulations results with static and dynamic behaviour is presented and validated with the technology AMS 0.35µm. Eventually we have also succeeded in reducing the static power consumption to 0.5 mW.

General Terms
Mixed signal, Wireless sensor.

Keywords
Radio Frequency receiver, VGA, CMOS analog integrated circuits, CMOS OTA Design.

1. INTRODUCTION
Many proposed new standards are under consideration for wireless sensor networking [1] [2] such as Bluetooth (IEEE 802.15.1), UWB (IEEE802.15.3), and Zigbee (IEE 802.15.4). Each of these standards is accompanied by limitations for sensor networks. Like Bluetooth devices which consume high power for sensor network applications [3].
In particular direct conversion receiver (figure 1) which has attracted widespread attention for its simple architecture and easy integration with the base band circuit, as well as for its low power consumption and low manufacturing costs [4].
According to figure 1, the block diagram of a direct conversion receiver is presented receiver section of an integrated where spectrum receiver operating in the 863– 870 MHz. This receiver architecture directly down converts the signal to base band rather than converting it into an intermediate frequency (IF) first, and image rejection is no longer necessary in this approach. In the first, the RF signal that comes out of the antenna is filtered by the band pass filter (BPF).Then, it is amplified by the low noising amplifier (LNA) before being down converted directly to base band along parallel in-phase (I) and quadrature (Q) signals. The frequency translation is performed by using two mixers using 0° and 90° phase shifted local oscillator (LO) signals. Finally, the I and Q base band signals are low pass filtered and amplified with variable gain amplifier (VGA) before the analogue to digital converter (A/D) conversion is intervened. In this case VGA is used to maximize the dynamic range of the system. It plays an important role of stabilizing the amplitude of a signal of interest under various conditions, providing constant amplitude signal in the signal path.

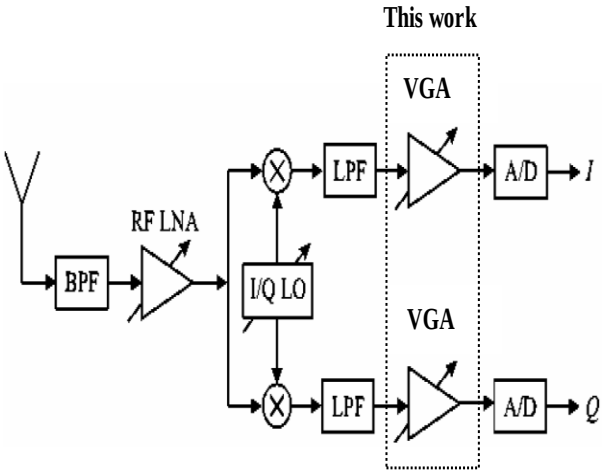

Figure 1: Block diagram of a direct conversion receiver or homodyne architecture

This paper addresses the design of a 220MHz VGA with 22 dB of gain range. The CMOS VGA architecture is based on a differential pair stage with voltage to current (V-I) converter, in which the gain is varied by changing the input voltage (V_{in}) from -1V to 0V. Then the output signal is sampled by the discret-time low pass Sigma-Delta (εΔ) modulator and then processed by the digital block. The two-stage VGA was analyzed and designed in Austriamicrosystems (AMS) 0.35µm CMOS technology.

This paper is organized as follows. Section 2 briefly discusses the receiver specification. Section 3 discusses the VGA design based on a differential pair stage with voltage to current

converter in which all simulations are specified, and full comparison of the performance of each VGA design are presented. Section 4 presents our conclusion.

2. RECEIVER SPECIFICATION

The main objective of a receiver for wireless communication applications is to recover the base band signals that are modulated on a carrier wave at radio frequencies.

The design of a high performance, low power integrated radio frequency receiver in mainstream silicon technologies CMOS is a very challenging task involving numerous tradeoffs during the design process, especially between noise, linearity and power consumption.

To achieve the objective cited above, all aspects of the receiver and radio system (Base band, Modulation scheme, hopping bandwidth, data rate, Sensitivity, Maximum range, BER...) must be responded [5].

To characterise the sensor thermal noise (N_t) is given by:

$$N_t = -174 + 10\log_{10}(f_b) = -125\ dB \quad (1)$$

Another two elements defining sensor are SNR_{in}, SNR_{out} (Signal to Noise Ratio) which are based on the following formula:

$$SNR_{in} = S - N_t = 23\ dB \quad (2)$$

$$SNR_{out} = \left(\frac{E_b}{N_0}\right)_{dB} - 10\log_{10}\left(\frac{f_b}{D}\right) = 5\ dB \quad (3)$$

As shown in figure 2, (Eb /N0) is equal to 11 with Noncoherent Frequency Shift Keying " NC-BFSK " to attenuate a bit error rate (BER) of 10^{-3} which is based on the following formula:

$$BER_{NC-BFSK} = \frac{1}{2} \times e^{-\frac{1}{2}\frac{E_b}{N_o}} \quad (4)$$

with D represented data rate of 20 Kbps.

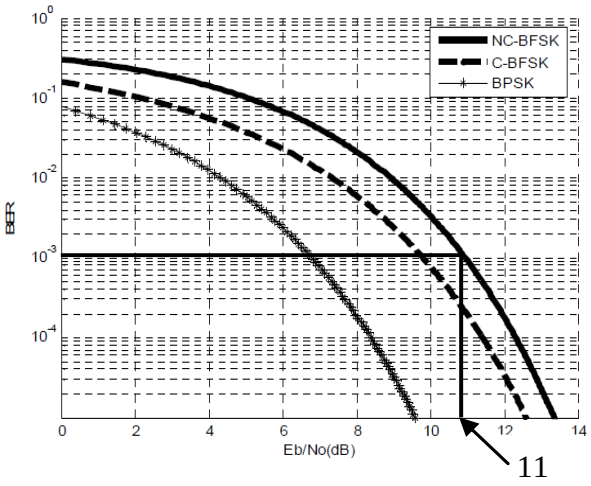

Figure 2: Bit error rate (BER) for BPSK, C-BFSK and NC-BFSK

In order to realize a low power integrated radio frequency receiver used for wireless sensor receiver, we must respond to technological specifications and requirements listed in Table 1.

Table 1. Summarize table of wireless sensor receiver specification

Parameters	Value
Base band frequency (f_b)	80 KHz
Modulation scheme	BFSK
Hopping bandwidth	7 MHz (863-870)MHz
Channels number	58
Data rate (D)	20 Kbps
Maximum range	50 m
BER	10^{-3} @ Eb/No=11dB
Sensitivity (S)	-102 dBm

3. VGA DESIGN AND SIMULATIONS

3.1 VGA and Sigma-Delta analog to digital converter (ADC)

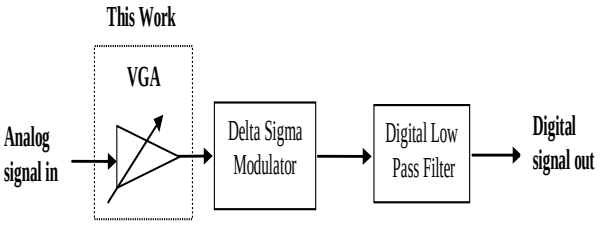

Figure 3: Block diagram of the A/D converter with VGA

The Block diagram (Figure 3) is described as follows: the analog input signal enters the variable gain amplifier front-end stage, which translates this signal to the processing frequency, providing gain control to adjust its dynamic range, the selected signal is sampled by sigma-delta (εΔ) modulator and then processed by the digital low pass filter. Here, VGA plays an important role in supplying a constant-amplitude signal to the Sigma-Delta analogue to digital converter.

Sigma-Delta (εΔ) analog to digital converters (ADC) have been successful in realizing high resolution consumer. With VGA, (εΔ) converters are well suited for low bandwidth, high-resolution acquisition, and low cost, making them a good ADC choice for many applications such as wireless sensor.

The effective number of bits of Sigma-Delta (N_{eff}) converter is given by [6]:

$$N_{eff} = \frac{1}{2}\log_2\left[(2N-1)^2(2L+1)OSR^{2L+1}/(\pi)^{2L}\right] \quad (5)$$

Where N represents number of bits of the quantization circuitry (N = 1), L represents order of modulator (L = 2) and OSR means Over Sampling Ratio which is based on the following formula:

$$OSR = \frac{F_s}{2 \times f_b} \quad (6)$$

To simplify the decimator design, the oversampling ratio is usually chosen in powers of 2 and hence 128 has been chosen as the oversampling ratio, we obtain an effective number of 15.95 bits. F_s is the sampling frequency which is calculated to 10.240MHz, and f_b means base band frequency (80 KHz).

The number 15.95 bits is the theoretical number because errors in the structure of parasites modulator reduce the SNR and therefore the number of bits, and to ensure low power and minimum consumption the number of bits is chosen as 16 bits

3.2 VGA performance

Variable gain amplifiers (VGAs) are essential components of many communication and electronics systems. In a radio frequency (RF) transceiver, the received signal typically has a high dynamic range. In order to supply a signal of constant amplitude to a base band section of the transceiver, a variable gain amplifier (VGA) with equivalent or better dynamic range is required. VGAs can be found in many applications and are used to maximize the dynamic range of overall systems in medical equipments, telecommunication systems, wireless sensor receiver, hearing aids, disk drives, and others. In wireless sensor receiver the VGAs play the important role of stabilizing the amplitude of the output signal under various conditions and supply a constant-amplitude signal to the Sigma-Delta analogue to digital converter.

The most demanding characteristics of a variable gain amplifier (VGA) are Noise Figure (NF), the third-order Intermodulation Intercept point (IIP_3), compression Point (P_{-1}) and Blocking Dynamic Range (BDR). The VGA specifications are calculated and presented below:

The Noise Figure (NF) is defined as:

$$NF = \frac{SNR_{in}}{SNR_{out}} = SNR_{in}(dB) - SNR_{out}(dB) = 18\ dB \quad (7)$$

Where SNR_{in} and SNR_{out} are input and output Signal to Noise Ratio.

In order to determine the third-order intermodulation intercept point (IIP_3), we firstly calculate the intermodulation product (IMR) by this expression:

$$IMR = P_{in} - P_{test} + SNR_{out} = -41 + (-99) + 5 = 63\ dBm \quad (8)$$

Where we estimate (P_{in}) the power levels of intermodulation interference equal to -41 dB. P_{test} is the test signal power given by:

$$P_{test} = S + 3 = -99\ dBm \quad (9)$$

Where S represents the sensitivity of -102 dBm. We obtain the third-order intermodulation intercept point (IIP_3) by:

$$IIP_3 = 0.5 \times IMR + P_{in} = -9.5\ dBm \quad (10)$$

Compression point (P_{-1}) is given by :

$$P_{-1} = IIP_3 - 10 = -19.5\ dBm \quad (11)$$

The Blocking Dynamic Range (BDR) can be expressed by:

$$BDR = P_{-1} - S = -19.5 - (-102) = 82.5\ dB \quad (12)$$

In order to achieve a novel structure of VGA with low power and high performance all aspects of the wireless sensor receiver must be respected. A summary of the VGA performance is listed in Table 2.

Table 2. Performance summary

Parameters	Value
Noise figure (NF)	18 dB
Third-order intermodulation intercept point (IIP_3)	-9.5 dBm
Compression point (P_{-1})	-19.5 dBm
Blocking Dynamic Range (BDR)	82.5 dB

In a variable gain amplifier, a control unit will provide a gain signal to the variable gain amplifier, and, based upon the gain signal. The variable gain amplifier will accordingly amplify an input signal by an amount corresponding to the gain signal, to obtain an amplifier output signal. In order for a signal of a constant level to be supplied to a base band terminal of the received signal, the variable gain amplifier must also have a high dynamic range. The VGA is a circuit that manually controls its gain in response to the amplitude of the input signal, leading to a constant-amplitude output.

3.3 Circuit description

Figure 4 shows the architecture of the proposed VGA. It is composed of an Operational amplifier (op-amp) and a voltage to current (V-I) converter

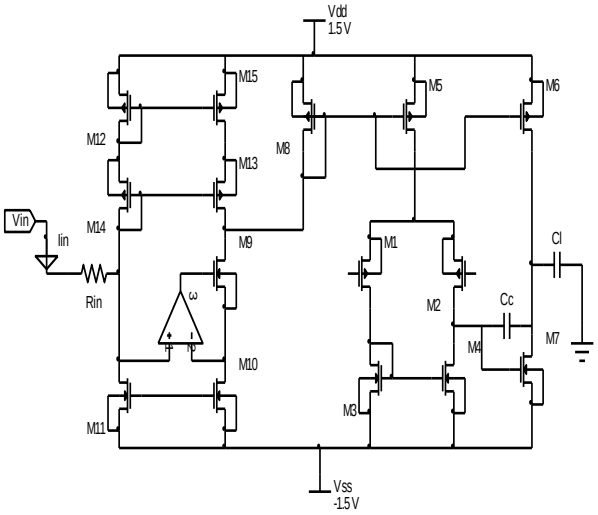

Figure 4: Architecture of the proposed two-stage VGA

Firstly, operational amplifiers (op-amp) have sufficiently high voltage gain so that when the negative feedback is applied, the closed-loop transfer function can be made practically independent of the gain of the op-amp. This principle is employed in many useful analog circuits and systems such as our application. The primary requirement of an op-amp is to have an open loop gain which is sufficiently large to implement the negative feedback concept. The OTA is made up of three stages even though it is often referred to as a "two-stage" op-amp, ignoring the buffer stage. The latter introduces an important concept of compensation. The primary goal of compensation is to maintain stability when negative feedback is applied around the operational amplifier.

The basic circuit diagram of two-stage CMOS differential amplifier is often desired as the first stage in an op-amp due to its differential input to single-ended output conversion and its high gain. The input devices of the differential pair are formed by P-channel MOSFETs M1 and M2. Either N-channel MOSFET (NMOS) or P-channel (PMOS) input devices can be used. However, PMOS input devices are used more often thanks to improved slew rate and reduced 1/f noise [7]. The

use of PMOS input devices also provides reduced power supply rejection thanks to the current mirrors, and low sensitivity to change in power supply voltage. This first stage of op-amp also had the current mirror circuit formed by an N-channel MOSFETs, M3 and M4. The transistor M7 serves as an P-channel common source amplifier which is the second stage of op-amp. The current I_{bias} of the op-amp circuit goes through current mirrors formed by P-channel MOSFETS, M8, M5 and M6. It is designed to produce a variable current between 10 µA and 150µA.

Secondly, as shown in figure 5 a proposed voltage to current converter is presented. This circuit offers a comparison between drain source voltage of M1 and M2 by using a differential amplifier to provide higher accuracy of the current copy. The input injection current signal I_{in} is formed by variable input voltage V_{in} with resistance R_{in}. On the one hand, we obtain a reduction of the input impedance which given by this relation:

$$R_{in} = \frac{1}{gm_1 . A_{olinp}} \quad (13)$$

and a very high output impedance, its value is:

$$R_{out} = ro_2 . A_{olout} = ro_2 . Av_{MC2} . Av_{op\,amp} \quad (14)$$

Where gm and ro are the small-signal transconductance gain and the output resistance of the MOS transistors. In this case we assume that the amplifier have an input open-loop gain A_{olinp} and output open-loop gain A_{olout} ($A_{olout} = Av_{MC2}.Av_{omp}$). Av_{MC2} and $Av_{op\ amp}$ denote the voltage gain of the transistor MC2 and amplifier gain respectively.

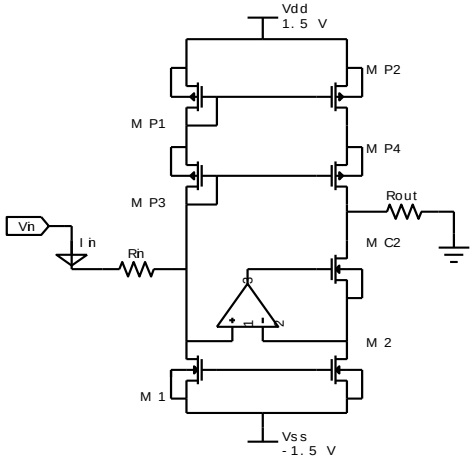

Figure 5 : proposed voltage to current converter

On the other hand, the drain source voltage of the mirror transistor M1 achieves a small constant value thanks to current source I_{in} and variable voltage source V_{in}. Drain source voltage can be decreasing to a minimum value, by selection of V_{in} from -1V to 0V and consequently a very low input voltage of the circuit.

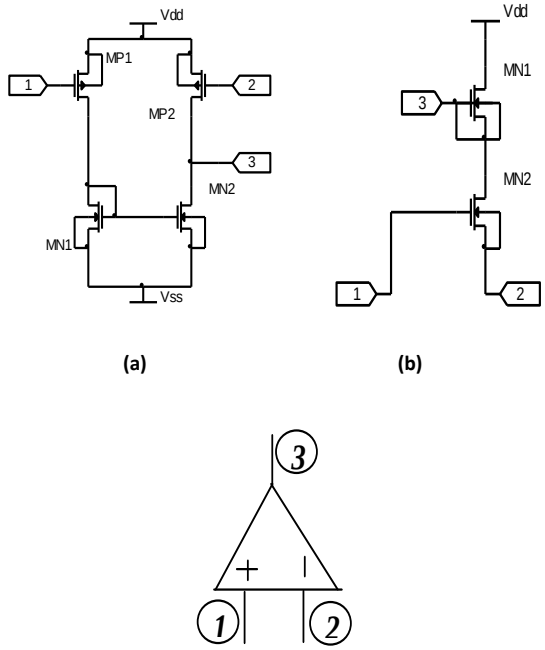

Figure 6: amplifier configuration:
(a) Simple differential amplifier structure [8]
(b) Two-transistor amplifier structure [9]

In order to achieve high current copy accuracy, it is necessary to use an amplifier between the mirror's input and output transistors.

The amplifier architectures are: simple differential amplifier and amplifier proposed by K. tanno. As shown in figure 6(a) [8], this structure is formed by the input differential pair (MP1 and MP2) and the active charge (MN1 and MN2). The figure 6(b) [9] shows a differential amplifier with two MOS transistors (MN1 and MN2) in which MN1 is operated in the weak version region (source gate voltage of MN1 equal to zero).This version can operate either in the linear region or in the saturation region for achieving low voltage and low consumption. For this reason we use this structure in our circuit.

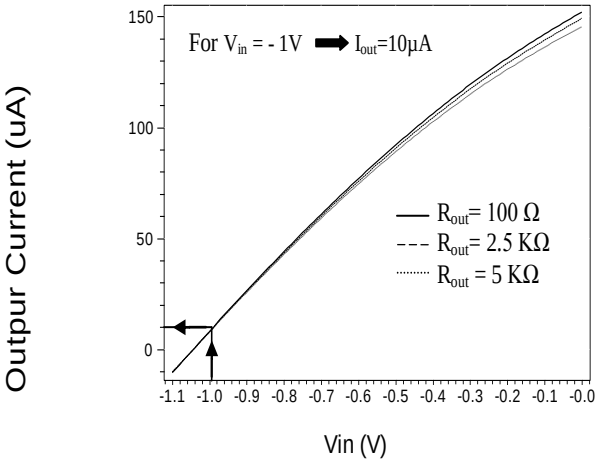

Figure 7: DC characteristics of V-I converter for different values of resistance R_{out}

Tspice simulations are carried for load resistor of 100 Ω. For an input voltage V_{in} varied from -1.1V to 0V, Figure 7 shows the DC characteristic for the V-I converter for different values

of resistance (R_{out}=100 Ω, R_{out}=2.5 KΩ, R_{out}=5 KΩ) in which the full input voltage swing capability is evident with truly linearity.

According to figure 8, the deviation of the DC output current from the ideal characteristic for different values of resistance R_{out}. The large error is reached for the lowest input voltage V_{in} of -1.1V. On the other hand the variation of V_{in} between -0.95V to 0V provide a small current error under 0.1% . For the maximum current error of 0.5%, V_{in} varied from -1.1V to -0.95V.

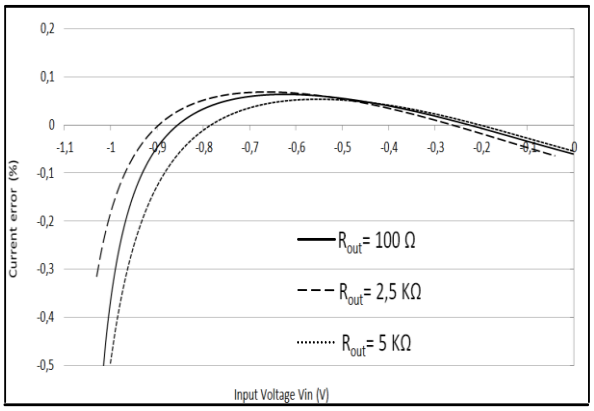

Figure 8: Current error of V-I converter

The figure 9 shows the AC characteristic of the proposed V-I converter. For a resistance of 100 Ω, we achieved a gain bandwidth (GBW) equal to 750 MHz, and 80.2 dB gain (Av).

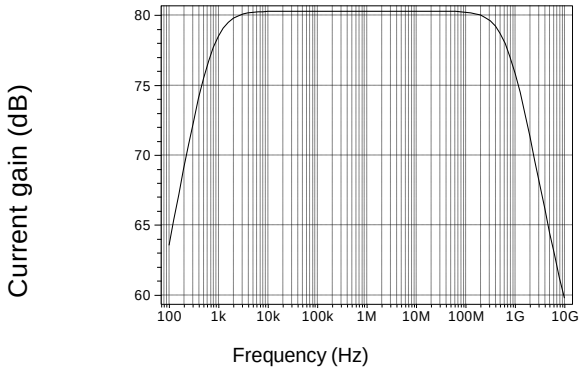

Figure 9: Frequency response of proposed V-I converter

3.4 VGA Simulations

The schematic of the gain stages is provided in Figure 4. As shown in this figure, the current I_{bias} of the op-amp circuit goes through current mirrors formed by P-channel MOSFETS, M8, M5 and M6. These transistors are used in strong inversion region to produce variable current.

The strong inversion region is the most frequently used among the three regions. In the strong inversion region, the commonly used drain current I_D with V_{GS} variation is represented by the square law equation:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[V_{GS} - V_T\right]^2\left[1+\lambda\,(V_{DS} - V_{eff})\right] \quad (15)$$

In this expression, μ is the surface mobility of the channel, C_{ox} is the capacitance per unit area of the gate oxide, W is the effective channel width, L is the effective channel length, λ is the channel length modulation factor, V_{GS} is the gate-to-source voltage, V_T is the nominal threshold voltage and V_{DS} is the resulting drain-to-source voltage.

The transconductance in the strong inversion region is [10]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2\,\mu\, C_{ox}.\frac{W_1}{L_1}.\, I_D} \quad (16)$$

Where $I_D = I_5$, $g_m = g_{m1}$, $\mu = \mu_p$ (17)

In this work the gain bandwidth of OTA is given by this relation:

$$GBW = \frac{g_{m1}}{2.\pi.C_c} \quad (18)$$

From equation (16) we can simplify the gain bandwidth to:

$$GBW = K\sqrt{I_5} \quad (19)$$

Where K is constant expressed as:

$$K = \frac{\sqrt{2\,\mu_p\, C_{ox}.\frac{W_1}{L_1}}}{2.\pi.C_c} \quad (20)$$

As shown in figure 10 by using equation (19) and MATLAB simulation, the variation of output current of V-I converter from 10μA to 150μA provide a variations of the gain bandwidth from 80 MHz to 300 MHz

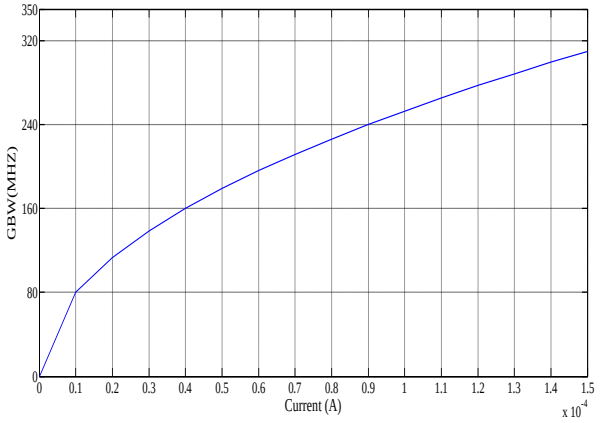

Figure 10: GBW Vs output current of the voltage to current converter

Figure 11 shows the simulated frequency response of the VGA over the entire gain range. As seen in the figure, the proposed design achieves the desired gain range of 22 dB in 1dB gain steps. The minimum bandwidth is 80 MHz, and the maximum bandwidth is limited to 300MHz for a load capacitance of 0.2 pf.

The overall performance of the two-stage VGA is summarized in Table 3 and is compared with previously reported work. As can be seen from this table, the proposed VGA has a competitive linearity, gain range, power consumption, and active area compared to other designs.

Reference	CMOS process	Bandwidth (MHz)	Supply Voltage(V)	Power (mW)	Gain range(dB)/ no.of stages	Min. And Max gain (dB)	IIP3 (dBm) @ Gmin	P_{-1} (dBm)@ G_{min}	NF (dB) @ G_{min}	Gain control
[11]	0.25µm	30~210	2.5	27.5	80/4	-35~55	7	-8	8	Analogue
[12]	0.35µm	10	3	35	60/3	*	*	*	*	Analogue
[13]	0.18µm	32~1050	1.8	6.48	95/2	-52~43	*	-17	*	Analogue
[14]	0.25µm	380	2.5	63.25	80/4	-70~11	*	*	11	Analogue
[15]	0.5µm	150	3.3	12.5	15/1	-5~10	*	*	*	Analogue
[16]	0.35µm	21	1.5	24.8	26/1	-6~20	*	*	*	Analogue
[17]	2 µm	~6	3	2.88	30/1	-0.4~29	*	*	*	Analogue
[18]	0.35µm	125	3.3	21	19/1	0~19	35	*	*	Digital
[19]	1.2 µm	18	3	*	60/2	*	*	*	*	Digital
[20]	0.35µm	95	3.3	32.7	70/3	-30~40	-1.96	0.61	*	Digital
[21]	0.8µm	15	5	25	14/1	-2~12	*	*	*	Digital
[22]	0.35µm	246	3	27	60/3	-15~45	-4	*	<15	Digital
[23]	0.18µm	20	1.8	13.28	60/3	0~60	*	*	*	Digital
[24]	0.25µm	18	3.1	18.7	24/2	*	*	*	*	Digital
[25]	0.18µm	140~270	1.8	11.8	75/3	-15~60	14.38	-2.35	12.5	Digital
This work	0.35µm	80~300	±1.5	0.5	22/2	38~ 60	-9.5	-19.5	18	Analogue

Table 3. Performance comparison of this work and previously reported VGAs

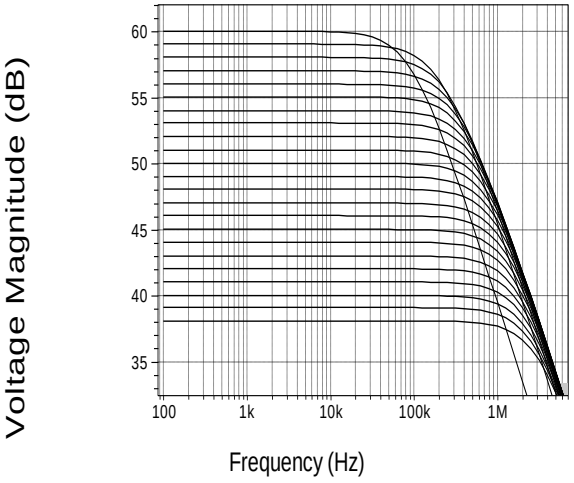

Figure 11: Two-stage VGA gain response for 38 dB to 60 dB in 1 dB steps

4. CONCLUSION

This work presents a novel design of a 220MHz VGA with 22 db of gain range. The architecture is based on a differential pair stage with voltage to current (V-I) converter, in which the gain is varied by changing the input voltage (V_{in}) from -1V to 0V. The variation of bandwidth is between 80 MHz and 300 MHz. Behavioural simulation indicated that the proposed design achieves the desired gain range of 22 dB in 1 dB gain steps and consume a minimum power of 0.5mW.

The design technique proposed in this paper combines better performance with simplicity of design and suitability of low energy. These parameters are very important in order to design Sigma-Delta ADC converter

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