Temperature effects on Threshold Voltage and Mobility for Partially Depleted SOI MOSFET

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ABSTRACT
As the channel lengths of conventional planar metal oxide semiconductor field effect transistor (MOSFET) shrink into the nano meter regime, performance of the devices becomes degraded mainly because of short channel effects. The nano range silicon on insulator metal oxide semiconductor field effect transistors (SOI-MOSFET) with Multi gate around the silicon channel can significantly improve the short channel effects and are therefore considered to be promising candidates for the next generation.
In this paper a detailed investigation of short-channel effects in advanced partially depleted SOI N-MOSFETs is done, which shows SOI devices from the same wafer can behave as fully or partially depleted according to the channel length. This paper Comprise the Low temperature behavior of threshold Voltage and Mobility for Partially Depleted SOI MOSFET.

Keywords
Partially Depleted SOI MOSFET, Low Temperature effects, conclusion.

1. INTRODUCTION
The Increasing demand for high data rate (over 1 Gb/s) opened new opportunities in the high performance range for CMOS. The benefits of a continuous pace in CMOS performance improvement due to aggressive device scaling *and* high isolation between the substrate and the active region can push forward silicon-on- Insulator (SOI) technology to be a promising choice for high-speed/high-frequency and very low power of system-on-chip integrated circuits [1], [2]. Partially depleted (PD) SOI technology is particularly attractive to address design of digital *and* analog/RF functions on the same chip, increasing high-performance and low-cost requirements for mobile and consumer applications.

SOI is a very promising technology for high performance integrated circuits, especially applicable for low-voltage, low-power and high-speed digital systems[3]. As compared to bulk silicon, the architecture of SOI MOSFETs is more flexible because more parameters such as thicknesses of film and buried oxide, substrate doping, and back gate bias can be used for optimization and scaling. It is also well known that the short-channel effects are remarkably reduced in SOI Technology.

2. PARTIALLY DEPLETED SOI MOSFET
The structures of SOI devices are not much different from bulk CMOS. An insulation layer is inserted underneath the device on the silicon substrate. This insulation layer introduces lower coupling capacitance from the conducting channel to the substrate compared to a bulk CMOS. The benefits of an SOI MOSFET also include higher current drive producing smaller delays, since doping-free channels have slightly higher mobility [4]. A buried oxide insulation layer minimizes current leakage from the drain/source junction to substrate. This renders the SOI MOSFET an outstanding silicon device applicable for high-speed and low-power applications.

Two types of SOI MOSFETs are generally used, partially and fully depleted SOI MOSFETs. applications.

A fully depleted SOI MOSFET has a thinner top silicon layer, so the channel is completely depleted of the majority carriers Hence, the SOI layer is much smaller than the depletion width of the device and its potential is tightly controlled by the gate. That means that there is no neutral region of the body of the MOSFET that can be charged. The advantage of FD SOI MOSFET include the elimination of the floating-body effect and better short channel behaviour. (Fig 1)

For Partially Depleted SOI device, the SOI layer thickness is thicker than the maximum depletion width of the gate. Usually the silicon film thickness is more than 50nm, which alleviates the constraint on device threshold voltage and its sensitivity (Fig 2), Also PD SOI devices make the manufacturing easier and the process and device design are much more compatible than with traditional bulk CMOS. In general, PD SOI device is optimal for high speed and is being targeted for applications where highest clock rates are needed. However the major issue of the partially depleted device is the floating body effect.

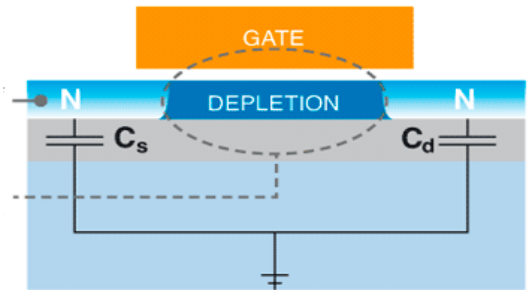

Figure 1: Fully Depleted SOI-MOSFET Structure

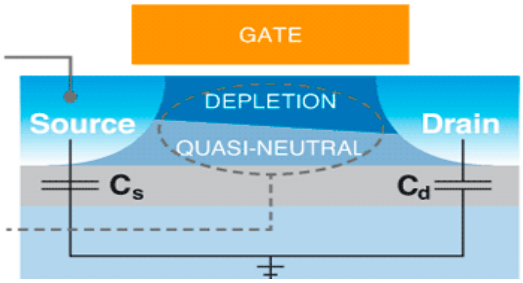

Figure 2: Fully Depleted SOI-MOSFET Structure

3. LOW TEMPERATURE EFFECTS

Threshold Voltage V_{th} and mobility parameters od a transistors depend on temperature. As the temperature decreases Device performance improves and as temperature Increases, the device performance degrades. As the Temp decrease mobility and V_{th} increase, junction leakage current and off-state power consumption decrease [5]. At low temperatures, the depletion region expands and therefore a PD transistor can convert to FD mode [6].

Study is done in the temperature range 77–400 K to investigate the performance as a function of temperature.

3.1 Effect on threshold Voltage

The threshold voltage increases at low temperature due to the increase in Fermi potential φ_F, depletion charge [6]:

$$\frac{dV_{th}}{dT} = \frac{d\phi_F}{dT}\left[\alpha\sqrt{\frac{q\varepsilon_{si}N_{eff}}{\phi_F C_{ox}^2}} + 2 + \frac{qD_{it}}{C_{ox}}\right] \quad (1)$$

where ϵ_{Si} and q are the silicon permittivity and electron charge; a = 1 for partially depleted devices and a = 0 for fully depleted transistors. Eq. (1) predicts that not only does V_{th} increase when the temperature decreases, but also the slope of this variation depends on whether the device works in a FD or PD mode.

Fig.3 show interesting features. The Behavior of V_{th} at low temperature is not the same for channels of different lengths. For a long device (L_g = 1um), a change in the slope dV_{th}/dT is observed at 300 K reflecting the transition from PD to FD mode.. For very short channels nano meter length range (L_g = 40 nm), the transition region shifts to lower temperature range (140 K). The second effect of the pockets is seen in the PD linear region (140 K < T < 300 K), where the slope dV_{th}/dT is higher for the shorter channel (L_g = 40 nm). This is explained by including in Eq. (2) the variation of N_{eff} versus gate length, the effective doping level being higher in short channels.

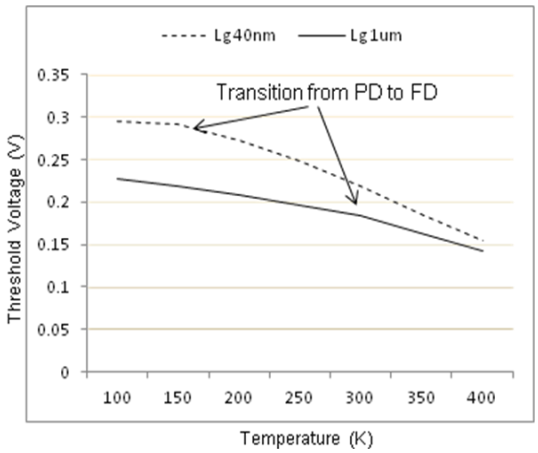

Figure 3: Threshold voltage Vs Temp Characteristics

The slope of $V_{th}(T)$ was Analyzed for different gate lengths at proper range of temperature.

Finally, it should be noticed that all transistors exhibit roughly the same slope dV_{th}/dT when working in FD mode. The reason is that N_{eff} becomes irrelevant in Eq.(1) for a = 0. The threshold voltage behavior can be explained by considering (i) the difference in effective doping between long and short devices [7], and (ii) the extension of the depleted region X_d at lower temperatures [6]:

$$X_d = \sqrt{\frac{4\varepsilon_{si}\phi_F}{qN_{eff}}} \quad (2)$$

As we know that the Fermi potential φ_F increases by lowering the temperature [6]. In the depletion region, all impurities are ionized by field effect. As a result, the depletion region extends as the temperature decreases. We now consider the pocket-induced difference in effective doping between short and long channels:

N_{eff} (Long) < N_{eff} (Short) => X_d (Long) > X_d (Short)

As the temperature decreases, the depletion region X_d(long) reaches t_{Si} (Si film thickness) before X_d(short). Short channel devices are more partially depleted than longer ones and become fully depleted at a lower temperature. We can also calculate the effective X_d for several gate lengths with the help of Eq.(2).

3.2 Effect on Mobility

The mobility defines with the help of different scattering mechanisms. In SOI MOSFETs the prevailing mechanisms are Coulomb scattering, phonon scattering and surface roughness scattering [8]. The surface roughness scattering is independent of temperature [9] but Coulomb and phonon scattering have opposite variations with temperature [10,11]

$$\mu_{ph}\alpha T^{-x} and \mu_c \alpha T \quad (3)$$

where x = 1 for the low-temperature range (77 K <T< 100 K) and x = 1-1.5 for higher temperatures (100 K < T < 450 K).

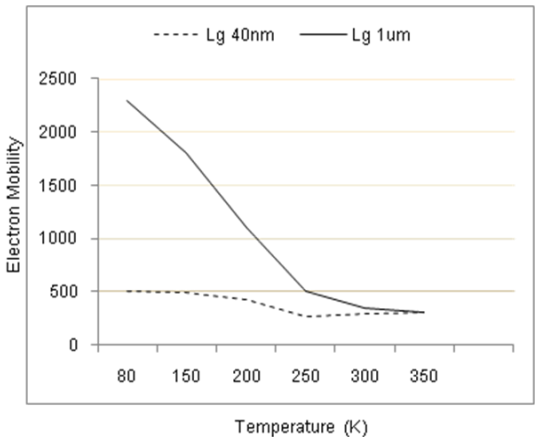

Figure 4: Mobility Vs Temp Characteristics

The function $Y(V_g)= I_d/ \sqrt{g_m}$ is used to find the mobility. The advantage of this method is to eliminate the first order effect of the series.

For long channels, the mobility variation follows the phonon scattering law, with x = 1.5 for high temperature range and x = 1 for low temperature range. The mobility reaches an excellent value (2200 cm^2/V-s) at 77 K. The mobility is limited by phonon interactions due to lower Doping in long channel Transistors. For short devices, the gain in mobility at low temperature is reduced. Coulomb scattering is enhanced by the high doping level. The theoretical curve in Fig. 4 was calculated with the Matthiessen rule

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} \qquad (4)$$

Assuming $\mu_c \alpha T$ and $\mu_{ph} \alpha T^{-1.5}$ (with μ_c =3.6. 10^3 cm^2/V s and μ_{ph} = 365 cm^2/Vs at 300 K).

4. CONCLUSION

The Structure / electrical properties of 'partially depleted' SOI MOSFETs have been studied in this paper.

For Partially Depleted SOI device, the SOI layer thickness is thicker than the maximum depletion width of the gate. Also PD SOI devices make the manufacturing easier and the process and device design are much more compatible than with traditional bulk CMOS.

Threshold voltage and mobility will be more for lower temp transistor (for a particular Gate length), OR we can say that Threshold voltage and Mobility improves at Low Temperature. It is clear from the Graphs of threshold voltage and mobility that transition from PD to FD mode occurs at a specific temperature which depends on the gate length. Long channels reach into full depletion mode at a higher temperature as compare to short channels.

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