MATLAB based Analysis and Simulation of Multilevel Inverters

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ABSTRACT
The objective of the present work is to obtain a three level ac output, which is obtained by a 3-phase, 3-level multi level inverter. An inverter receives dc supply for its input and produces ac output. Here the dc input to the multilevel inverter is obtained by a single-phase un-controlled full wave rectifier. 230 V, 50 Hz single-phase ac supply is directly taken from supply mains, stepped down to 48 V by a step down transformer and is rectified by the rectifier circuit. Using a simple L-C filter at the rectifier output terminals the obtained dc supply can be made ripple free. The rectifier circuit consists of 4 number diodes and in each half cycle a pair of diodes conduct and pulsated dc obtained and finally rectified to obtain a pure dc. The obtained dc from the rectifier is directly fed to the multi level inverter. The switching sequence of switches used in the multilevel inverter inverts the dc input and a 3-phase, 3-level ac output is obtained. Simulation of the firing pulse generation circuit and multi-level inverter was done using MATLAB 7.5 and Simulink.

Keywords
Multi-Level Inverter, Matlab, Simulink, PWM, Diode Clamping.

1. INTRODUCTION
The multilevel inverters [4] have drawn tremendous interest in the power industry. They present a new set of features that are well suited for use in reactive power compensation. It may be easier to produce a high power high voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure [6]. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase the power rating of the overall circuit [2]. As the no of voltage levels increases the harmonic content of the output voltage waveform decreases significantly

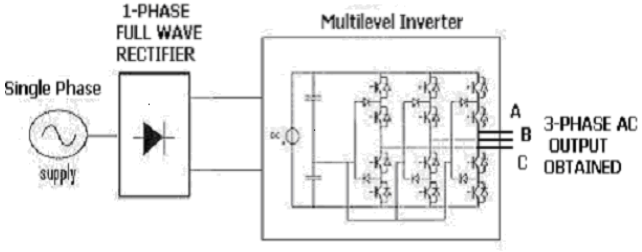

Fig 1: Block Diagram of 3 Level Diode Clamped Inverter

Here the dc input to the multilevel inverter is obtained by a single-phase uncontrolled full wave rectifier. 230 V, 50 Hz single-phase ac supply is directly taken from supply mains, stepped down to 48 V by a step down transformer and is rectified by the rectifier circuit. Using a simple L-C filter at the rectifier output terminals the obtained dc supply can be made ripple free. The rectifier circuit consists of 4 number diodes and in each half cycle a pair of diodes conduct and pulsated dc obtained and finally rectified to obtain a pure DC [3].

To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require various pulse width modulation (PWM) strategies [1], which increase the switching frequency of the power devices. In the case of multi level inverters, as the number of voltage levels increases the harmonic content of the output voltage waveform decreases, even without using any pulse width modulation technique. As the switching frequency is reduced the power losses are also minimized, and thereby increasing the efficiency of the system.

Since the early years high power line commutated thyristors in conjunction with capacitors and reactors have been employed in various circuit configurations to produce variable reactive output. Using appropriate switch control the VAR output can be controlled continuously from maximum capacity to maximum inductive output at a given bus voltage.

2. SIMULATION ANALYSIS
The switching states of the lookup table shown in table 6.1 can be obtained from the repeating sequence stair available in the sources block. Here the DC voltage of 80 v has been split into two 40 V battery sources. The output voltages are taken across the resister of 1000 ohms.

Table 1: Switching Sequence

Phase Voltages			Line Voltages			Switch States Leg 1				Leg 2				Leg 3			
V_{a0}	V_{b0}	V_{c0}	V_{ab}	V_{bc}	V_{ac}	S_1	S_2	$S1'$	$S2'$	S_1	S_2	S_1'	$S2'$	S_1	S_2	S_1'	$S2'$
0	$-V_{d/2}$	$V_{d/2}$	$V_{d/2}$	$-V_d$	$-V_{d/2}$	0	1	1	0	0	0	1	1	1	1	0	0
$V_{d/2}$	$-V_{d/2}$	0	V_d	$-V_{d/2}$	$V_{d/2}$	1	1	0	0	0	0	1	1	0	1	1	0
$V_{d/2}$	0	$-V_{d/2}$	$V_{d/2}$	$V_{d/2}$	V_d	1	1	0	0	0	1	1	0	0	0	1	1
0	$V_{d/2}$	$-V_{d/2}$	$-V_{d/2}$	V_d	$V_{d/2}$	0	1	1	0	1	1	0	0	0	0	1	1
$-V_{d/2}$	$V_{d/2}$	0	$-V_d$	$V_{d/2}$	$-V_{d/2}$	0	0	1	1	1	1	0	0	0	1	1	0
$-V_{d/2}$	0	$V_{d/2}$	$-V_{d/2}$	$-V_{d/2}$	$-V_d$	0	0	1	1	0	1	1	0	1	1	0	0

For the switches S1, S2, S3 and S4 the switching pulses are to be given. These switching pulses are drawn from a PWM generating circuit which is according to the behavior of the main circuit [5]. The characteristics required are:

1. Frequency of voltage applied at the inverter terminals should be same as the frequency of the source voltage. For this to happen, PWM is generated taking reference from source voltage.
2. The switching pulses should be given such that the resultant waveform should have average values for each pulse resulting in a sinusoidal waveform.
3. One pair of switches has to give switching pulses while the other pair has to be in idle state or off state.

For PWM to have the first characteristic a sample has to be taken from the source itself for frequency. For the second characteristic to be satisfied we need to use a signal generator and the best source of sine wave that can be thought of is the source waveform itself. So the source voltage waveform is selected as reference.

The source voltage waveform is obtained by using a voltmeter at the source. A transport delay block is used for getting a delay between source voltage and Inverter voltage. The output of the delay block is given to PWM sub circuit

In PWM sub circuit we used a block provided by MATLAB. This block will give the pulses with duty cycle proportional to the instantaneous value of the reference.

Duty Cycle = $\frac{V+1}{2}$

Where V is the instantaneous value

(i.e.) when V is negative, duty cycle <50%

When V is positive, duty cycle>50%

When V is zero, duty cycle = 50%

But the voltage waveform of source starts from the instantaneous value zero. For instantaneous value '0' the duty cycle will be 50% which is undesirable. So a waveform has to be generated such that, for voltage waveform starting at 0 another waveform has to start at 1 corresponding to the original waveform. PWM input has to reach peak with the source waveform and has to reach -1 when source waveform reaches 0. This is followed by the source expression "-cos2θ". So we squared the source waveform by using the multiplication block. Then remove the DC offset half by subtracting the above result with half. Then we multiplied it with a gain two because the waveform is now which is having half the amplitude required. So when a gain of two is applied it becomes - cos2θ. Now this can be used as reference to the PWM block provided by the MATLAB.

Now we need to separate the switching pulses for the pair of switches S1, S4 and the other pair S2, S3 so as to follow the 3rd characteristic. For this, we developed a circuit where one output is a square waveform. This reaches +1 during the positive half cycle of source waveform and reaches 0 during the negative half cycle of the waveform. The other output is vice versa of the above i.e., it will reach 0 for the positive half cycle of the source waveform and reaches +1 for the negative cycle of the waveform.

The first output is multiplied with the PWM pulses and is given to the pair S1, S4 switches. The second output is multiplied with the PWM pulses and is given to the pair S2, S3 switches. This is how PWM is being generated.

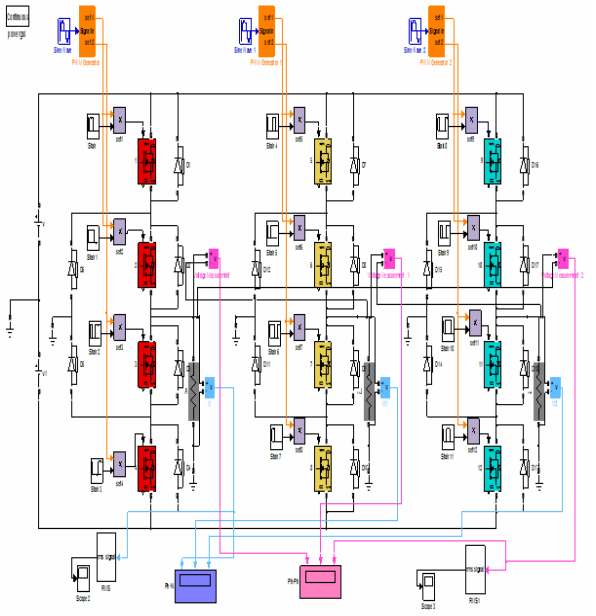

Fig 2 Simulink model for three leg operation of a 3 level diode clamped multi inverter for achieving PWM

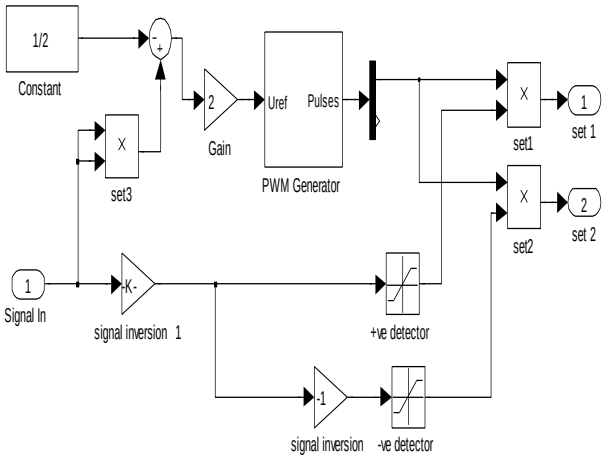

Fig 3: PWM Generator Circuit

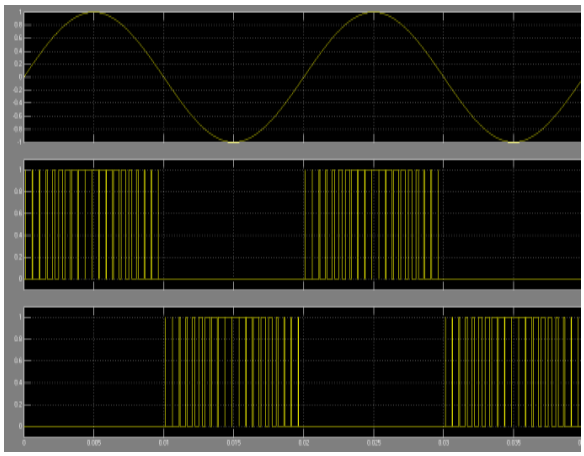

Fig 4: PWM Generation for A Reference Wave (Sine Wave)

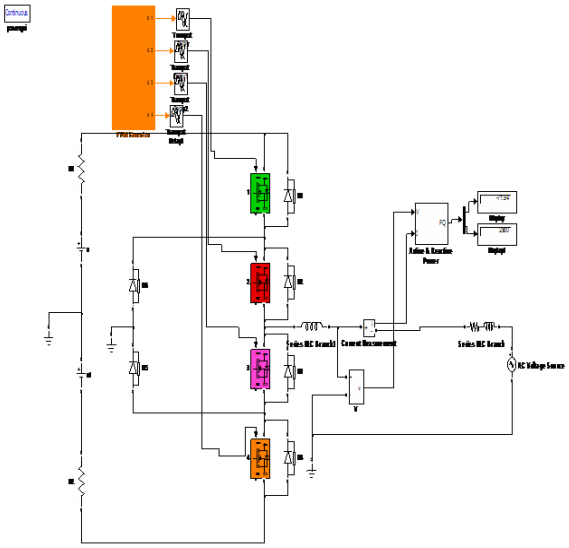

Fig 5: Simulink model for Reactive Power Compensation for Single Leg Using PWM Technique

4. RESULTS

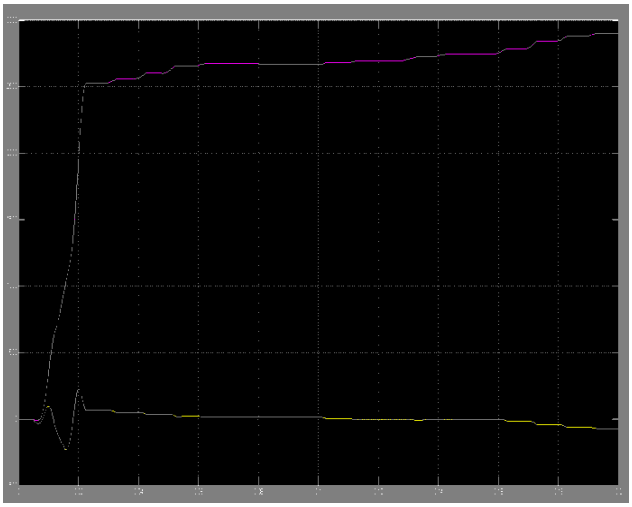

Fig 6: Active and reactive power graph for the reactive power compensation for single leg of 3 level inverter

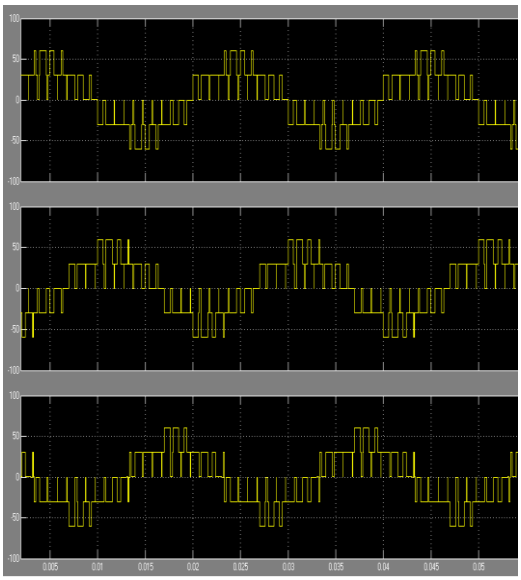

Fig 7: Phase to phase voltage of a simulated 3 level diode clamped multi inverter with PWM

Table 2: Reactive Power compensation studies

Delay	Inverter		Source		balance	
	P	Q	P	Q	P	Q
1	0.26	320.4	99.7	-220.5	99.96	99.9
5	-62.97	377.9	162.9	-278	99.93	99.9
10	-90.54	453	190.4	-353.1	99.86	99.9
355	106.8	259.6	-6.982	-159.7	99.818	99.9
350	138	183.4	-38.04	-83.46	99.96	99.94

3. CONCLUSION

Reactive power compensation using three-level inverter has been achieved. This is achieved by using PWM generation block and by changing the transport delay. It is observed that by changing the delay, the reactive power obtained from the inverter changes depending on the reactive power drawn by the load.

4. REFERENCES

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