# Implementation of FIR Filter and FFT Systems on a STRATIX-III FPGA Processor

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## **ABSTRACT**

In this paper, the implementation of DSP modules like FIR Filter and FFT based systems are designed and implemented. The design is based on high performance FPGA "Cyclone II" and implementation is done after functional and timing simulation. The simulation tool used is ModelSim. The tool for synthesis and implementation is Quartus II. The experimental results shows the functional and timing analysis for all the DSP modules carried out using high performance synthesis software from Altera.

Keywords: Simulation, FPGA, Code Conversion

## 1. INTRODUCTION

This paper specifies the design analysis and simulation aspects of an N tap FIR filter, direct form FIR filter and FFT based computational systems. An N tap FIR filter is described by the following equation  $y(n) = \sum x(n) *h(n-k), 0 \le k \le N-1$  the Coefficients are generated using FIR Compiler tool. Direct form FIR structure is implemented in pipelined and iterative form Filter structure is implemented in a modular form.FFT reduces the computation time required to compute DFT and improves performance by a factor of 100 over the direct evaluation of DFT.To compute all values of N requires N2 complex multiplications and N\*(N-1) complex additions.FFT reduces the number of complex multiplications and additions to N/2(log2N-1) multiplications and N(log2N)additions. In DIT algorithm the input is in bit reversed order and output is in natural order. The main advantages of these implementations are, it is very easy to interface with the special purpose DSP processor and also it is easy for cascading. The FIR filter structure is implemented in a modular form.

#### 2. BLOCK SCHEMATIC

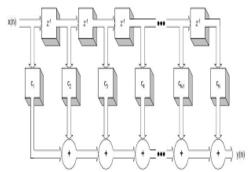


Figure 1 Block diagram of FIR filter-cascaded.

In this section the FIR filter is implemented on a FPGA as a fully parallel implementation and is called as a pipelined FIR

filter, which has the ability to perform 60 operations in a single clock cycle. The block diagram shown below is pipelined FIR filter.

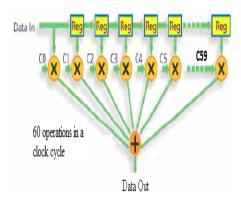


Figure 2 Block diagram of FIR filter-pipelined

# 3. FLOW DIAGRAM

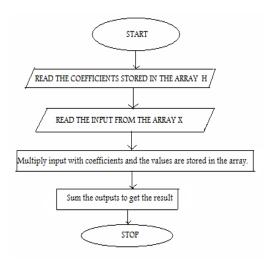


Figure 3 Flow chart FIR filter-pipelined

According to the above flow diagram a software routine is developed and accordingly the simulation is carried out using Quartus II software. The target device selected is Stratix III.The functional and timing analyses were carried out. The maximum frequency obtained is 247.65MHz.

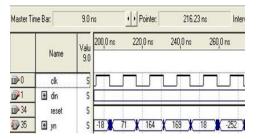


Figure 4 Simulation results of pipelined FIR filter

#### 4. SERIAL FIR FILTER

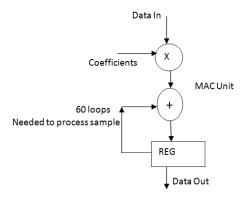


Figure 5 Block diagram of serial FIR filter

In this section the FIR filter is implemented on a FPGA as a serial implementation and is called as a serial FIR filter, which takes 60 loops in a single clock cycle, which is needed to process the sample. The flow diagram of the serial FIR filter approach is as shown below.

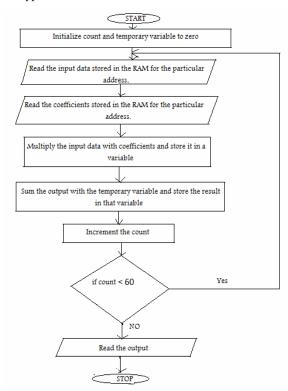


Figure 6. Flow chart of serial FIR filter

In the above flow diagram the iterative implementation of the FIR filter is carried out. Accordingly the software routine is written in VHDL programming language, for which the functional and timing analysis results are generated which are shown as in the figure given below.

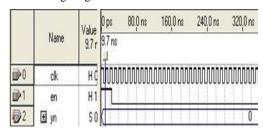


Figure 7. Simulation results of Serial FIR structure

#### 5. FIR STRUCTURE

Filter structure is implemented in a modular form. Advantages are it is easy to interface with processor. Further the advantage involves that it is easy for cascading operation. The figure 8 shows the RTL schematic block of FIR filter, this block specifies the register transfer levels at the different stages in the schematic structure.

## 6. FAST FOURIER TRANSFORM (FFT)

The DFT of a sequence can be computed using the following formulae.

 $X(k) \!\!=\!\! \Sigma x(n) e_{\text{-}j2\,\Pi\,nk/N}\, 0 \!\!\leq\!\! k \!\!\leq\!\! N \!\!-\! 1$  ; n=0 to N and  $W_N \!\!=\!\! e_{\text{-}j2\,\Pi/N}$ 

CooleyTukey DIT algorithm is used for the implementation of 128-point FFT. FFT reduces the computation time required to compute DFT and improves performance by a factor of 100 over the direct evaluation of DFT.To compute all values of N requires N2 complex multiplications and N\*(N-1) complex additions.

The simulation is carried out using Quartus II software. The target device selected is Stratix III. The functional and timing simulations were carried out. The output is obtained after 156 clock cycles. The maximum frequency obtained is 164.77 MHz's.

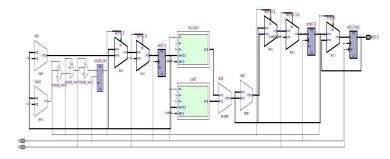


Figure 8. RTL Schematic of serial FIR filter

#### 7. MATLAB RESULTS

In this the model based design approach is provided for an integrated workflow. This model based design speeds up the algorithm development with a unified design environment. Automates the manual steps in FPGA implementation to enable shorter iteration cycles from the MATLAB environment.

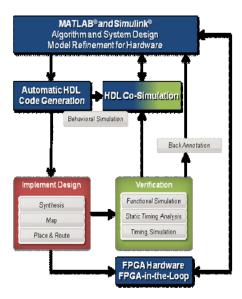


Figure 9. Mapping diagram of MATLAB to FPGA.

In this section the computational simulation of FFT implemented in QUARTUS Stratix-II VHDL environment is as shown in below figure

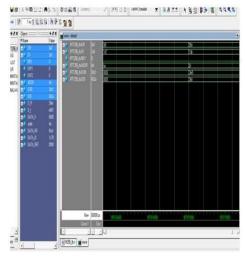


Figure 10. Simulation of FFT Computational analysis.

Further the two simulation results of FFT are obtained in MATLAB are as shown below.

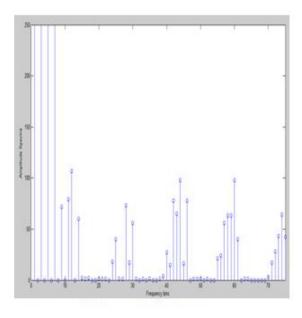


Figure 11. Simulation of FFT in MATLAB for mapping on to the FPGA.

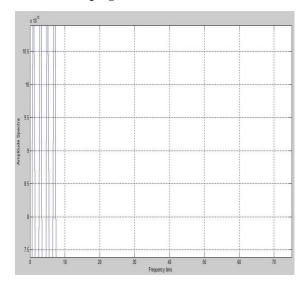


Figure 12. FFT Simulations in MATLAB.

# 8. CONCLUSIONS

In this paper the implemented DSP modules are FIR filter and FFT based computational systems. All these DSP modules are designed from the block diagram approach to the synthesis and simulation aspects. The functional timing analysis results and the synthesis results are measured in precise and accurate manner. Finally the simulation waveforms are obtained in the FPGA simulation tools and the simulation waveforms are verified with the hardware design aspects, and matching results are obtained. The filter structure is implemented in a modular form. All the simulations are carried out in the Quartus-II software. The target device selected is Stratix-III.The functional and timing analysis for all the modules are carried out and accurate measurements are obtained.

## 9. REFERENCES

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