VHDL-AMS modelling and Optimization of a Fractional-N Synthesizer with experiment Designs

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ABSTRACT
In this work, we expose our approach to design and optimize mixed analogue and digital systems at a high level description using the hardware description language VHDL-AMS. Many statistical experimental design methods are employed in optimization. We apply Hocke_D4 experimental designs with five parameters in order to minimize the lock time and the spurious level of a fractional-N synthesizer acting as a direct MSK modulator and designed for the DECT standard application.

General Terms
Computer aided design, Hardware description language, VHDL-AMS, PLL.

Keywords
Hierarchical design, VHDL-AMS description, MSK modulator, Fractional-N synthesizers, Optimization, Experimental designs, lock time, spurious level.

1. INTRODUCTION
The need for new analogue synthesis techniques to support a future high-level mixed-signal synthesis environment is increasing along with the advancement in technology and the evolution of commercial requirements. The emergence of VHDL-AMS since 1999 [1] has provided a platform which can form the basis for high-level analogue and mixed-signal synthesis systems. Many efforts are focused on the development of new methodologies to integrate the Top-Down hierarchical design flow in a synthesis environment using VHDL-AMS [2].

So far, electrical simulators like SPICE or ELDO have been the most widely used simulation tools. Abstraction level is low whereas accuracy level is high since accurate device models are used. However, CPU time grows with the circuit size and the type and length of simulation. There is no doubt that electrical simulation is the logical choice for simulating basic cells. The situation changes considerably when dealing with more complex systems.

An efficient solution consists of using behavioral simulation. This approach requires the circuit to be partitioned into basic blocks and described by using a behavioral description language. A set of explicit expressions relates the output variables with the input and internal state variables of each block. Thanks to this high level description approach, behavioral simulators can perform long transient analysis in reasonable CPU times while maintaining a satisfactory accuracy level. At this level, it is possible to achieve an optimized topology before passing to transistor sizing [3].

A VHDL-AMS description for our studied system, the MSK modulator, allows the verification of its performances and permits to ensure the correctness of the design, especially to check circuit operation over range of process and environment variations.

Direct modulation of fractional-N synthesizers acting as transmitters has become an active area of research. A key limitation in such systems is that the low-pass filter response of the synthesizer dynamics causes inter-symbol interference in the transmitted data. Techniques have recently emerged that focus on increasing synthesizer bandwidth [4-5].

An MSK modulator based on fractional-N synthesizer is a multivariable system. The traditional 'one-factor at a time' technique used for optimizing such system does not only consume time but also often easily miss the alternative effects between components. Furthermore, this method requires carrying out a number of experiments to determine the optimum levels, which are untrue. These drawbacks of single factor optimization process can be eliminated by optimizing all the affecting parameters collectively by experimental design using response surface methodology. For this reason, we apply this technique to optimize the performances of our modulator.

This paper is outlined as follows. In section 2, we detail the high level description of the MSK modulator. In section 3, we present the optimization result of the modulator with experimental designs. Section 4 draws a conclusion.

2. HIGH LEVEL DESCRIPTION OF THE MSK MODULATOR
Antonio Calaci et al. demonstrates in [6] the benefits of systematic circuit analysis and optimization applied at different abstraction levels. Since both, systematic sizing approaches and statistical analysis, require many simulations, they apply a hierarchical approach with different levels of simulation and accuracy from system to transistor level to balance the tradeoff between time and accuracy. All sizing and optimization steps are driven by WiCkeD [7], an EDA environment independent tool for circuit analysis and sizing. WeiCkeD does statistical optimization with a unique deterministic worst-case distance algorithm. Antonio Calaci chooses a double ring oscillator consisting of a Main PLL and Dither PLL as example to demonstrate the efficiency of his proposed methodology.

In [8], Guo Yu et al. proposes Yield-Aware hierarchical optimization of a phase locked loop. The PLL is described in Verilog-A. Guo Yu focuses on the optimization of the VCO, the charge pump and the filter. The hierarchical optimization uses building block pareto performance models. He faces two fundamental difficulties in achieving such a methodology: yield-aware pareto performance characterization at the building block level and yield-aware system-level optimization problem formulation.

In [9], Dean Banerjee et al. discusses different techniques that can be used to find the best theoretical optimal solution for the design of the loop filter of a PLL and then satisfy the tradeoff between the PLL lock time and the spurious level. Dean Banerjee exposes a new approach for the loop filter design and optimization, which is applied to develop a software application called "Easy PLL".

With Easy PLL, designers enter system requirement, select a PLL and a VCO and enter the required performances. The software calculates then the loop filter component values. If the lock time or the spurious level is missed, designers change the loop filter order.

M. Henderson Perrott uses VppSim software environment to compute the PLL parameters [10]. VppSim provides a software framework that supports Verilog and C++ co-simulation within the Cadence environment. VppSim therefore provides a top-down design methodology in which designers start at the highest level with CppSim modules, and then gradually build more granular models using Verilog and Spectre. Designers can also benefit from the ability to convert CppSim systems created within Cadence into Matlab or Simulink functions.

In our case, we use the hardware description language VHDL-AMS to describe and simulate our system. We verify its stability and then optimize its lock time and spurious level. The hierarchical design flow we adopted is detailed in figure 1. First, specifications are translated into a VHDL-AMS description with the help of a VHDL-AMS library. In our case, we simulate the developed description in Simplorer software. An optimization algorithm based on experimental designs helps to converge to an optimal solution with Nemrodw software.

Different simulations and characterizations in Simplorer 7.0 software allow the verification of the required performances. Then, a transistor level description is developed taking into consideration the performed optimal solution. The digital part is synthesized with RTL Compiler Software [11]; both the analogue and the digital parts are then simulated in Virtuoso software [12].

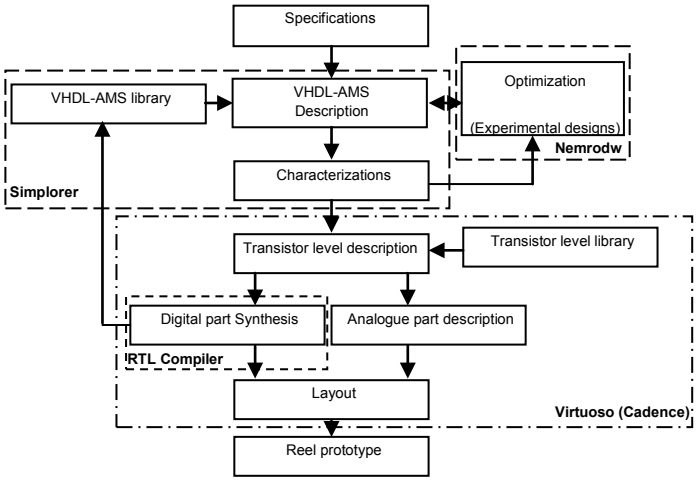

Figure 1. Hierarchical design flow

Figure 2 shows the block diagram of the studied MSK modulator [13-14]. It is a mixed system composed of both analogue and digital parts. It is based on a fractional-N frequency synthesizer directly modulated at high data rate with a ΣΔ modulator. This technique achieves good noise performance. In fact, it allows digital phase/frequency modulation to be achieved at high data rates without mixers or D/A converters in the modulation path.

The synthesizer is implemented as a phase locked loop (PLL). To achieve good noise performance with a simple design, the PLL bandwidth is set to a low value relative to the data bandwidth. To illustrate our optimization approach, the described modulator is used to build a 1.77GHz to 1.9 GHz transmitter using Gaussian Frequency Shift Keying (GFSK), respecting the DECT standard [14].

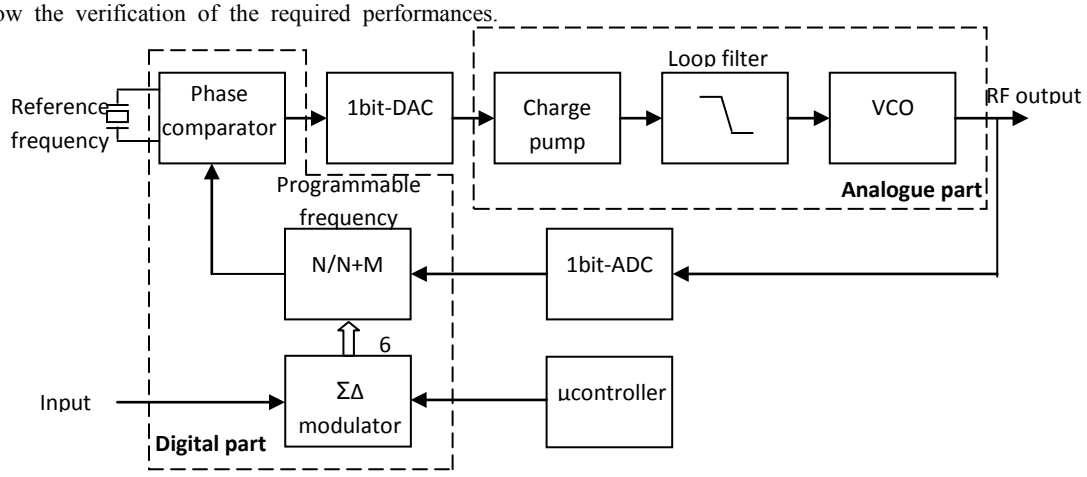

Figure 2. Block diagram of the FSK modulator

2.1 Digital part modelling

The digital part of the modulator contains a phase frequency detector (PFD), a Sigma Delta modulator and a N/N+M frequency divider. The PFD topology is depicted on figure 3. It is mainly composed of RS flip flops and NAND gates. It is described with a VHDL code.

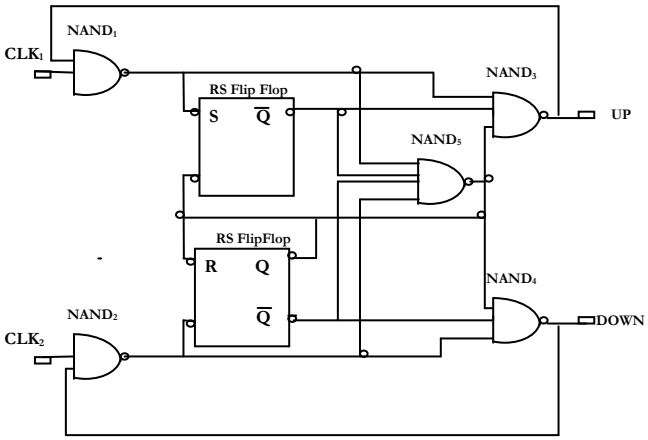

Figure 3. The phase frequency detector topology

The reference frequency F_{REF} of the MSK modulator is fixed at 20MHz. To achieve an output frequency varying between 1,77GHz and 1,9GHz, the frequency divider ratio should vary between 88.5 and 95.

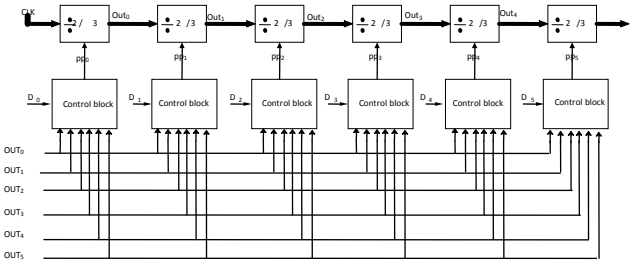

Figure 4. The frequency divider topology

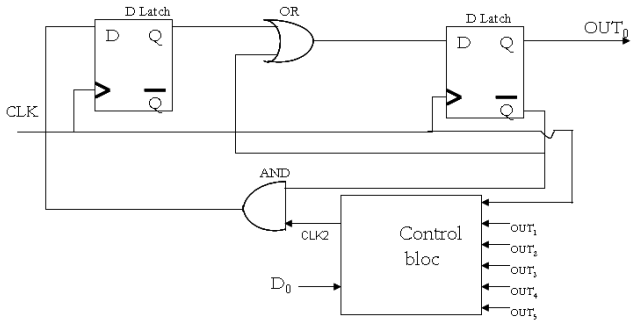

Figure 5. The 2/3 divider bloc topology

The designed frequency divider topology is shown in figure 4. It uses six 2/3 divider blocs driven by six control blocs. The 2/3 divider topology is detailed on figure 5. It is composed of two D-latches, OR and AND gates. When the input D_i is low, the CLK frequency is divided by 2. Whereas, when D_i is high, the frequency is firstly divided by 3 then by 2 as shown in figure 6. We can then verify that the frequency division ratio N varies between 64 and 127, depending on the 6 inputs D_i as [13]:

$$N = 2^6 + 2^0 D_0 + 2^1 D_1 + 2^2 D_2 + 2^3 D_3 + 2^4 D_4 + 2^5 D_5$$

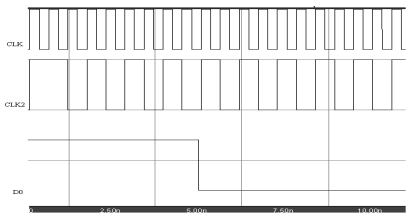

Figure 6. The 2/3 divider simulation

The designed Sigma Delta modulator is a third-order modulator as shown in figure 7. It is composed of a 6-bit ADC (typically known as a comparator) driven by the output of an integrator fed with an input signal summed with the output of a 1-bit DAC fed from the ADC output.

The integrator constantly ramps up or down at node 1, which feeds the comparator or 1-bit ADC. The output of the 1-bit ADC controls the ones-density that is fed back through a 1-bit DAC, which creates an average output voltage at node 2 at the rate of the sampling frequency f_S. This average voltage is then forced to be equal to V_{IN} by the summing point. As the input signal increases, the number of "ones" in the serial bit stream increases, whereas the number of "zeros" in the serial bit stream decreases. Conversely, as the input signal goes negative, the number of "zeros" in the serial bit streams increases, however the number of "ones" decreases. Simply, the average value of the input voltage is contained in the serial bit stream of the comparator running at f_S. The 6-bit output signal of the ΣΔ modulator drives the frequency division ratio (D_i).

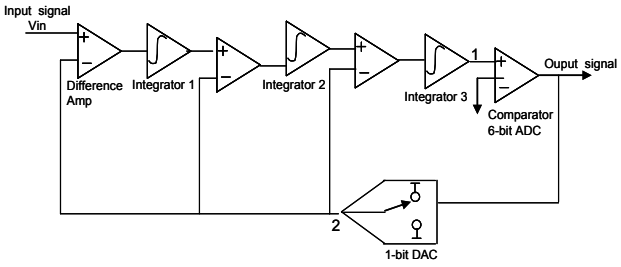

Figure 7. Third-order multi-bit ΣΔ modulator

All blocs constituting the frequency divider and the ΣΔ modulator are described with a VHDL code. The last is introduced in Virtuoso Digital implementation software which consists of a capacity-limited version of Encounter RTL Compiler with global synthesis technology. We run the Virtuoso Digital Implementation system to synthesize an RTL netlist as detailed on figure 8. We use the AMS 0.35µm CMOS technology. We extract information about the power consumption for each bloc. Table 1 shows that the synthesized digital part consumes 6.7 mW. This study will be helpful for the optimization of the modulator's performances.

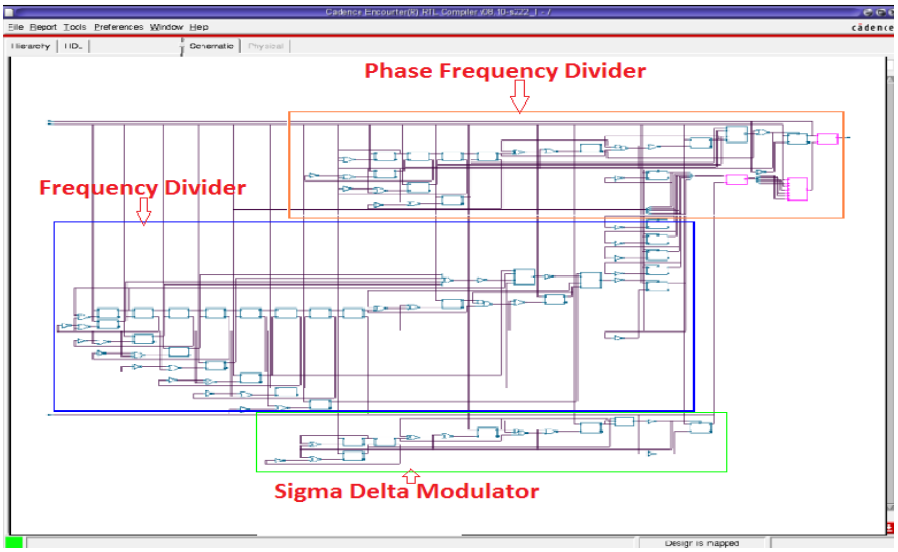

Figure 8. The synthesized RTL netlist

Table 1. Recapitulative power of digital part

Digital blocs	Cells	Leakege(nW)	Internal(µW)	Net(µW)	***Sum(µW)***
PFD	12	1.64	382.58	39.41	***421.99***
Frequency divider	863	87.98	3787.5	2245.45	***6032.9***
ΣΔ modulator	19	3.52	162.22	118.87	***281.09***

2.2 Analogue part modelling

The analogue part of the MSK modulator is composed of a charge pump, a loop filter and a Voltage Controlled Oscillator (VCO).

The design of the charge pump is critical for the achievement of high data rates since it forms the bottleneck in dynamic range that is available to the modulation signal. Figure 9 illustrates the topology we have considered in its design. To avoid distortion of the modulation signal, the variation in duty cycle should be limited to a range that allows the output of the charge pump to settle close to its final value following all positive transitions. The charge pump is described in VHDL-AMS. The developed model takes into account the dissymmetry error of the output current I_{CP} and the effect of transient times.

The loop filter consists of an active low pass filter whose transfer function is expressed as:

$$Z_F(f) = \frac{1}{j2\pi f C_2} \frac{1 + j\frac{f}{f_z}}{1 + j\frac{f}{f_p}} \quad (1)$$

where $f_p = \frac{1}{2\pi R C_1}$ and $f_z = \frac{1}{2\pi R(C_1 + C_2)}$ (2)

$f_Z < f_p$ to allow the PLL stability to be achieved.

To develop a high level description of the loop filter, relations (1) and (2) are introduced in a VHDL-AMS description.

The designed voltage controlled oscillator is an LC one. Its output frequency f_{out} is modeled by a second order polynomial model where A is a no linearity coefficient. It is extracted after a transistor level simulation of the VCO [15]:

$$f_{out} = f_0 + K_{VCO} * \left(V_{IN} + A * V_{IN}^2\right) \quad (3)$$

where f_0 is the VCO center frequency and K_{VCO} is its sensitivity.

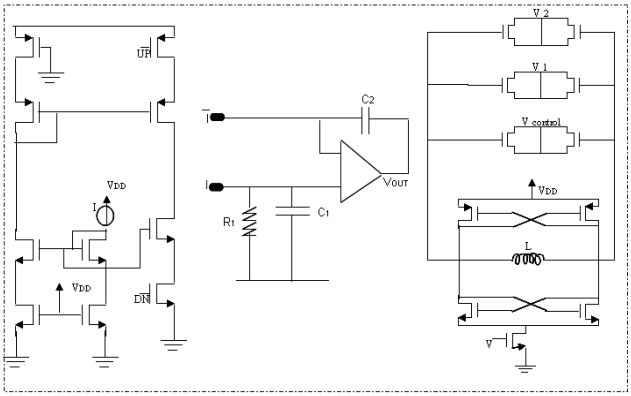

Figure 9. Analogue part topology

The VHDL and the VHDL-AMS codes describing respectively the digital and the analogue parts constituting the MSK modulator are associated to obtain a complete high level description of the modulator. It is simulated in Simplorer 7.0 Software [16]. Table 2 resumes the main parameters of the modulator. They are extracted with the help of CppSim system simulator. In fact, we enter the bandwidth of the PLL of the PLL and CppSim extracts the open loop parameters.

Table 2. The parameters of the modulator

Charge Pump current	I_{cp} = 1.5 µA
Loop Filter components	R = 416 kΩ, C_1= 3pF, C_2= 30pF
VCO characteristics	K_{vco} = 30 MHz/V, f_0=1810 MHz
Frequency reference	20 MHz
Frequency Divider	N= 90

At this step of study, the developed VHDL-AMS description allows the verification of the modulator performances and permits to ensure the correctness of the design. It helps the designer to achieve a first optimum topology. In our design methodology, this characterization is followed by an optimization step. Our target consists of extracting an optimal solution providing a faster modulator with a reduced spurious level. As the system is described in VHDL-AMS, and at this level of abstraction, we don't have fully implicit mathematical relationships to explain the PLL lock time and spurious level over the modulator parameters. Therefore, it is not possible to apply a traditional optimization method. We apply a special and specific method based on experimental designs.

3. Optimization with experimental designs

Recently, many statistical experimental design methods have been employed in optimization. They are based on experiments. We show in this paper that they can be applied to optimize electronic integrated circuits. The real experiments are replaced in this case by simulations.

The most frequent designs in optimization problems involving three or more factors are central composite ones, Box-Behnken designs, D-optimal designs, and others, such as Hoke designs [17]. Central composite designs and Box-Behnken designs are the most appropriate to detect curvatures in a multidimensional space, but require a large number of experiments beyond three factors. D-optimal designs are less frequent, but adequate in cases involving linear functions where the factors can only be varied over a restricted area, and thereby create an irregular experimental domain in which orthogonality cannot be achieved. Hoke designs are economical second-order designs based on irregular fractions of partially balanced type of the 3^k factorial for a number of factors $k \geq 3$.

In this work, we consider that the experimental region is a hypercube and we apply a five factor-Hoke-D4 design. Considering that the efficiency of any experimental design is defined as the number of coefficients of the model divided by the number of experiments, Hoke_D4 design is the most efficient compared to central composite, Box-Behnken or Doehlert designs. Hoke_D4 designs are also more efficient in mapping space: adjoining hexagons can fill a space completely and efficiently, since the hexagons fill space without overlap.

To find the optimum conditions for a high data modulation of the studied MSK modulator, the experimental designs as a function of selected main factors have to be determined. The lock time and the spurious level of the PLL frequency synthesizer are in trade-off relationship with each other. Since a PLL frequency synthesizer typically consists of many components, it is important to consider the possible variations of each component parameter to ensure a high quality manufacturing process. The following parameters have to be evaluated for the design of an optimal loop filter, necessary in the PLL prototyping stage: phase noise, spurious level, lock time, loop bandwidth and power consumption.

In this work, we optimize the spurious level and the lock time. The constraints consist of respecting the output frequency range and the phase noise limitation of the DECT standard [14]. Our goal consists of reducing the lock time by maintaining a tolerable spurious level. In this case, the MSK modulation can be achieved at higher input data rates. The lock time and the spurious level mainly depend on the loop filter parameters, the VCO sensitivity and the charge pump current. So they depend on the analogue part design. For the selected topologies of the charge pump, the loop filter and the VCO, the power consumption is assumed to be less than 1mW. We show previously that the synthesized digital part consumes 6.7mW, considerably greater than the analogue part. That's why, in our optimization approach, we don't introduce the power consumption in the cost function. The analysis of results and the building of experimental designs are carried out with the NEMRODW mathematical statistical software [18].

We apply the experimental design with three levels. In this case, the effect of each factor is studied according to three different values to which we attribute levels +1, 0 and –1 respectively corresponding to the maximum, the middle and the minimum values as illustrated on table 3.

Table 3. Factor range of variation

Variable	Factor	Level (-1)	Level (0)	Level (+1)
X_1	I_{cp} (μA)	1	2	3
X_2	R (KΩ)	416	708	1000
X_3	C_1 (pF)	1	2	3
X_4	C_2 (pF)	10	20	30
X_5	K_{vco} (MHz/V)	30	65	100

To converge to an optimum solution, a relationship between the lock time T_R, spurious level S_{pur} and the five factors X_i is developed. It consists of a full second-order polynomial model obtained by multiple regression technique using the Hoke_D4 experimental designs.

Because of the none-linearity of the studied system, the experimental responses Y_i are represented by a quadratic equation of the response surface:

$$Y_{1,2} = b_0 + \sum_{i=1}^{5} b_i x_i + \sum_{\substack{i \neq j \\ i=1 \\ j=1}}^{5} b_{ij} x_i x_j \qquad (4)$$

where b_0 is a constant, b_i, b_{ij} and b_{ii}, are respectively linear, cross-product and quadratic coefficients.

Y_1 : response representing the lock time ($Y_1 = 1/T_R$);

Y_2 : response representing the spurious level ($Y_2 = 1/Spur$);

The Hoke_D4 matrix consists of N experiments with N=f(k), where K is the number of studied variables. In our case K=5 and, therefore, the matrix is comprised of only 27 simulations instead of $3^5 = 243$. For each one, we measure the lock time T_R and the spurious S_{pur} after 27 simulations in Simplorer 7.0 software. The obtained results are summarized on table 4.

Coefficients (b_i, b_{ii}, b_{ij}) of the postulated model given by expression (4) are calculated on the basis of Hoke_D4 experimental designs with the help of NEMRODW software. The obtained coefficients are summarized on equations (5) and (6).

$$Y_1 = 0.098 + 0.031X_1 + 0.002X_2 + 0.001X_3 + 0.007X_4 + 0.016X_5 - 0.006X_1X_2 + 0.004X_1X_3 + 0.012X_1X_4 + 0.004X_1X_5 - 0.007X_2X_3 - 0.006X_2X_4 - 0.004X_2X_5 + 0.013X_3X_4 + 0.004X_3X_5 + 0.01X_4X_5 + 0.121X_1^2 - 0.061X_2^2 - 0.027X_3^2 - 0.077X_4^2 - 0.003X_5^2 \quad (5)$$

$$Y_2 = 12.311 - 0.979X_1 - 0.248X_2 + 0.978X_3 - 1.086X_4 - 0.049X_5 + 2.57X_1X_2 - 2.107X_1X_3 + 1.23X_1X_4 - 1.264X_1X_5 - 1.742X_2X_3 - 1.005X_2X_4 + 0.214X_2X_5 - 2.288X_3X_4 - 0.081X_3X_5 - 1.766X_4X_5 - 0.498X_1^2 + 2.607X_2^2 + 5.457X_3^2 - 7.098X_4^2 - 2.478X_5^2 \quad (6)$$

Once coefficients b_i, b_{ii} and b_{ij} are determined, we calculate Y_1 and Y_2 using equations (5) and (6). The obtained results are shown on table 4.

Table 5. The variance Analyze

Function	Variation Source	Sum of squares	Degrees freedom	Main square	Significance
Y_1	Regression	0.0920	20	0.0046	93.3
	Residual	0.0656	6	0.0109	
	Total	0.1576	26		
Y_2	Regression	6.85372E+2	20	3.42686E+1	78.3
	Residual	3.16106E+2	6	5.26844E+1	
	Total	1.00147E+3	26		

To estimate the quality of the model and validate it, analysis of the variance and the residual values (difference between the calculated and the experimental result) are examined (table 5). We also compute R^2 as:

R^2 = (Sum of squares attributed to the regression)/ Total Sum of squares)

We find R^2=0.543 related to Y_1 and R^2=0.684 related to Y_2 which reveals that the simulated results fit the second-order polynomial equations (5) and (6).

After the validation of the proposed second-order polynomial model, we can draw 3D plot representing the evolution of Y_1 and Y_2 versus 2 factors. Using contour plot graphs facilitates the evaluation of the influences of the selected factors. Such plots are helpful in studying the effects of the factor variation in the studied domain and, consequently, in determining the optimal experimental conditions.

The lock time, obtained for a variation of factors X_1 and X_5, when fixing X_2, X_3 and X_4 at their intermediate level (0 in coded variable), is shown in figure 10. We can see that the maximum Y_1 (corresponding to a minimum T_R) is achieved by maintaining high I_{cp}. In a second graphical study, we analyze the variation of two factors X_1 and X_2. Other factors are fixed at their central value. Figure 11 shows the minimum T_R value was processed at higher I_{cp} and medium R.

In a third graphical study, we analyze the variation of the two factors X_1 and X_2. Figure12 shows minimum spurious level for both low R and I_{cp} which is the opposite result compared to the previous study.

In a fourth graphical study, we analyze the variation of the two factors X_2 and X_3. Figure 13 shows a minimum spurious for both high C_1 and low R.

Table 4. Experiment matrix

N°	I_{pom}	R	C_1	C_3	K_{vco}	T_R(µs)	Spur(dB) at 20MHz	Y_1 simulated	Y_1 calculated	Y_2 simulated	Y_2 calculated
1	-1	-1	-1	-1	-1	25.05	-4.32	0.040	0.018	4.320	5.447
2	1	0	0	0	0	2.36	-9.74	0.420	0.251	9.740	10.835
3	0	1	0	0	0	26.86	-13.2	0.037	0.039	13.200	14.670
4	0	0	1	0	0	14.97	-24.77	0.066	0.072	24.770	18.747
5	0	0	0	1	0	22.73	-4.96	0.043	0.028	4.960	4.128
6	0	0	0	0	1	6.7	-1.8	0.149	0.111	1.800	9.785
7	1	1	1	1	-1	17.59	-7.26	0.056	0.072	7.260	8.573
8	1	1	1	-1	1	24.55	-13.4	0.040	0.061	13.400	12.509
9	1	1	-1	1	1	13.15	-15.34	0.076	0.103	15.350	13.161
10	1	-1	1	1	1	6.7	-3.42	0.149	0.175	3.420	3.104
11	-1	1	1	1	1	16.97	-4.19	0.058	0.041	4.190	3.780
12	1	1	-1	-1	-1	16.86	-12.3	0.059	0.076	12.300	12.342
13	1	-1	1	-1	-1	36.13	-6.68	0.027	0.043	6.680	8.596
14	1	-1	-1	1	-1	28.18	-12.42	0.035	0.056	12.420	13.038
15	1	-1	-1	-1	1	22	-4.86	0.045	0.072	4.860	3.274
16	-1	1	1	-1	-1	24.23	-10.48	0.041	0.014	10.480	12.302
17	-1	1	-1	1	-1	46.78	-5.82	0.021	-0.001	5.820	6.344
18	-1	1	-1	-1	1	13.87	-13.11	0.072	0.056	13.110	11.430
19	-1	-1	1	1	-1	41.64	-13.78	0.024	0.001	13.780	16.177
20	-1	-1	1	-1	1	34.31	-25.02	0.029	0.012	25.020	25.213
21	-1	-1	-1	1	1	33.81	-10.67	0.029	0.017	10.670	9.565
22	-1	0	0	0	0	30.87	-15.66	0.032	0.188	15.660	12.792
23	0	-1	0	0	0	19.91	-18.41	0.050	0.035	18.410	15.167
24	0	0	-1	0	0	11.15	-12.54	0.089	0.070	12.540	16.790
25	0	0	0	-1	0	81	-7.24	0.012	0.014	7.240	6.299
26	0	0	0	0	-1	18.28	-19.64	0.054	0.079	19.640	9.882
27	0	0	0	0	0	21.23	-5.22	0.047	0.098	5.220	12.311

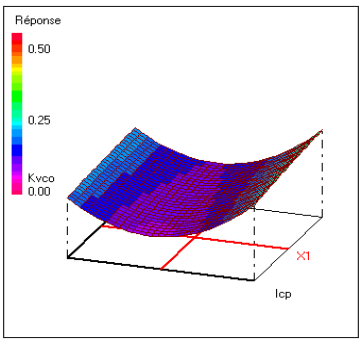

Figure 10. The lock time variation: I_{cp}, K_{vco} (Y_1)

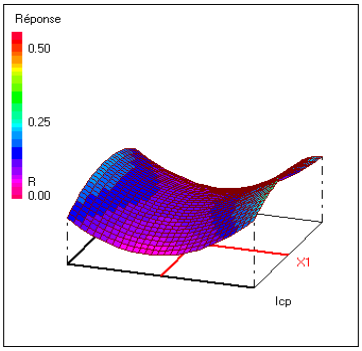

Figure 11. The lock time variation: I_{cp}, R (Y_1)

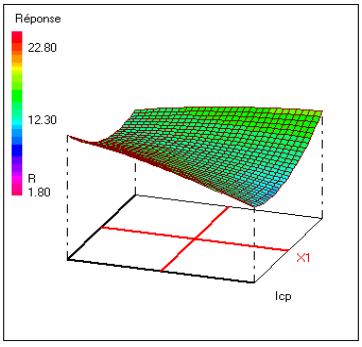

Figure 12. The spurious level variation: I_{cp}, R (Y_2)

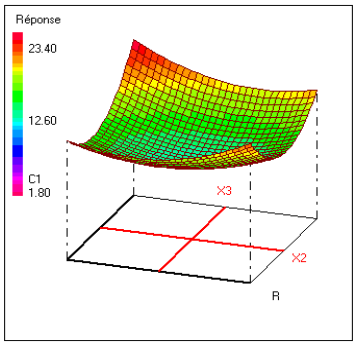

Figure 13. The spurious level variation: C_1, R (Y_2)

We verify with this graphical study that there is a trade-off between the lock time and the spurious level. The relationship between Y_1, Y_2 and variables may be illustrated graphically by plotting both the response values versus the levels of variables simultaneously (figure 14). Such plots are helpful in studying the effects of the variation of the variables in the studied domain and, consequently, in classifying variables depending on their influence on T_R and S_{pur}. We define the sensitivity S_1 and S_2 as:

$$S_1 = \left|\frac{\delta T_R}{\delta X_i}\right|_{a\ \mathrm{var}\ age} \quad \text{and} \quad S_2 = \left|\frac{\delta S_{pur}}{\delta X_i}\right|_{a\ \mathrm{var}\ age}$$

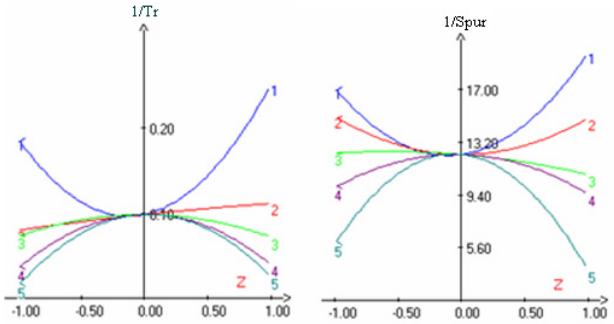

Figure 14. Lockup time and spurious variation

The obtained sensitivities S_1 and S_2 are summarized on table 6. The more influent factors are I_{cp} and K_{VCO}. The less influent ones are C_1, C_2 and R. With the help of NEMRODW Software, we calculate an optimum solution. The level of each factor corresponds to a value in the interval [-1 +1] (table 6). The optimized solution gives a lock time equal to 7.17µs and a spurious level equal to -4.55 dB at 20MHz. When simulating the VHDL-AMS description of the modulator with the optimized solution, we obtain T_R = 7µs and S_{pur} = -4.38 dB at 20MHz (figures 15 and 16). The simulated results are close to the calculated ones, which illustrates the efficiency of the applied optimization method with three levels. As illustrated on table 7, and before the optimization, the lock time is equal to 21.23 µs. After optimization, it is 3 times reduced. The spurious is maintained at a tolerable value.

Table 6. Optimal solution

Number	Factors	S_1	S_2	Level	Value
1	I_{cp}	0.18	10.4	0.9848	2.95 µA
2	R	0.024	3.8	0.5307	530.7 KΩ
3	C_1	0.04	2.4	0.9365	2.8 pF
4	C_2	0.08	4	0.9586	28.75 pF
5	K_{vco}	0.12	11.6	0.7619	76.19 MHz/V

Table 7. Comparison of the obtained solutions

	Lock Time T_R	Spurious level S_{pur}
Before optimization	21.23 µs	-5.22 dB at 20MHz
After optimization	7 µs	-4.38 dB at 20MHz

Because the modulator is faster, the modulation can be achieved at higher input data rates. This result can be verified in figure 17. In fact, in this figure, we compare the obtained signals at the receiver after the demodulation of the transmitted signal with 2MHz input rate. We can see that before the optimization, we loose the emitted signal. After the optimization, the modulator is faster and we can find again the emitted signal at 2MHz.

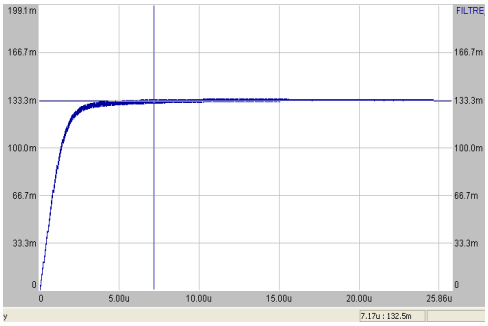

Figure 15. Lock time simulation

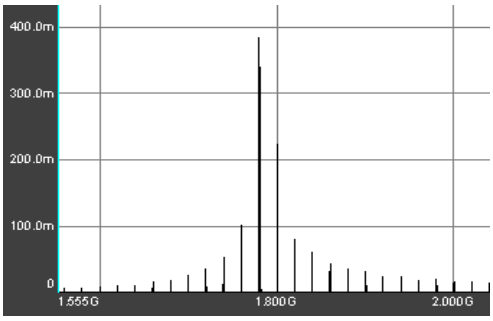

Figure 16. PLL output spectrum (Spurious determination)

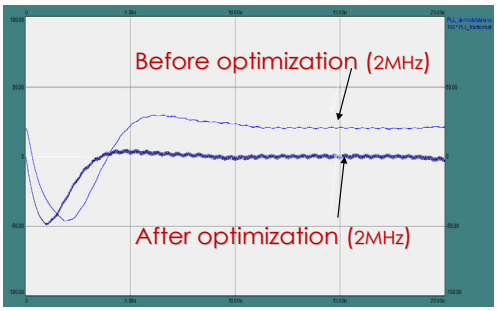

Figure 17. Demodulated signals

4. CONCLUSION

This study exposes a high-level description and simulation with VHDL-AMS of an MSK modulator. We show how a high level language can be used to describe such complex system. At this level, we can talk about virtual prototyping making possible the characterization of a designed system and the prediction of its performances before developing a transistor level description. The applied optimization algorithm based on experimental designs helps to converge to an optimum solution by doing a minimum number of simulations.

NEMRODW software produces ternary diagrams, which shows interactions between factors taken two by two. The proposed full second-order polynomial model obtained by multiple regression technique using Hoke_D4 experimental designs produces satisfactory results compared to the simulation of the developed VHDL-AMS virtual prototype. We converge to an optimum solution given a faster MSK modulator with a reduced spurious.

Many computer aided design softwares are employed to achieve a hierarchical design flow. Our objective consists in helping to develop new analogue synthesis techniques to support a future high-level mixed-signal synthesis environment.

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