Design of Area and Power Efficient Modified Carry Select Adder

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ABSTRACT
Adders are one of the widely used digital components in digital integrated circuit design. The Carry Select Adder (CSA) provides a good compromise between cost and performance in carry propagation adder design. However, conventional CSA is still area-consuming due to the dual ripple carry adder (RCA) structure. In this paper, modification is done at gate-level to reduce area and power consumption. The Modified Carry Select-Adder (MCSA) is designed for 8-bit, 16-bit, 32-bit and 64-bit and then compared with conventional CSA respective architectures. MCSA shows reduction in area and power consumption in comparison with conventional CSA with small increase in delay.

Keywords
Multiplexer, performance, adder, VLSI and data paths.

1. INTRODUCTION
Addition is the heart of computer arithmetic, and the arithmetic unit is often the work horse of a computational circuit. They are the necessary component of a data path, e.g. in microprocessors or a signal processor. There are many ways to design an adder. The Ripple Carry Adder (RCA) provides the most compact design but takes longer computing time. If there is N-bit RCA, the delay is linearly proportional to N. Thus for large values of N the RCA gives highest delay of all adders. The Carry Look-Ahead Adder (CLA) gives fast results but consumes large area. If there is N-bit adder, CLA is fast for N≤4, but for large values of N its delay increases more than other adders. So for higher number of bits, CLA gives higher delay than other adders due to presence of large number of fan-in and a large number of logic gates. The Carry Select Adder (CSA) provides a compromise between small area but longer delay RCA and a large area with shorter delay CLA.

In rapidly growing mobile industry, faster units are not the only concern but also smaller area and less power become major concerns for design of digital circuits [2]. In mobile electronics, reducing area and power consumption are key factors in increasing portability and battery life. Even in servers and desktop computers power dissipation is an important design constraint. Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position [3]. Among various adders, the CSA is intermediate regarding speed and area [2].

In this paper we proposed Modified Carry Select-Adder (MCSA) architecture to reduce area and power with minimum speed penalty .The MCSA is designed by using single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs.

2. CARRY SELECT ADDER
Carry Select Adders (CSA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. The carry-select adder partitions the adder into several groups, each of which performs two additions in parallel. Therefore, two copies of ripple-carry adder act as carry evaluation block per select stage. One copy evaluates the carry chain assuming the block carry-in is zero, while the other assumes it to be one. Once the carry signals are finally computed, the correct sum and carry-out signals will be simply selected by a set of multiplexers. The 4-bit adder block is RCA. The Figure 1 shows 16-bit conventional Carry Select adder.

3. BINARY TO EXCESS-1 CONVERTER
BEC is a circuit used to add 1 to the input numbers. A circuit of 4-bit BEC and the truth table is shown in Figure 2 and Table 1 respectively.

The goal of addition is achieved using BEC together with a multiplexer (mux) shown in Figure 3, one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This gives the two partial results in parallel and the muxes are used to select either BEC output or the direct inputs according to the control signal Cin.

The Boolean expressions of 4-bit BEC are listed below, (Note: functional symbols, ~ NOT, & AND, ^ XOR).

$$X_0 = \sim B_0$$

$$X_1 = B_0 \text{^} B_1$$

$$X_2 = B_2 \text{^} (B_0 \& B_1)$$

$$X_3 = B_3 \text{^} (B_0 \& B_1 \& B_2)$$

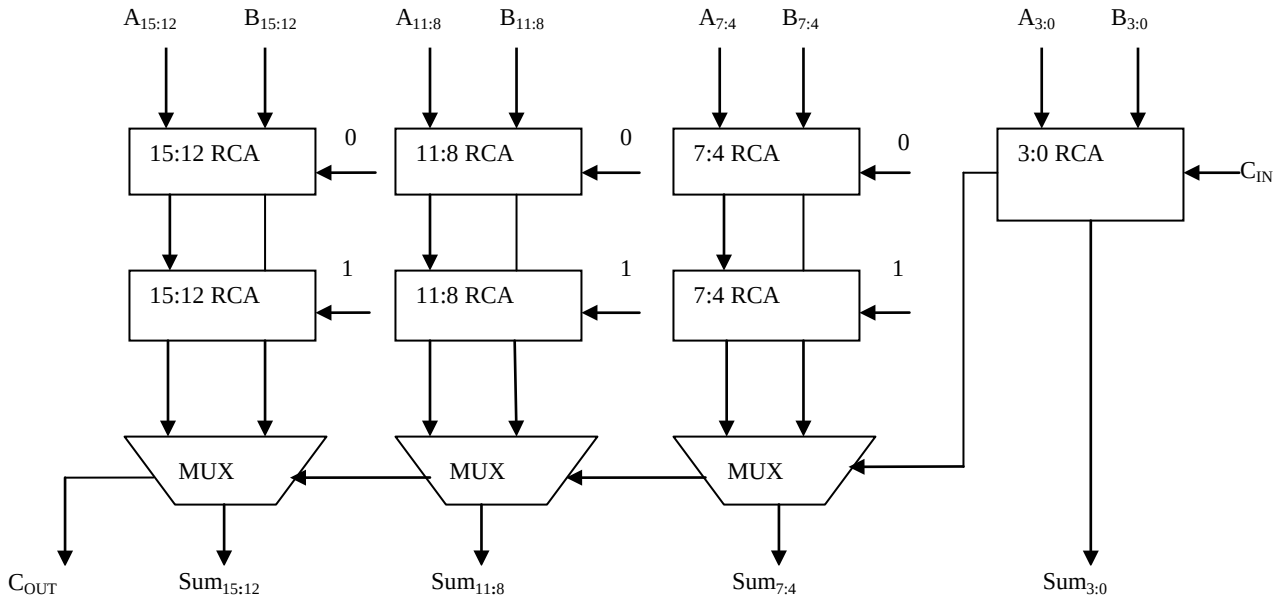

Fig 1:16-bit Conventional Carry Select Adder.

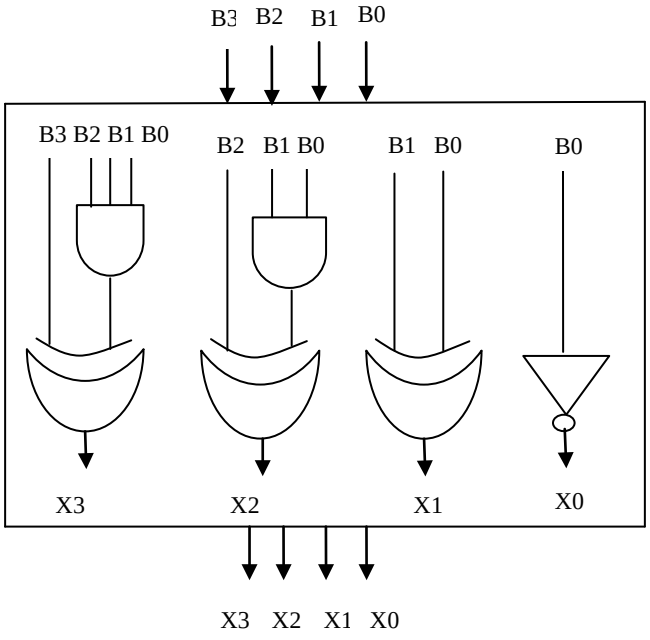

Fig 2: 4-bit Binary to Excess-1 Code Converter.

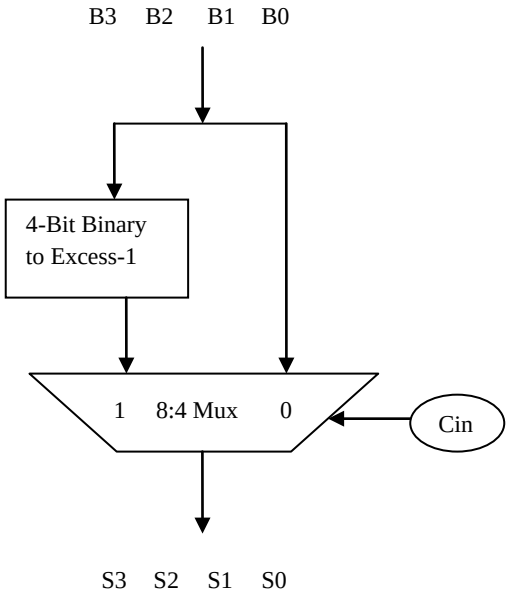

Fig 3: 4-bit Binary to Excess-1 logic with 8:4 multiplexer.

Table 1. Truth table of 4-bit Binary to Excess-1 logic

Binary	Excess-1
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

4. PROPOSED MODIFIED CARRY SELECT ADDER (MCSA) SCHEME

A Modified Carry Select-Adder (MCSA) design is proposed, which make use of single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. As the base of proposed design is that the number of logic gates used in BEC is less than that of RCA. Thus BEC replaces the RCA with Cin=1 instead of using dual RCAs to reduce area and power consumption of the conventional CSA. To replace the N-bit RCA, an N+1 bit BEC is required. The MCSA architecture for 16-bit is shown in Figure 4. The importance of BEC logic comes from the large silicon area reduction when designing MCSA for large number of bits [7].

To elaborate this, the gate calculations are made for 4-bit BEC and 4-bit RCA area as under.

For 4-bit RCA
In 4-bit RCA, four FAs are connected in a chain. Therefore the gates require to built 4-bit RCA are shown in Table 2.

Table 2 . AND, OR and INV gates in 4-bit RCA

AND	28
OR	16
INV	16

For 4-bit BEC
The 4-bit BEC can be obtained by using the Boolean equations (2.17), (2.18), (2.19) and (2.20). From these Boolean equations, the number of AND, OR and INVERT gates used to built 4-bit BEC are shown in Table 3.

Table 3. AND, OR & INV gates in 4-bit RCA

AND	9
OR	3
INV	7

5. SIMULATION RESULTS AND COMPARISON

The various adders are designed using Verilog language in Xilinx ISE Navigator 12.4 .And all the simulations are performed using Xilinx ISim simulator. The performance of proposed MCSA is analysed and compared against the conventional CSA designs. The number of gates used in the design indicates the area of design. The power consumption is measured in terms of total power and dynamic power **.** The speed of the adder is estimated by the delay involved in the design. It can be seen from Table 4 that area and power consumption of MCSA is less than that of conventional CSA, whereas delay is more in MCSA. This shows that area and power consumption of MCSA is reducing at the cost of small decrease in speed. As the number of gates used in the design of MCSA are fewer than the conventional CSA. The reduced number of gates of the MCSA offers a great advantage in the reduction of area and total power consumption.

Table 4. Comparison of area, power and speed of conventional and Modified CSA

Word-size of Adder	Area Reduction (in percent)	Power Consumption reduction (in percent)	Delay Overhead (in percent)
8-bit	16.5	8	15
16-bit	20.62	14	9
32-bit	22.21	16	6.9
64-bit	22.92	17	4

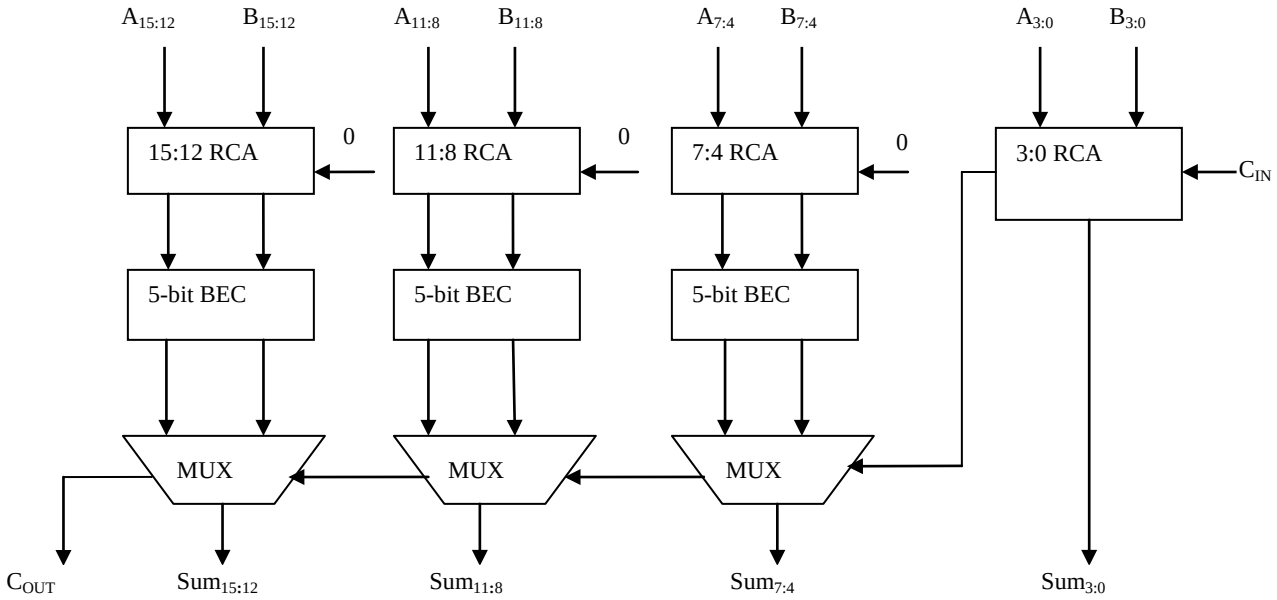

Fig 4: 16-bit Modified Carry Select Adder (MCSA).

In Figure 5, it is shown that the reduction in area and power consumption of MCSA increases with increasing word size of adder. On the other hand, the delay over head decreases with increasing word size. This is shown in Figure 6.

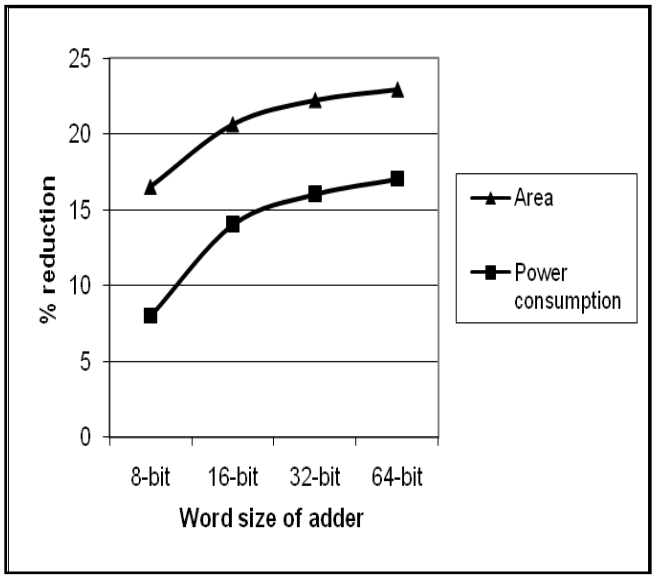

Fig 5: Percentage reductions in area and power consumption.

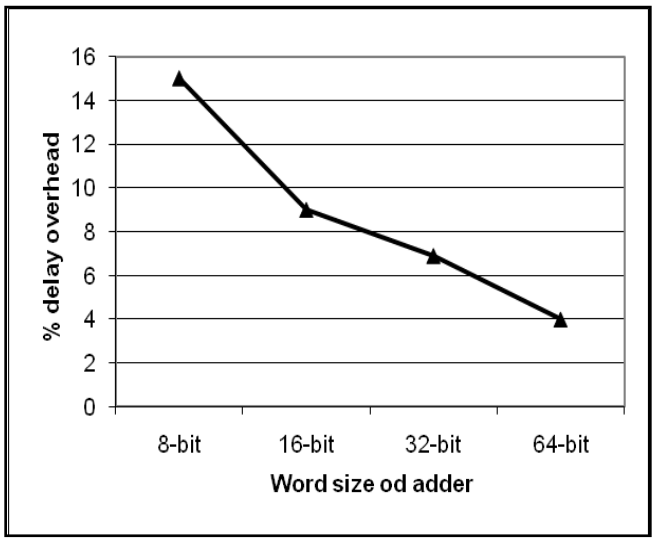

Fig 6: Percentage of delay overhead.

It is clear from above results that the area of 8-bit, 16-bit, 32-bit and 64-bit proposed MCSA is reduced by 16.5 %, 20.62%, 22.21%, and 22.92%. The total power consumed shows the similar pattern of increasing reduction in power consumption 8%, 14%, 16% and 17 % with word size. Whereas delay overhead also exhibits a similar decreasing trend of 15%, 9%, 6.9% and 4% with word size.

6. CONCLUSION

In this paper, a Modified Carry Select-Adder (MCSA) is designed by using single Ripple Carry Adders (RCA) and

Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The MCSA architecture for 8-bit, 16-bit, 32-bit and 64-bit is designed and then compared with conventional CSA respective architectures. MCSA shows reduction in area and power consumption in comparison with conventional CSA with small increase in delay. The synthesis results shows that the reduction in area and power consumption increases with increasing word size of adder whereas delay decreases with increasing word size. It is also analyzed that MCSA for 8-bit, 16-bit, 32-bit and 64-bit shows an increasing order of reduction in area by 16.5 %, 20.62%, 22.21%, 22.92% and power consumption by 8%, 14%, 16%, 17 % respectively. Whereas, the delay overhead for 8-bit, 16-bit, 32- bit and 64-bit MCSA indicates decreasing trend with bit size as 15%, 9%, 6.9% and 4% respectively. Therefore, MCSA architecture is low area, low power, simple and efficient for VLSI hardware implementation. In future, the design can be further extend for higher number of bits

7. REFERENCES

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