

Design of a Multifunction BVMF Reversible Logic Gate and its Applications

Bhagyalakshmi H R

Visvesvaraya Technological University
BMS College of Engineering
Bangalore

Venkatesha M K

Visvesvaraya Technological University
RNS Institute of Technology
Bangalore

ABSTRACT

The power dissipation problems which occur in the computational operations of a computer can be avoided by replacing the irreversible structures by reversible structures. The reversible logic gates are used for the construction of important arithmetic and logic units of quantum computers. This has led many researchers to take reversible logic very seriously. In this proposal a new reversible logic gate called BVMF gate is designed which is useful for the realization of multi functions required for building important computational blocks of quantum computers.

General Terms

Reversible logic circuits, Quantum computers

Keywords

Reversible logic gate, quantum computational blocks, multifunction reversible logic gate.

1 INTRODUCTION

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum computers use reversible computational structures to perform various arithmetic and logical operations. According to Landauer's principle, the loss of one bit of information dissipates $kT \ln 2$ joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that in order to avoid $kT \ln 2$ joules of energy dissipation in a circuit it must be built from reversible circuits [2].

A reversible logic gate is an n -input, n -output logic device with one-to-one mapping. This helps to uniquely determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Extra inputs are added to make the number of inputs equal to the number of outputs in a reversible logic gate [3, 4]. Fan-out in reversible gates must be derived from the gate maintaining one or more inputs constant.

A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit produces minimum number of garbage outputs. Also they must use minimum number of constant inputs [3, 4]. It has been shown that both the combinational as well as the sequential circuits can be designed using reversible logic gates.

From the survey of existing research works on various reversible logic circuits we observe that the important parameters of interest are minimum garbage outputs, minimum delay and minimum quantum cost. To achieve this many researchers find an optimized way of connecting discrete reversible logic gates to build the circuit. But in this proposal we are introducing a new reversible logic gate which can be used for different functions by placing different constant inputs on one or more inputs. In this way the gate becomes more flexible and hence can be used for the realization of various circuits.

This paper is organized as follows: Section 2 gives the necessary information on some of the basic reversible logic gates along with their logic diagrams. In Section 3 the design of the proposed flexible reversible logic gate along with truth table is described. In section 4 applications using the proposed BVMF gate are described. Finally section 5 concludes with scope for further research.

2 BASIC REVERSIBLE LOGIC GATES

In this section some basic reversible logic gates are discussed.

2.1 Feynman Gate

Figure 1 shows a 2x2 Feynman gate [5]. The input vector is $I(A, B)$ and the output vector is $O(P, Q)$ and the relation between input and output is given by $P=A, Q = A \oplus B$. It is used to copy the input without producing garbage bits with $B=0$.

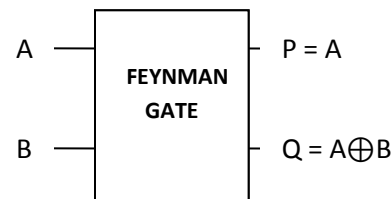


Figure 1: Feynman gate

2.2 Double Feynman Gate (F2G)

Figure 2 shows a 3x3 Double Feynman gate [6]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$ and output is defined by $P = A, Q = A \oplus B, R = A \oplus C$.

It can be used for fan-out purpose and for generating complement inputs at its outputs by using appropriate constant values at inputs.

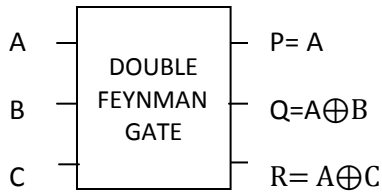


Figure 2: Double Feynman gate

2.3 Toffoli Gate (TG)

Figure 3 shows a 3x3 Toffoli gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by $P = A$, $Q = B$, $R = AB \oplus C$.

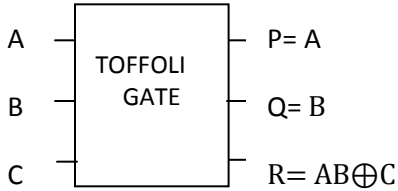


Figure 3: Toffoli gate

Toffoli gate can be used as basic AND gate with values $C=0$ and as a NAND gate with $C=1$ as shown in Figure 3a and Figure 3b respectively.

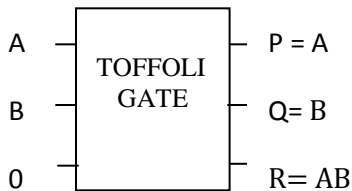


Figure 3a: Toffoli gate as an AND function

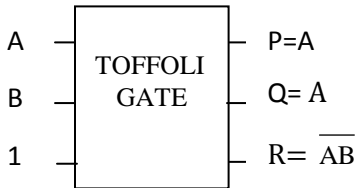


Figure 3b: Toffoli gate as a NAND gate

With $B=1$ and $C=0$ it can be used as a fan-out gate for input A while passing B as shown in Figure 3c.

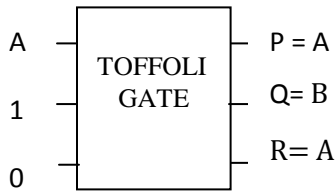


Figure 3c: Toffoli gate as fan-out gate

2.4 Fredkin Gate (FG)

Figure 2.4 shows a 3x3 Fredkin gate [3]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by $P=A$, $Q=A'B \oplus AC$ and $R=A'C \oplus AB$.

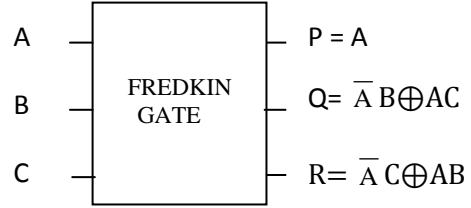


Figure 4: Fredkin gate

Fredkin gate fan-outs A with $B = 0$ and $C = 1$ at its output P and Q while at R it produces complement of A.

With $C = 0$ it produces of A.B at R while with only $B = 0$ it produces A.C

2.5 Peres Gate (PG)

Figure 5 shows a 3x3 Peres gate [6]. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$.

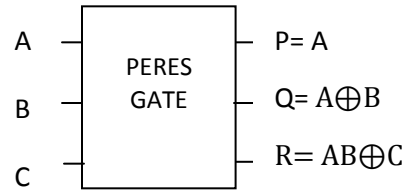


Figure 5: Peres gate

Peres gate behaves as a half adder with inputs A and B maintaining $C = 0$.

With $C = 1$ the outputs are $Q = A \oplus B$ and $(AB)'$.

With $B = 1$ and $C = 0$ it outputs A, A' and A at P, Q and R respectively.

2.6 BVF Gate

Figure 6 shows a 4 * 4 BVF gate [12]. This is a reversible double XOR gate and can be used for duplication of the required inputs to meet the fan-out requirements. The input vector is I(A,B,C,D), the output vector is O(P,Q,R,S) and the output is defined by $P = A$, $Q = A \oplus B$, $R = C$ and $S = C \oplus D$.

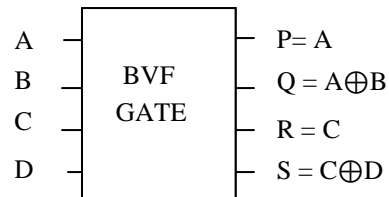


Figure 6: BVF gate

BVF gate can be used as a fan-out gate with $B = 0$ and $D=0$ as shown in Figure 6a.

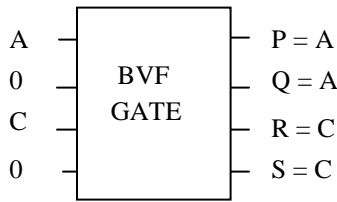


Figure 6a: BVF as a fan-out gate

3. PROPOSED BVMF GATE

Basic functions are obtained by maintaining different constant values at the inputs of some of the important existing gates. In the proposed 4×4 gate, multiple functions [7-11] are accommodated in order to make it more flexible as flexibility is one of the important requirements of a logic gate.

3.1 BVMF Gate

This is a multifunction 4×4 reversible logic gate shown in Figure 7 with input vector $I (A, B, C, D)$ and the output vector is $O (P, Q, R, S)$.

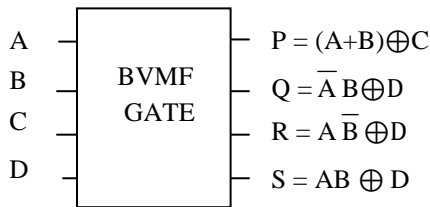


Figure 7: BVMF gate

The truth table of BVMF gate is as shown in Table. 1

Table .1 Truth table of BVMF gate

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	1	0	0	0
0	0	1	1	1	1	1	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	1	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	1	1	0

4. APPLICATION OF BVMF GATE

BVMF gate can be used for the following applications.

1. Universal gate
2. Fan-out
3. Decoder
4. Demultiplexer
5. Comparator

4.1 Universal Gate

Implementation of basic gates using BVMF gate with AB as inputs and CD as control inputs.

(i) With A and B as inputs while CD maintained constant at 00 as shown in figure 8a , AND and OR gates are available at the outputs. The truth table is as shown in table.2

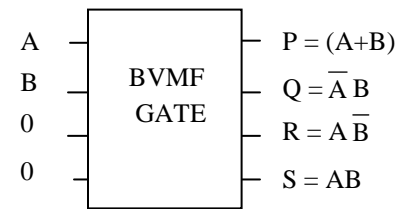


Figure 8a: OR and AND functions

Table.2 for $CD = 00$

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	1	0	0	1	1	0	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	0	1

(ii) With A and B as inputs while CD maintained constant at 01 as shown in figure 8b, OR and NAND gate functions are available at the outputs. Truth table is as shown in table.3.

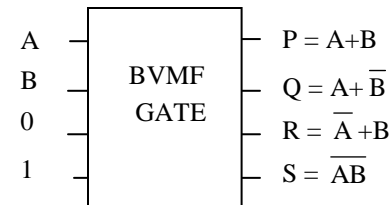


Figure. 8b : OR and NAND functions

Table 3 for $CD = 01$

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	1	0	1	1	1
0	1	0	1	1	0	1	1
1	0	0	1	1	1	0	1
1	1	0	1	1	1	1	0

(iii) With A and B as inputs while CD maintained constant at 10 as shown in figure 8c, NOR and AND gate functions are available at the outputs. Truth table is as shown in table.4.

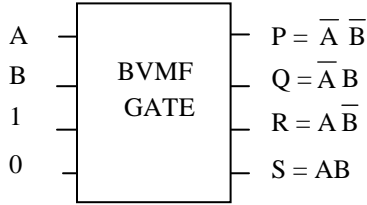


Figure. 8c: AND and NOR functions

Table 4 for CD = 10

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	1	0	1	0	0	0
0	1	1	0	0	1	0	0
1	0	1	0	0	0	1	0
1	1	1	0	0	0	0	1

One important application of BVMF gate with C = 1 and D=0 is that it can be used as a 2 to 4 decoder. In this particular application of BVMF gate input C acts as control input and D as active low enable input. On the other hand it can be viewed as a 1 to 4 DMUX with A and B as select inputs and C as active high input and D as an active low enable input just like irreversible 1 to 4 DMUX circuit as shown in fig. 8d.

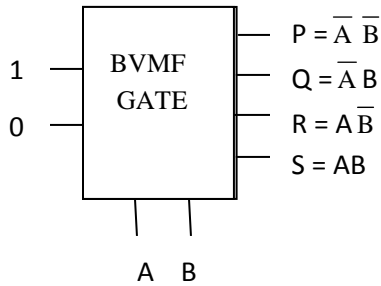


Figure. 8d: 1 to 4 DMUX

(iv) With A and B as inputs while CD maintained constant at 11 as shown in figure 8e, NOR and NAND gate functions are available at the outputs. Truth table is as shown in table.5.

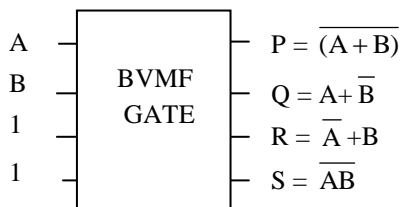


Figure.8e: NOR and NAND functions

Table 5 : CD = 11

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	1	1	1	1	1	1
0	1	1	1	0	0	1	1
1	0	1	1	0	1	0	1
1	1	1	1	0	1	1	0

Inputs and outputs of BVMF gate for different constant inputs at C and D are recorded as shown in table.6 and table 7.

Table.6 : Outputs with C and D as control inputs in BVMF gate

A	B	C	D	P	Q	R	S
X	X	0	0	A+B	A-bar B-bar	A-bar B	AB
X	X	0	1	A+B	A+B-bar	A-bar+B	A-bar B-bar
X	X	1	0	A-bar+B	A-bar B	A B-bar	AB
X	X	1	1	A+B	A+B-bar	A-bar+B	A-bar B-bar

Table 7:Basic gate functions using BVMF gate.

A	B	C	D	P	Q	R	S
X	X	0	0	OR	A-bar B-bar	A-bar B	AND
X	X	0	1	OR	A+B-bar	A-bar+B	NAND
X	X	1	0	NOR	A-bar B	A B-bar	AND
X	X	1	1	NOR	A+B-bar	A-bar+B	NAND

From the above studies it is observed that BVMF gate can be used as a universal gate.

4.2 Fan-out

With C and D as inputs while maintaining A and B as control variables fan-out can be achieved.

(i) C and D as inputs with AB maintained constant at 00 as shown in figure. 9a fan-out of D can be achieved. Truth table is as shown in table 8

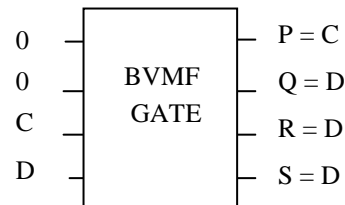


Figure.9a:Fan-out

Table 8 for AB = 00

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	1	0	0	0
0	0	1	1	1	1	1	1

(ii) With C and D as inputs while AB maintained constant at 01 as shown in figure. 9b fan-out of D and the complement of C and D can be achieved. Truth table is as shown in table 9.

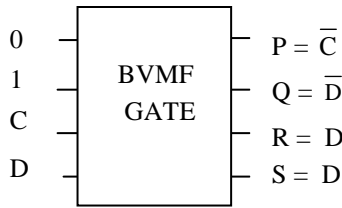


Figure.9b : Fan-out and complement

Table 9 for AB = 01

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	0	1	1

(iii) With C and D as inputs while AB maintained constant at 10 as shown in figure. 9c fan-out and the complement of C and D can be achieved. Truth table is as shown in table 10.

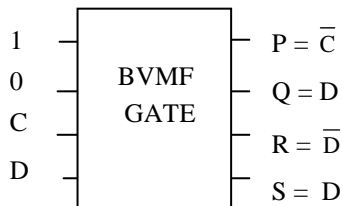


Figure. 9c: Fan-out and complement

Table 10 for AB = 10

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
1	0	0	0	1	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	1	0	1	0	1

(iv) With C and D as inputs while AB maintained constant at 11 as shown in figure. 9d fan-out and the complement of C and D can be achieved. Truth table is as shown in table 11.

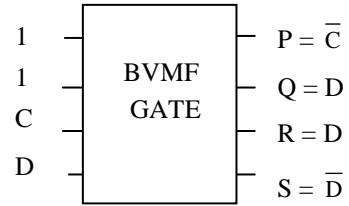


Figure. 9d : Fan-out and complement

Table 11 for AB = 11

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	1	1	0

Outputs of BVMF gate as fan-out gate for different constant inputs at A and B are recorded as shown in table.12.

Table 12 : Fan-out of C and D

A	B	C	D	P	Q	R	S
0	0	X	X	C	D	D	D
0	1	X	X	C-bar	D-bar	D	D
1	0	X	X	C-bar	D	D-bar	D
1	1	X	X	C-bar	D	D	D-bar

With CD as inputs and AB maintained at constant BVMF can be used as a fan-out gate.

4.3 Comparator

Implementation of comparator circuit using BVMF gate is as shown in fig.10.

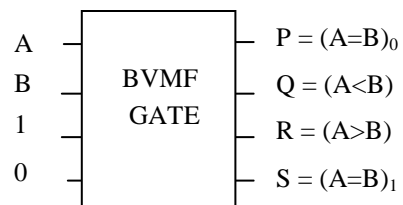


Figure 10: BVMF gate as a comparator

The above circuit compares A with B clearly indicating the values of A and B. Table.13 shows the comparator table.

Table 13: BVMF as a Comparator gate

A	B	C	D	$(A=B)_0$	$(A<B)$	$(A>B)$	$(A=B)_1$
0	0	1	0	1	0	0	0
0	1	1	0	0	1	0	0
1	0	1	0	0	0	1	0
1	1	1	0	0	0	0	1

5. CONCLUSIONS

The focus of this paper is the application of a reversible logic gate to realize multiple functions and to implement basic functions like fan-out, decoder/DMUX , comparator which are of importance in VLSI communication systems and other significant application areas like such as quantum computing, nano-technology, and optical computing. In the present proposal an attempt is made to design a multifunction reversible logic gate keeping in view the optimization factors of the reversible circuits. This paper also aims at minimising the parameters like number of garbage outputs, number of constant inputs, number of reversible gates and their levels. The proposed logic gate is highly optimized as it does not yield the garbage output and at the same time it is highly flexible as it produces important basic functions used in logic circuit design. The future work includes applying concept of reversible logic to build different combinational circuits using new flexible reversible logic gates.

6. ACKNOWLEDGMENTS

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