32 nm Gate Length FinFET: Impact of Doping

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ABSTRACT
FinFET, a self–aligned double-gate MOSFET structure has been agreed upon to eliminate the short channel effects. In this thesis, we report the design, fabrication and physical characteristics of n-channel FinFET with physical gate length of 32nm using visual TCAD (steady state analysis). All the measurements were performed at a supply voltage of 1.5V and T_{ox}=5nm. We elucidate the impact of doping concentration on the Performance of n-channel 32nm gate length FinFET at 22nm width. The drain current increases gradually when donor ion concentration in source/drain regions increases to 7e20 cm^{-3}. Adding opposite type of source/drain impurity or decreasing acceptor ion concentration in channel further improves the performance of FinFET.

Keywords
FinFETs; CMOS; Drain Induced barrier lowering; Silicon-on-insulator

1. INTRODUCTION
SOI (silicon on Insulator) basis multi-gate transistor structure is advisable for miniaturization of transistors and adequate for conquering short channel effects [1]. Fragile structured SOI devices are encouraging for escalating CMOS devices into nano-scale regime. One of them is dual-gate FinFET, includes a steep Si fin restrained by self-aligned double gate [2]. The FinFET technology is enticing because the procedure is accessible to implement with existing processing approaches [3]. The technology consists of developing a slender silicon island (fin) by engraving the silicon film [3].

Some of the essential aspects of FinFET are ultra thin Si fin for elimination of short channel effects, lifted source/drain to cut down parasitic resistance and revamp drive current [2]. FinFETs exploit symmetric gates to achieve tremendous performance, but can be fabricated with asymmetric gates so as to target threshold voltage [4]. FinFETs are drafted to benefit numerous fins to attain larger channel widths [4, 5]. Source/Drain pads bridge the fins in parallel. Increment in number of fins leads to boost the current through the device [4, 5]. For example, a device having five fins has five times higher current than single fin device [4]. The leading asset of the FinFET is the ability to exceptionally lower the short channel effects [2, 3, and 4]. In spite of double gate structure, the FinFET is related to its essence, the conventional MOSFET in layout and fabrication [2]. Three dimensional FINFET design is shown in Fig. 1. FINFET comprises a narrow perpendicular fin placed on the exterior of the wafer. Source and drain are crosswise on both sides of fin. This structure is positioned on SOI substrate.

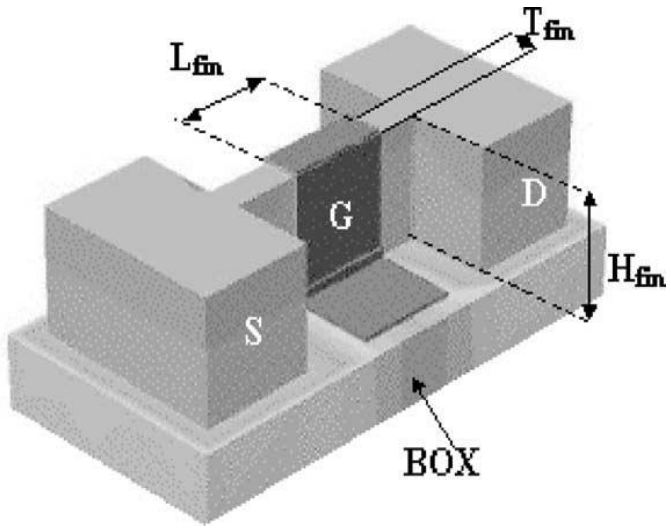

Fig 1: FinFET structure [3]

2. DEVICE FABRICATION
The FinFETs are manufactured on bonded SOI wafers with a modified planar CMOS mechanism. A considerable discrepancy between a FinFET and a traditional planar FET is a slim active region (fin) [6]. Contraction of the fin width (i.e. body thickness), T_{fin} is essential for scaling of double-gate FinFET [6]. And the super-imposition of the gate to the active region should be productively restrained to curtail the transistor performance variation [6].

In two-gate FinFET, effective gate length equals to $2H_{fin}$ and in Tues gate FinFET equals to $2H_{fin} + T_{fin}$. Tues gate FINFET has two gates positioned on both faces of the fin resolved by H_{fin} and a gate raised above which is as much as T_{fin} [1, 7]. Accordingly, the gate length of 32 nm and H_{fin}=5 nm the calculated width of gate i.e. T_{fin}= 22nm. The top view drawing of FinFET is shown in Fig. 2.

Fig. 3 shows the material used for the contrasting regions. Nitride spacers (sp1, sp2, sp3 and sp4) are used as gate insulator and the gate oxide (toxide/Boxide) is SiO_2 type [1, 3, and 8]. The front and back gate electrodes are of aluminium metal with gate contact having work function of 4.17eV. The source and drain are homogenous having ohmic contact with aluminium electrode. This region of the device is massively doped to 7e20 cm^{-3} of n-type ions and acceptor region is doped with 1e16 cm^{-3} p-type ions. The doping profile of the device is shown in Fig. 4. For simulation purpose, we build a mesh for the device to be fabricated according to the mesh size as given in table1, the meshed device is shown in Fig. 5. The steady state analysis of FinFET is realized by basic drift diffusion equation method [1]. The IV characteristic curves are simulated at room temperature (300K) for heat transfer coefficient of 1KW/K/cm^2. Fig. 5 shows the hole current in FinFET at Vg=V_d=1.5V and Drain current of 0.0410523mA.

Table 1 Regions of FinFET with mesh size

Region	Material	Mesh size(μm)
Substrate	Silicon	0.005
Source/Drain	Al	0.001
Tgate/Bgate	Al	0.001
Toxide/Boxide	SiO_2	0.0005
Spacers(sp1,sp2,sp3,sp4)	Nitride	0.1

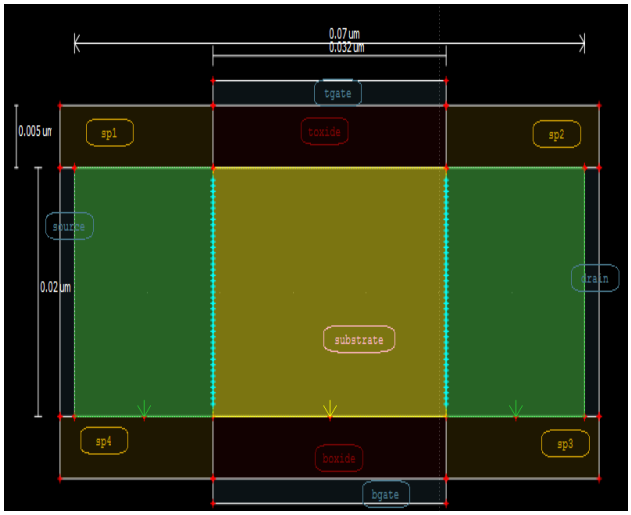

Fig 2: Drawing of FinFET in TCAD

3. DEVICE CHARACTERISTICS

The emblematic trait of the FinFET is that the conducting channel is encased by a slender silicon "fin", which forms the body of the device. The thickness of the fin deduces the effective channel length of the device. The Wrap-around gate structure yields a superior electrical regulation over the channel and thus aids in reducing the leakage current and conquering other short-channel effects. Fig. 7 and Fig. 8 shows the I_d-V_d characteristics at 32nm gate length device with a 22nm-thick Si fin body on linear and logarithmic scale respectively. At 1.5V gate voltage, Drain voltage is varied from 0 – 1.5V with step of 0.05V. Following I_d-V_d characteristics are determined for different gate voltages (1.5V, 1.25V, 1V, 0.5V). The slope of I_d – V_d curve is higher for the high applied gate voltage. Fig. 9 shows the sub threshold I_d – V_g characteristics curves where V_g = -0.5 to 1.5V provided drain voltage of 1V and 0.05V.

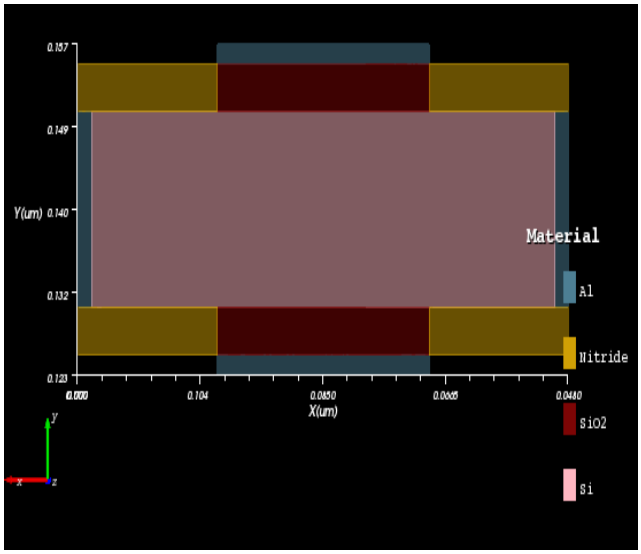

Fig 3: Material used for fabrication

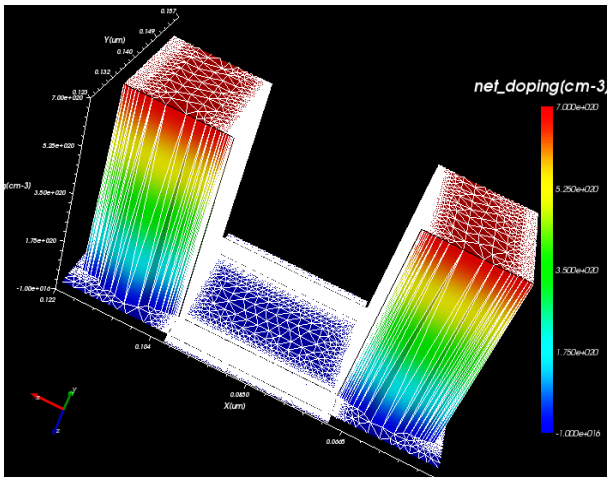

Fig 4: 3D View of Net doping for the device

To examine the effect of amount of impurity of source/drain regions on FinFET output characteristic curve, when the doping is varied. Fig 10 shows the boost in drain current with increase in doping of source/drain. The side diffusion of source/drain regions consequence in reduction in device's effective channel length which leads to hike in drain current of the device [1].

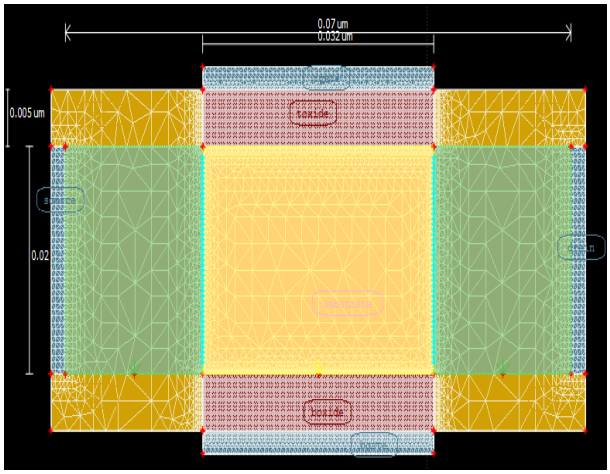

Fig 5: Meshed FinFET

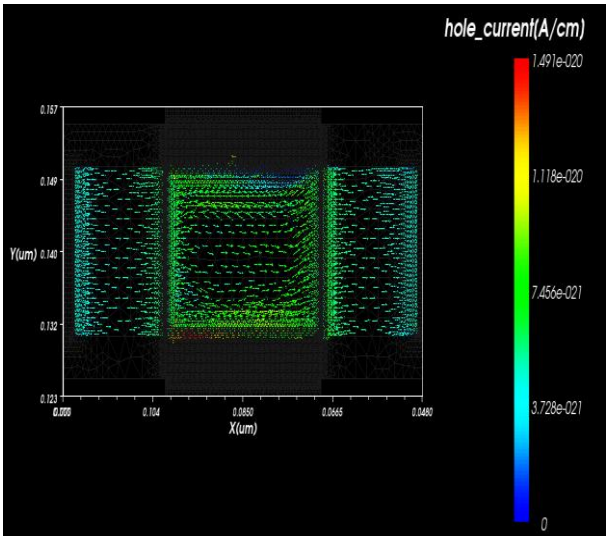

Fig 6: Hole current at V_g=V_d=1.5V and I_d= 0.0410523mA

The aftereffect of impurity of opposite type of source/drain region is contraction of channel length which has valuable impact on transistor conductance [1,8]. Fig 11 shows the I_d-V_d characteristic curve for distinct acceptor ions concentration. The drain current is high for lower concentration of the p-type ions in channel as DIBL (drain induced barier lowering) reduces gradually as channel doping increases [8]. Hence Fig 12 shows the I_d-V_d characteristics for the different acceptor and donor ions concentrations. It represents that the higher concentration of donor ions in n-type region and lower concentration of acceptor ions in p-type region consequences to increase the conductance of transistor. I_d-V_d characteristics curve is high at 7e20 cm^{-3} donor ions concentration and 1e16 cm^{-3} acceptor ions concentration.

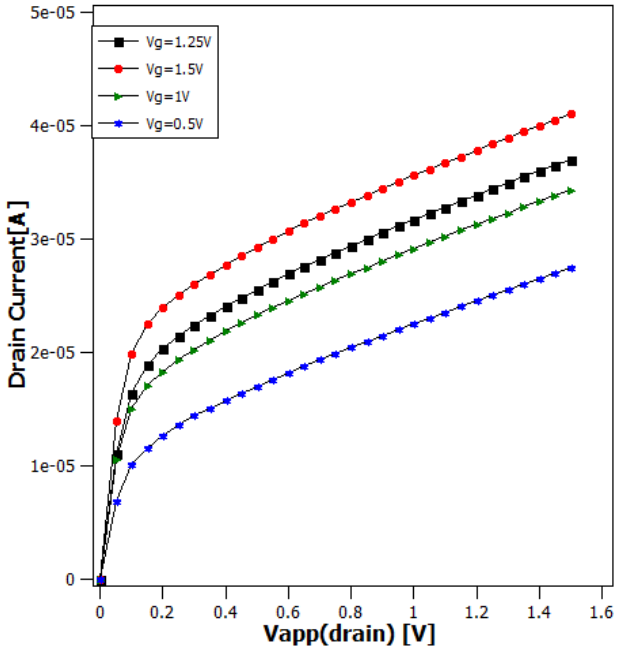

Fig 7: I_d – V_d characteristics for 32nm gate length n-FinFET

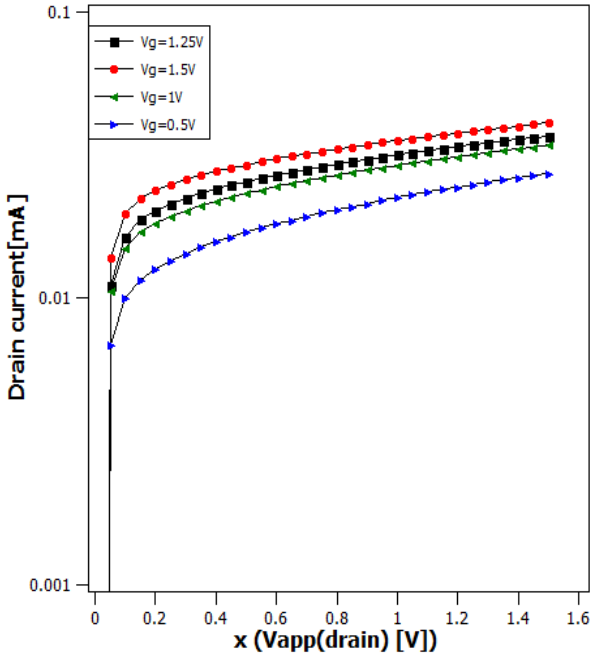

Fig 8: I_d – V_d characteristics for 32nm gate length n-FinFET on logarithmic scale

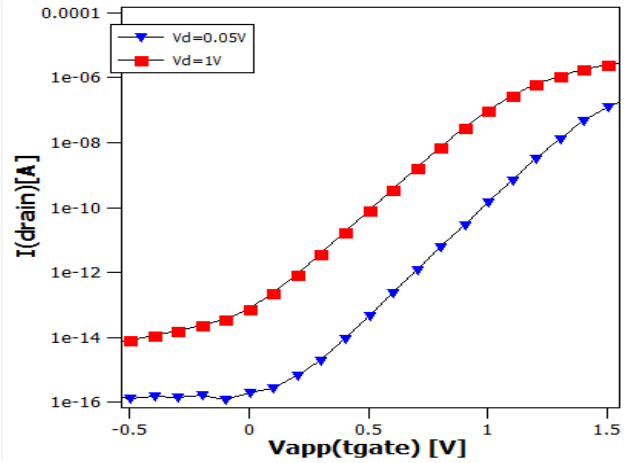

Fig 9: Subthreshold I_d – V_g behavior(logarithmic scale) of 32nm gate length n-FinFET transistors

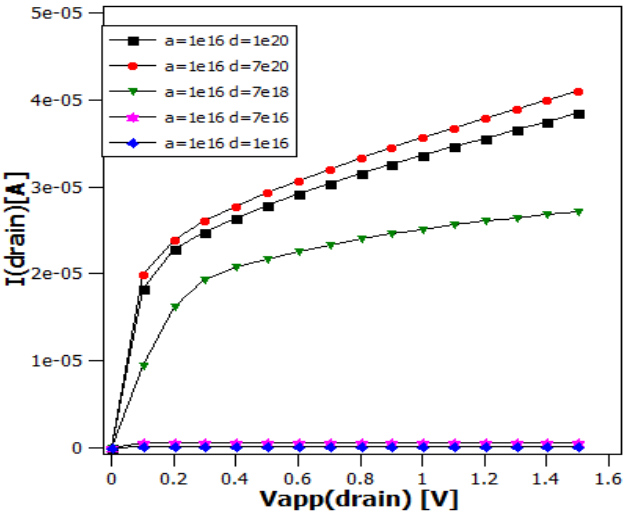

Fig 10: Increasing source/drain impurity (donor type) leads to increase in drain current

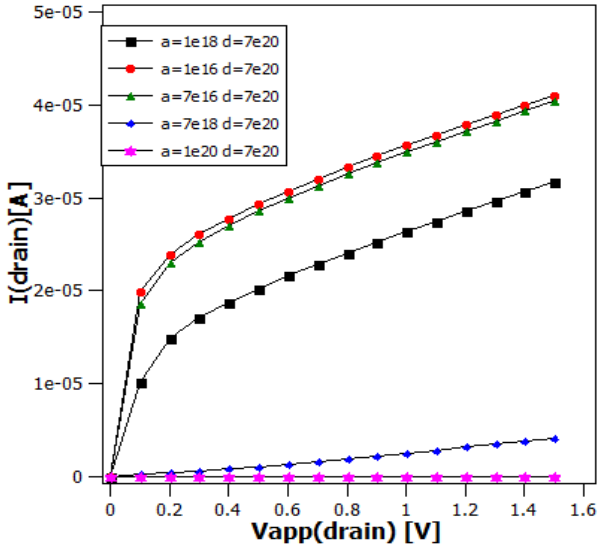

Fig 11: Decreasing acceptor ion concentration leads to increase in drain current

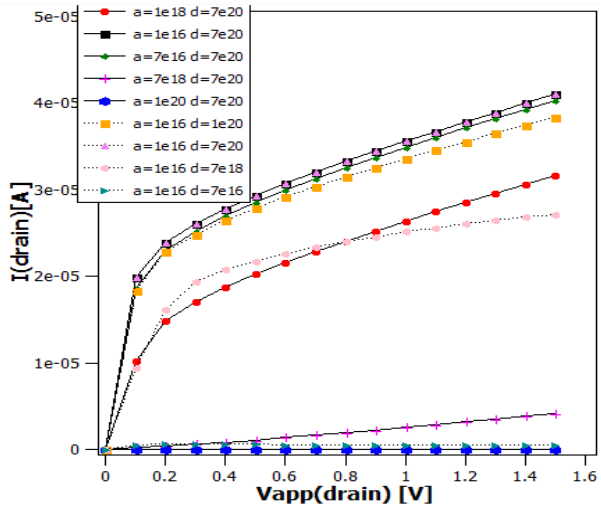

Fig 12: I_d – V_d characteristics for different concentraions of donor and acceptor ions

4. CONCLUSION

The steady state analysis of n-channel 32nm gate length FinFET at 22nm fin width has been done using visual 2D-TCAD software. As the supply voltage at gate is increased, there is hike in I_d which indicates that resistance reduces at higher V_g. The drain saturation current is 0.0343453mA at V_g=1V and 0.0410523mA at V_g=1.5V which indicates approximately 20% hike in I_d with increase in 0.5V gate voltage. The drain current increases when donor ion concentration in source/drain regions rises to 7e20 cm^{-3}. Adding opposite type of source/drain impurity or decreasing acceptor ion concentration in channel further revamp the conductance of FinFET. As for the high donor ion concentration of 7e20 and lower acceptor ion concentration of 1e16, I_d-V_g characteristic curve represents the terrific outcome but it shows inferior conductance when both the donor and acceptor concentration is equivalent of 1e16.

5. REFERENCES

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