Impact of Varying Fin Width in an n-FinFET at 20nm Gate Length

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ABSTRACT
A double gate FinFET can reduce drain induced barrier lowering and improve threshold (short channel effects). In this paper, a very important geometrical parameter, that is, the fin width of a FinFET has been analyzed. In this article, a double gate n channel FinFET with a gate length of 20nm has been reported. The transfer characteristics of the FinFET at various fin widths have been obtained at a supply voltage of 0.1 V. A comparison is then made between the transfer characteristics of various fin widths. It is observed that, at greater fin widths the drain current also increases as compared to that at shorter fin widths. Thus an increase in device performance is expected, but at the cost of increase in short channel effects. All the simulations have been performed in visual TCAD (Tiber CAD).

Keywords
TCAD, silicon on insulator (SOI), DIBL, Fin field effect transistor (FinFET)

1. INTRODUCTION
According to Moore's Law, the number of transistors in an integrated circuit doubles every two years, or we can say the overall processing power of an integrated circuit doubles every two years [1]. Several strategies have been developed by various manufacturers to scale down the size of the microprocessors and the memory cells such as CMOS technology, SOI technology, etc. [2]. One such strategy is the multi-gate transistor [3].

A MOSFET with more than one gate into a single device is referred to as a multi-gate device or transistor. FinFETs, the multi or tri-gate architectures can be scaled down to deca-nanometer range [4]. In FinFETs, the gate is wrapped around a thin, undoped Si, called a 'fin'; this is from where it derives its name. The sides of the fin are wrapped around by an oxide, which breaks the active region into several fins and a gate overlaps the channel regions of the fins. This increases the control of the gate over the channel and thus high switching ratios can be attained [5].

In a bulk nanoscale MOSFET, the variation of device performance as a result of fluctuations in dopant ions is high [6]. This can be overcome in a FinFET owing to its electrostatic control over the channel as mentioned above.

Figure 1 shows the schematic of a FinFET along with its important geometrical parameters, the gate length (L_G), fin width (W_{fin}) and fin height (H_{fin}).

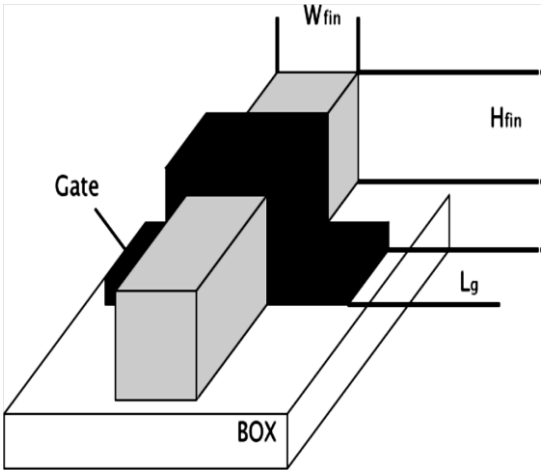

Figure 1 Schematic of a FinFET device, showing important dimensions: the fin width (W_{fin}), fin height (H_{fin}) and gate length (L_G)[5]

In a MOSFET the control over the short channel effects such as the drain induced barrier lowering, channel length modulation and hot carrier effects etc. is less [7]. This can be improved in a FinFET. In a FinFET, we can improve the control over short channel effects by decreasing the fin width. But decreasing the fin width comes with its own set of disadvantages like, an enhanced parasitic source to drain resistance, which degrades the drain current and transconductance [5].

2. DEVICE FABRICATION
The circuit schematic of a 2D double gate n type FinFET in TCAD software is as shown in the figure 2. The modeling of double gate FinFET has been done in TCAD.TCAD is a software tool that models semiconductor fabrications and also semiconductor device operation.

FinFET has been fabricated on SOI (silicon on insulator) wafer with SiO_2 as the buried oxide of thickness 1nm. The gate length of the FinFET has been chosen to be 20nm. All the analyses have been done on this gate length only [8]. The substrate used is that of silicon. The gates as well as the source and the drain electrodes have been taken to be made of Al. The workfunction of both the front and back electrode is 4.17eV. Both the source and drain have ohmic contacts and the heat transfer coefficient is $1KW/K/cm^2$.

Using nitride spacers leads to an increase in the on state current i.e. it improves the switching ratio [9]. Here we have used four nitride spacers i.e. sp1, sp2, sp3 and sp4.We can also use dual material spacer (the spacer with two different dielectrics e.g. silicon nitride and hafnium oxide) or triple

material spacers (the spacer with three different dielectrics e.g. silicon dioxide, silicon nitride and hafnium oxide) to further enhance the device performance.

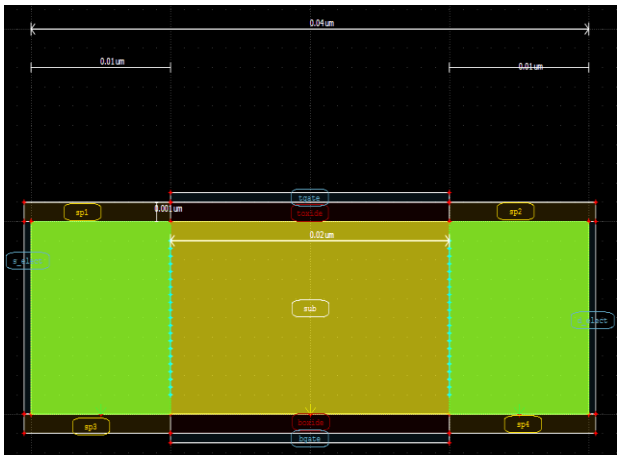

Figure 2 Circuit schematic of 2D FinFET in TCAD software

TABLE 1 Different Parameters at 20nm Technology

Parameters	Dimensions
Length of gate (L_G)	20nm
Spacer Width	1nm
Gate Oxide Thickness	1nm
Thickness of Fin(W_{fin})	Varied from 1nm to 1000nm
Doping Conc. Of Source and Drain	1e+20
Doping Conc. Of Channel	1e+18

The height of the FinFET is 10nm. The substrate is doped with acceptor type impurity with a doping concentration of 1e+18/cm^3, where as the source and drain are doped with donor type impurity with the doping concentration of 1e+20/cm^3. The fin width has been varied from 1nm to 1000nm.

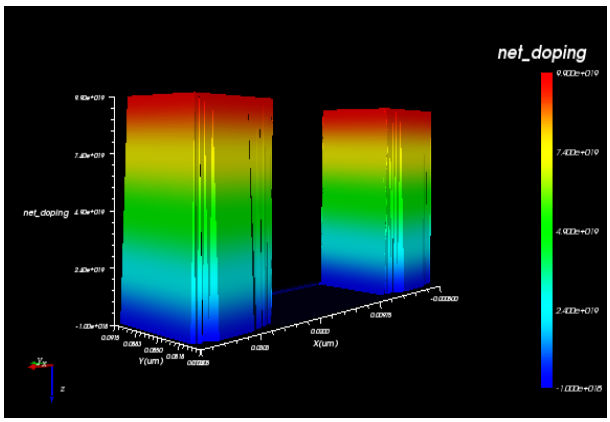

Figure 3 3D view of Net Doping in the FinFET

3. SIMULATION AND RESULTS

Device simulations have been performed using the drift diffusion model at room temperature i.e. at 300K. Here we varied the fin width of a double gate FinFET from 1nm to 100nm. For every finwidth a set of results was obtained and a corresponding plot of the transfer characteristics was obtained. The drain current at different finwidths was then compared at a given gate voltage.

Firstly, we varied the gate voltage (at a constant drain voltage of 0.1V) and obtained the corresponding values of drain current (figure 4 and 5); Secondly we varied the drain voltage (at a constant gate voltage of 0.1V) and obtained the drain current (figure 6 and 7).

We observed that, as the fin width is increased, the drain current also increases for a given gate voltage. For higher values of fin width, the drain current saturates at a value greater than that for the lower values of fin width. The current increases linearly as the gate bias moves from negative to positive and finally attains a saturation value.

Figure 5 shows the variation of drain current as a function of gate voltage at lower fin widths, i.e. from 1nm to 80nm in a logarithmic scale, since at much higher fin widths the short channel effects are very prominent. Here also, we observe that as the fin width increases the drain current also increases but at much lesser short channel effects than that observed in very high fin widths.

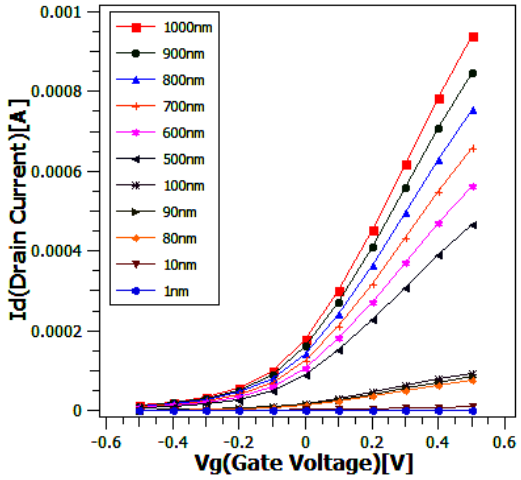

Fig 4 V_g vs. I_d plot at various fin widths from 1nm to 1000nm

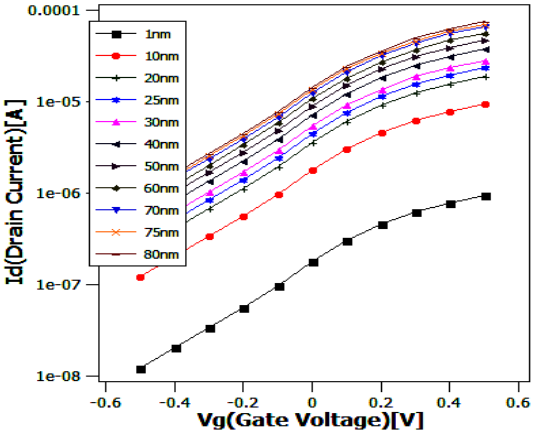

Fig 5 V_g vs. I_d plot at various lower fin widths ranging from 1nm to 80nm in Logarithmic Scale

Whereas when we study the drain current as a function of drain voltage at a constant value of gate voltage, we observe that, for higher values of fin width when the bias is negative i.e. for negative values of drain voltage, the drain current is

less than that for the lower fin widths. But as the bias moves from negative to positive the drain current increases for that of higher fin widths, and saturates at a current higher than that for the lower fin widths. Thus, as we study the drain current as a function of drain voltage, we observe that the drain current initially increases linearly and then attains a constant value for higher values of fin width whereas, for lower values of fin width the drain current remains almost constant at a value lower than that for higher fin width. Thus greater the fin width, greater is the performance of the FinFET.

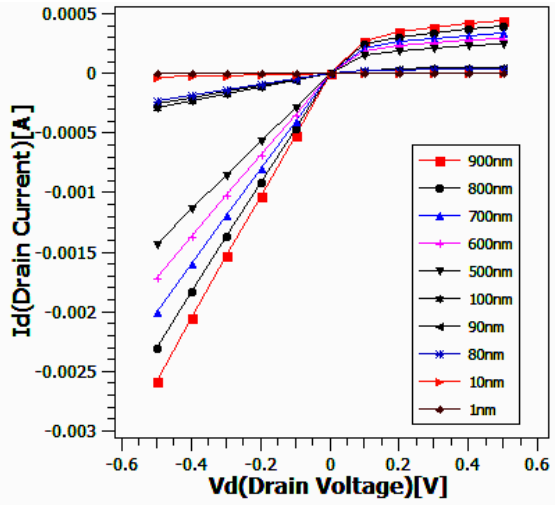

Fig6V_d vs. I_d plot at various fin widths from 1nm to 100nm

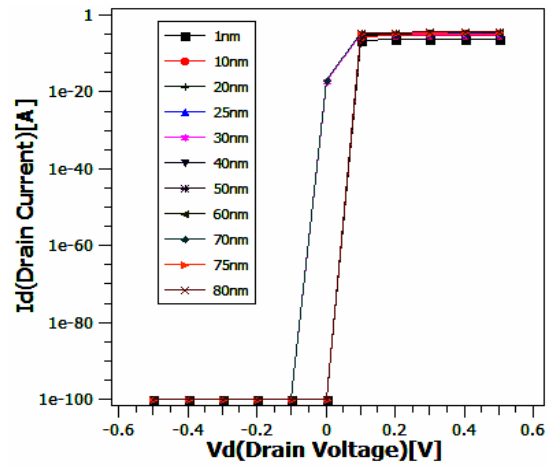

Fig 7 V_d vs. I_d plot at various lower fin widths, ranging from 1nm to 80nm in Logarithmic Scale

Figure 7 shows the variation of drain current as a function of drain voltage at lower fin widths in a logarithmic scale. It is observed that the initially current is very small for all the fin widths. But as the drain voltage moves from negative to positive bias there is a rapid increase in the drain current up until it reaches saturation. For fin widths 30nm and drain voltage surge is at -0.1V whereas for fin widths less than 30nm, the surge is observed at 0V. Thus we observe that as the fin width is increased the threshold voltage decreases which leads to drain induced barrier lowering and hence there is an increase in the short channel effects. The drain currents of all the fin widths attain saturation at almost the same drain voltage.

4. CONCLUSION

A 20nm gate length FinFET has been fabricated and analyzed in 2D using the Visual TCAD software at a supply voltage of 0.1 V. The transfer characteristics of the FinFET under different fin widths have been obtained and the comparison of the transfer characteristics at different fin widths has been studied. At shorter fin widths, the control over the short channel effects is good but the source to drain resistance increases which leads to a decrease in drain current. Thus we conclude that at lower values of fin width the drain current is less and increasing the fin width leads to an increase in drain current and hence improve the device performance. But at higher fin widths, the control over the short channel effects is less. Hence, the fin width must be selected in order to compensate for both the short channel effects and the drain to source resistance.

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