Design of Low Power, High Gain PLL using CS-VCO on 180nm Technology

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ABSTRACT
This paper investigates the design and performance of the PLL (Phase Locked Loop). The proposed PLL designed with PFD (Phase Frequency Detector), CP (Charge Pump), first order Low Pass Filter and CS-VCO (Current Starved-Voltage Control Oscillator), in this paper the designed PFD used for proposed PLL is free from dead zone. The VCO used for the designed PLL shows larger tuning range and high gain as compares to previous work, i.e. tuning range (167MHz – 1.711GHz) and VCO gain (2.21GHz/V or $13.875*10^9$ radians/s*V). In the proposed work, the designed PLL has higher pull-in range 950MHz (50MHz – 1GHz) with maximum jitter 9.8ps. Power dissipation for proposed PLL system is low, i.e. 277.2 µW with maximum pull-in time is 265ns at 1GHz. The proposed PLL circuit is implemented on CADENCE UMC0.18um process technology file with supply voltage 1.8V. All simulations are done using cadence spectre simulator.

Keywords
PLL, PFD, CS-VCO, Concepts of Lock range, Lock time, Jitter, Dead zone and passive Low pass filters.

1. INTRODUCTION
The PLL is the most important and developing part of Digital electronics, Communication (Wireless and wire-line) and High-speed (Low propagation delay) digital systems. A PLL designed by Integrated CMOS has achieved the great importance in the last few decades because of the high performance system design in the digital and communication area. It is basically used in clock generator, frequency synthesizer and also used as a data/clock recovery systems in computer, radio-frequency domain and communication system. For designing the PLL wider tuning range, VCO of High gain and high frequency range of operation are required. Basically PLL constitute of PFD (Phase Frequency Detector), Charge pump, Loop filter and VCO (Voltage Control Oscillator), these three are the basic building blocks of the PLL.

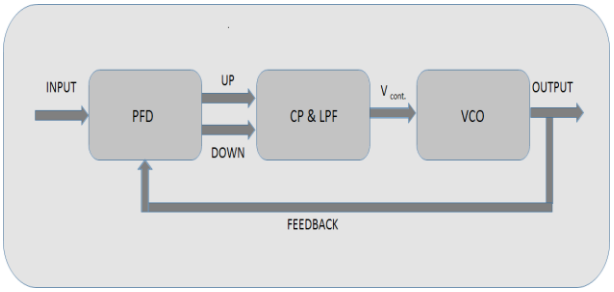

Fig 1: Basic Building Block of PLL

A PFD (Phase Frequency Detector) is basically used to compare the phase of feedback signal from VCO with the phase of input reference signal and generate outputs (UP or DOWN) according to the Phase difference. The Charge pump charges or discharges the capacitor of the Low pass filter according to the UP or DOWN signal of the PFD, and VCO increases or decreases output frequency according to the control voltage produced by the charge pump. The basic block diagram of the PLL is shown in the Figure-1.

In the previous work [2], [3] and [5], the PLL was designed on the 0.18um technology. The proposed circuit is designed on a similar technology with some improvement, i.e. the High VCO-Gain, larger Tuning range of VCO, greater Lock range with Low power Dissipation and less jitter as compare to the previous work. In this paper, the proposed PLL introduction explained theoretically in the section-1. Section-2 represents the PLL circuit description. Section-3 describes the analysis of proposed PLL circuit in locked state. Section-4 shows all the simulation results and Section –5 concludes the proposed work.

2. PROPOSED PLL CIRCUIT DESCRIPTION

2.1 PFD (Phase Frequency Detector)
The Phase Frequency Detector (PFD) generate a phase error (UP/DOWN) signal by comparing phase of input (reference) signal and VCO output signal. UP signal will be HIGH when phase of input (reference) signal leads to VCO output signal otherwise DOWN signal will be HIGH.

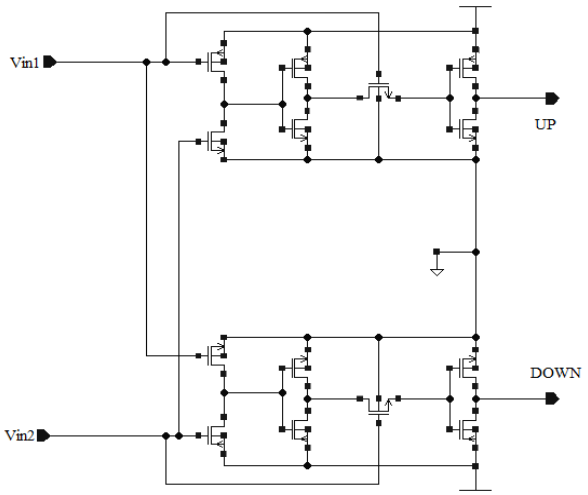

Fig 2: Proposed PFD circuit

Figure-2 shows the Phase Frequency Detector of the proposed PLL designed by the help of four inverters, two pass transistors, two NMOS and two PMOS [1]. The proposed PFD is Dead zone free due to the absence of the reset circuitry so that PFD will be produced proper output for any difference in phase of input reference signal and output signal of VCO.

2.2 CP and LPF

Charge pump (CP) basically used to convert the digital output of PFD into a current signal, so that a stable controllable signal is generated for oscillator to control the oscillation frequency. Charge pump stores the charge in the capacitor of Loop Filter.

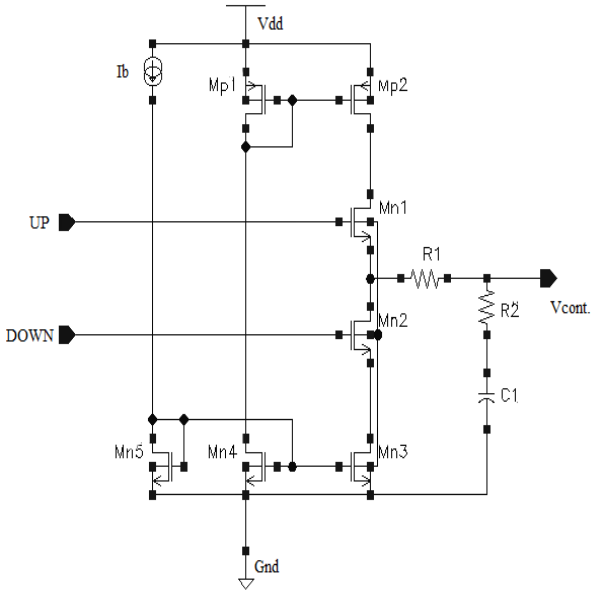

Fig 3: CP and LPF

Low Pass Filter (LPF) in the proposed circuit is used to filter out noise (High Frequency Data) from PFD and to store the charge from CP and provide analog voltage to CS-VCO.

Figure–3 shows the schematic of proposed Charge pump (CP) [2] and Low Pass Filter (LPF) [3], operated by the UP and DOWN signals generated by the PFD. When UP signal is HIGH transistor MN1 will be ON and capacitor of LPF starts charging, and when DOWN signal is HIGH transistor MN2 will be ON and capacitor of LPF starts discharging.

Table 1. Sizing of CP

Mos-transistor	Aspect ratio
Mp1,Mp2 (nm)	$^{600}/_{180}$
Mn1 - Mn5 (nm)	$^{240}/_{180}$

2.3 Proposed VCO for PLL

VCO plays a vital role in the designing of PLL. Basic function of VCO is to increase or decrease the output frequency according to the input control voltage

Figure–4 shows the proposed schematic diagram of CS-VCO (Current Starved Voltage Controlled Oscillator) [3]. In this schematic MP2 and MN2 transistor work as a current limiter for inverter (MP7 and MN7). For five stage CS-VCO, five such inverter with current limiter transistor connected in series. Proposed VCO generates sinusoidal oscillations and last inverter (MP12 and MN12) is used to convert the sinusoidal wave to square wave. Table-2 shows sizing of CS-VCO.

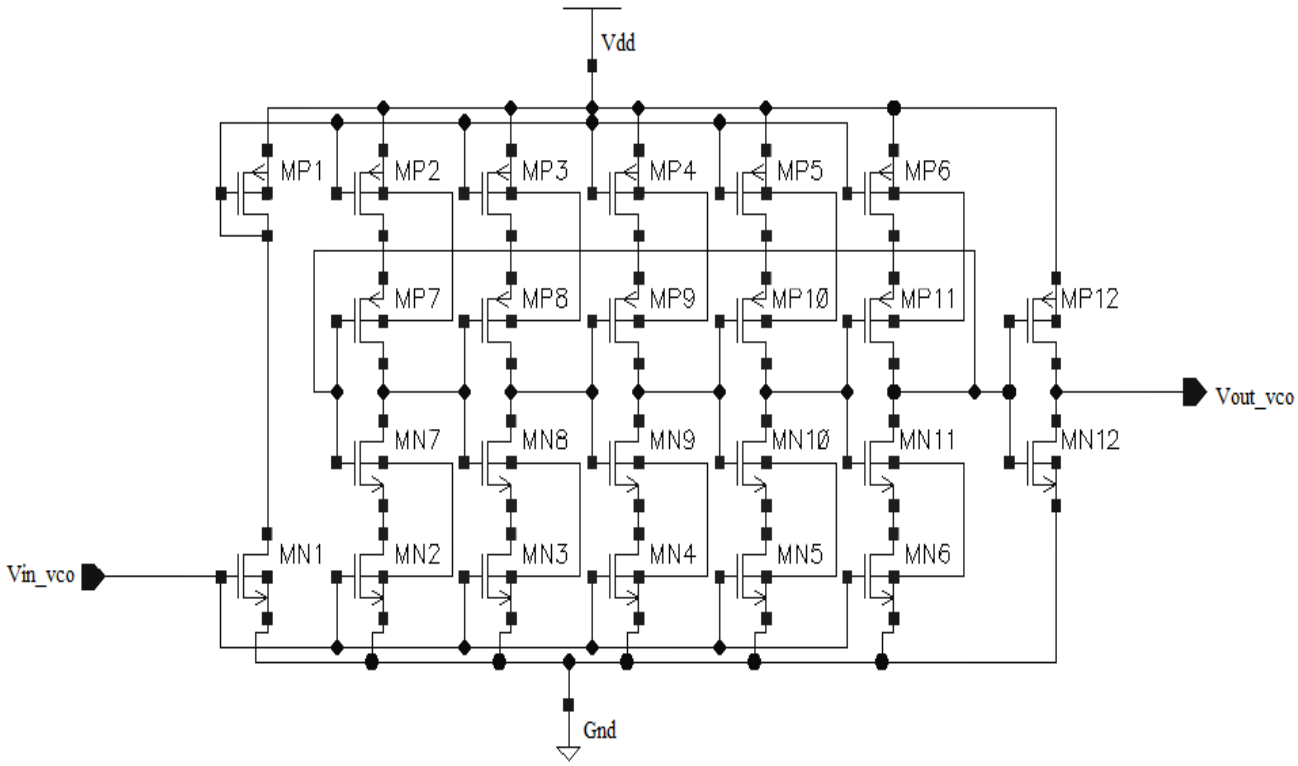

Fig 4: CS-VCO

Table 2. Sizing of CS-VCO

Mos-transistor	Aspect ratio
PM1 – PM6 (nm)	$^{1800}/_{180}$
PM7 – PM11 (nm)	$^{900}/_{180}$
PM12 (nm)	$^{460}/_{180}$
NM1 – NM11 (nm)	$^{400}/_{180}$

3. ANALYSIS OF PLL IN LOCKED STATE

Figure–5 shows the linear model of proposed PLL. In which $G_1(s)$ is the transfer function of PFD, CP and LPF, and $G_2(S)$ is the transfer function of VCO.

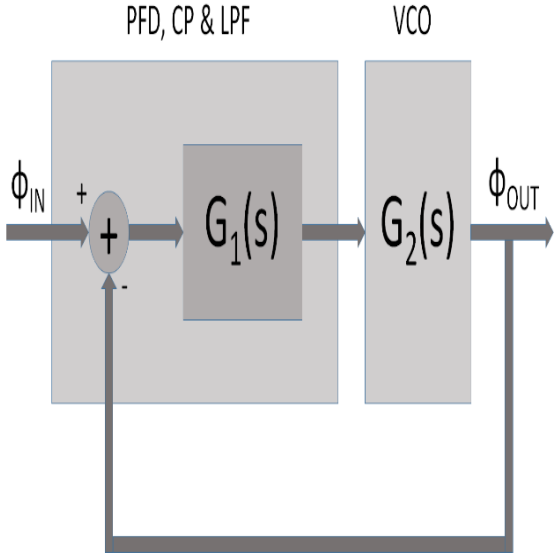

Fig 5: Linear Model of PLL

Equivalent T.F. of PFD, CP and LPF as [4]-

$$G_1(s) = \frac{I_{cp}}{2\pi}\left(R_1 + {}^{1}/_{C_0 s}\right) \quad (1)$$

T.F. of VCO as [4]-

$$G_2(s) = \frac{K_{vco}}{s} \quad (2)$$

Open loop T.F. of proposed PLL is-

$$H(s)_{open} = G_1(s).G_2(s) \quad (3)$$

$$H(s)_{open} = \frac{I_{cp}}{2\pi}\left[R_1 + 1/(C_0.s)\right].\frac{I_{vco}}{s} \quad (4)$$

Closed loop T.F. of this PLL is-

$$H(s)_{close} = \frac{\varphi_{out}}{\varphi_{in}}(s) = \frac{H(s)_{open}}{1-H(s)_{open}} \quad (5)$$

$$\frac{\varphi_{out}}{\varphi_{in}}(s) = \frac{\frac{I_{cp}.K_{vco}}{2\pi C_0}(R_1.C_0.s+1)}{s^2+\frac{I_{cp}}{2\pi}.K_{vco}.R_1 s+\frac{I_{cp}}{2\pi C_0}.K_{vco}} \quad (6)$$

Relation in Phase and Frequency-

$$\omega = \frac{d\varphi}{dt} \quad (7)$$

Since the phase and frequency related by a linear operator, eq.-(6) also applies to input and output variations of frequency-

$$\frac{\omega_{out}}{\omega_{in}}(s) = \frac{\frac{I_{cp}.K_{vco}}{2\pi C_0}(R_1.C_0.s+1)}{s^2+\frac{I_{cp}}{2\pi}.K_{vco}.R_1 s+\frac{I_{cp}}{2\pi C_0}.K_{vco}} \quad (8)$$

According to eq.-(6) and eq.-(8)

When φ_{in}/ω_{in} changes very slowly, i.e. ($s\rightarrow 0$) then $H(s)_{close}$ will be one and $\varphi_{out}/\omega_{out}$ change according to φ_{in}/ω_{in} means PLL in locked state.

When φ_{in}/ω_{in} changes abruptly, but after enough time to settle the system, i.e. ($s\rightarrow 0$) then $H(s)_{close}$ will be one and $\varphi_{out}/\omega_{out}$ tracks the φ_{in}/ω_{in} means PLL in locked state.

4. SIMULATION RESULTS

4.1 Transient Response of PFD

Figure-6 shows the transient response of PFD. Two pulse signals of different frequencies are connected to the inputs of Phase Frequency Detector, and resulted signal (UP/DOWN) is observed at output terminals of PFD.

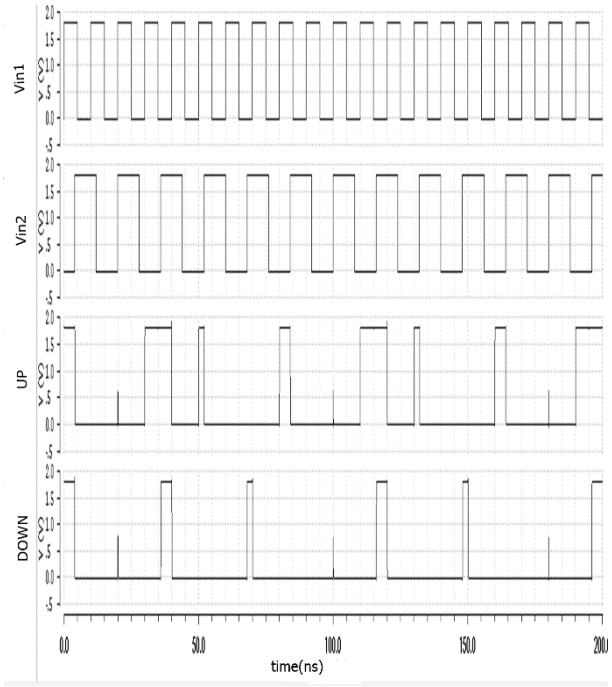

Fig 6: Transient Analysis of PFD

According to this whenever phase of Vin1 signal lead to the phase of Vin2 signal, UP will be HIGH, and when phase of Vin2 signal leads to the phase of Vin1 signal, DOWN will be HIGH.

4.2 Transient Response of CS-VCO

Figure-7 shows the transient response of CS-VCO.

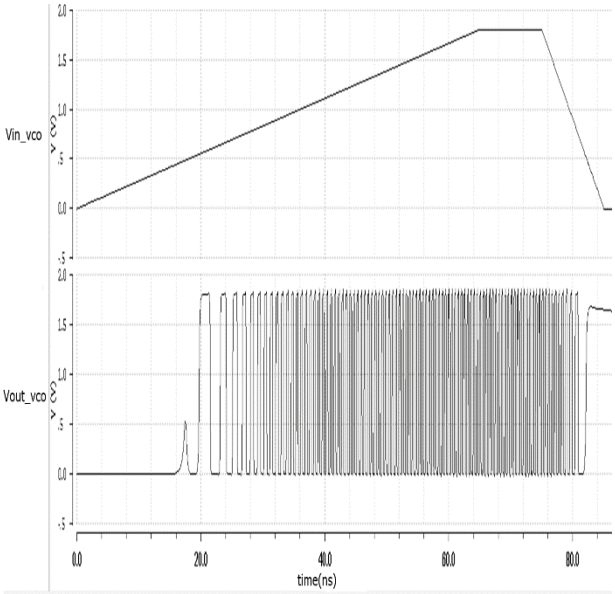

Fig 7: Transient Analysis of CS-VCO

A ramp signal (0.0 V-1.8 V) is connected to the input of VCO as control voltage and corresponding oscillation frequency is observed at VCO output terminal.

4.3 Periodic Steady State Analysis of CS-VCO

Figure-8 shows the tuning range of CS-VCO by the Periodic Steady State (PSS) analysis. Tuning range of CS-VCO is 167.22MHz – 1.711GHz is obtained because in this region plot is almost linear for the control voltage 540mV – 1.24 V.

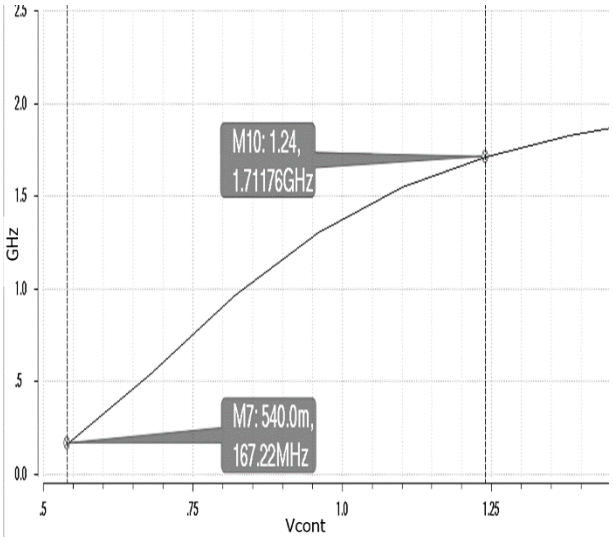

Fig 8: PSS Analysis of CS-VCO

VCO Gain can be calculated as [3] -

$$[K_{vco} = 2\pi * \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \text{ radians/sV}] \qquad (9)$$

From equation (9) Kvco is 13.875*10^9 radians/sV ***or*** 2.21 GHz/V.

4.4 Transient Analysis of PLL

Figure-9 shows the transient response of PLL. A pulse signal of 1GHz frequency is connected to input reference terminal of the PLL and second input terminal of the PLL is connected with its output terminal, and results are observed as-

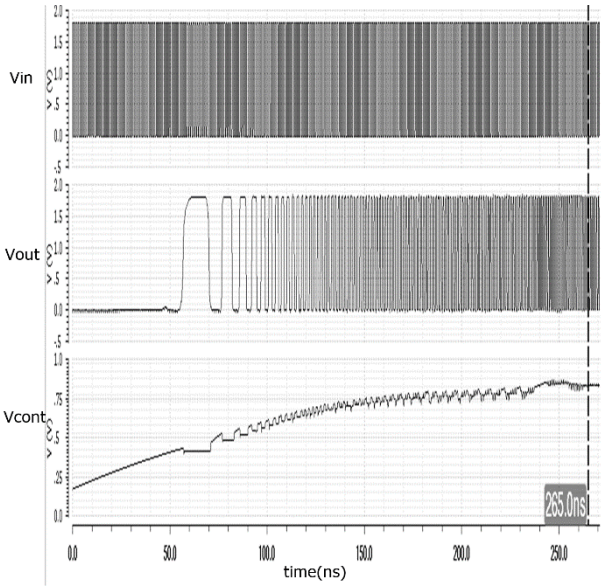

Fig 9: Transient Analysis of PLL

In the PLL, initially control voltage starts increasing according to oscillation frequency, but after some time oscillations get sustained, and control voltage became constant and at this time locking starts. Locking range of the proposed PLL is 950MHz (50MHz – 1GHz).

4.5 Locking Plot of PLL

In figure-10 VCO output signal shows in blue, reference signal in red and control voltage in black. By overlapping them, it is clear that VCO output locked with input reference and control voltage is constant.

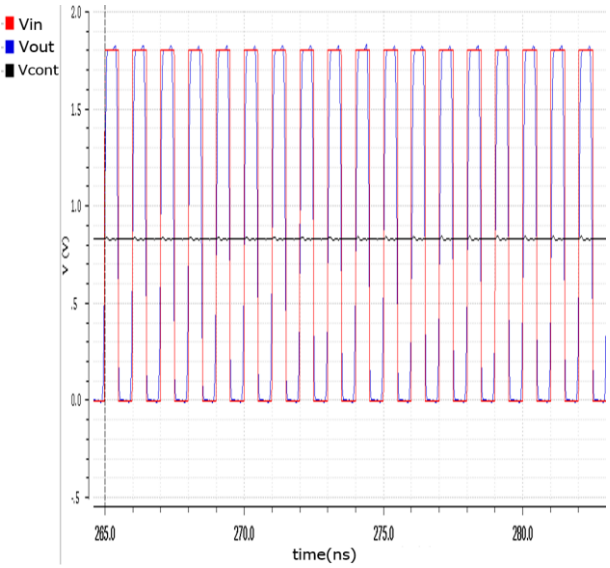

Fig 10: Locking Plot of PLL

Locking (Pull-In) time of designed PLL at 1GHz is 265ns.

4.6 Power Dissipation of PLL

Figure-11 shows the total power dissipation by the PLL system.

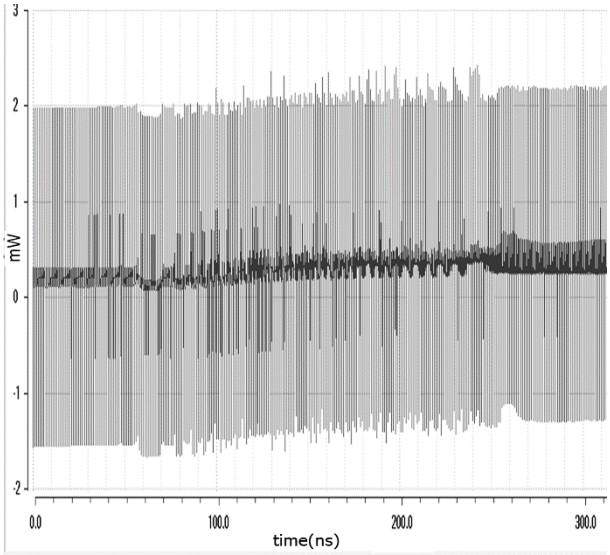

Fig 11: Power Dissipation of PLL

Total power dissipation is calculated as [3]-

$$[P_{avg} = V_{dd} * I_{avg} = V_{dd} * I_{dd}] \quad (10)$$

From the above expression P_{avg} is 277.2µW.

4.7 Eye Diagram of PLL

Figure-12 shows the Eye diagram of PLL at 1GHz.

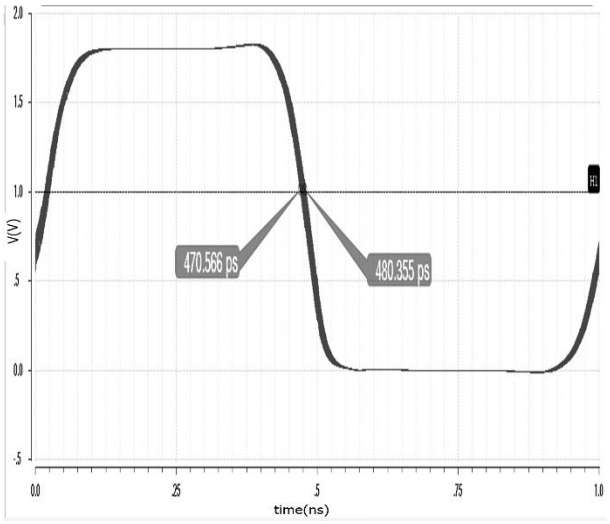

Fig 12: Eye Diagram of PLL

By this method calculated Jitter is 9.8p seconds [2].

Table 3. Comparison table of proposed PLL

Reference	**Proposed Work**	**[5]**	**[2]**	**[3]**
Technology	CMOS 180nm	CMOS 180nm	CMOS 180nm	CMOS 180nm
Supply Voltage (V)	1.8	1.8	1.8	1.8
Tuning Range (MHz)	167 - 1711	320 - 960	500 - 1500	431 - 1796
Power Dissipation (mW)	0.27	20	0.32	7.08
Pull-In Time (ns)	265	330	--	54
VCO Gain (GHz/V)	2.21	1.72	--	1.48
Jitter (ps)	9.8	--	24	--
Pull-In Range (MHz)	50 - 1000	--	--	357 - 900

5. CONCLUSION

In the proposed paper PLL is implemented on CADENCE UMC180nm process technology with an improved lock range 950MHz (50MHz–1 GHz) which is very large as compared to previous work [2], [3] and [5]. Proposed PFD is dead zone free and it has less area as compared to conventional PFD due to absence of reset circuitry, also high gain 2.21GHz/V and larger tuning range 167MHz – 1.711GHz is achieved in designed CS-VCO. Simulation of this PLL circuit is done using spectre simulator of CADENCE and improved simulation results are obtained, i.e. power dissipation 277.2 µW and jitter 9.8ps at 1GHz.

6. REFERENCE

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