Area Efficient Layout Design of CMOS Comparator using PTL Logic

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ABSTRACT

Comparator is a very useful combinational logic circuit. In this paper performance analysis of CMOS Comparator and PTL logic design has been shown. In the design of integrated circuits, several logic families is being used which is described by Pass Transistor Logic (PTL). It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. The layout of 2-bit comparator is developed using automatic and semi-custom techniques. Both the layouts are compared and analyzed in terms of their area consumption. Automatic layout is generated from its equivalent schematic whereas semi-custom layout is optimized manually. The result shows that semi-custom layout of PTL logic consumes 35% less area as compared to CMOS logic design to provide area efficient solution.

Keywords

CMOS technology, Layout, Performance analysis, logic circuits, PTL

1. INTRODUCTION

Comparator is a very useful combinational logic circuit & a basic arithmetic component of digital system. In many computers and other kinds of device processors, subtractors are used not only for the arithmetic calculations, but are also frequently used in other parts of the processor, where there is a requirement of calculating addresses, table indices, and similar operations[1]. Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and depending upon the condition of these inputs it produce an output. In Very Large Scale Integrated designs, Comparators are the common devices. In other words, in a given technology, transistors are required to compensate the reduction of supply voltage to achieve high speed, larger, which also means that more die area and power is needed [2]. For comparator with short input, this is suitable approach.The circuit complexity increases drastically for the comparator with longer inputs, accordingly operating speed is degraded. In the world of technology it has become essential to develop various new design methodologies to reduce the power and area consumption [3]. Most of the developed low-power SRAM techniques are used to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. An SRAM cell is to reduce the power in write operation by introducing two tail Transistors in the pull-down path for reducing leakages [4]. Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the

sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption [5]. Scaling down of the technology has led to increase in leakage current. Nowadays, a leakage power has become more dominant as compared to Dynamic power. Leakage current is a primary concern for low-power, high-performance digital CMOS circuits [6]. In one complete cycle of CMOS logic, current go from VDD to the load capacitance to charge it and then go from the charged load capacitance to ground during discharge. Due to this one complete charge/discharge cycle, a total of Q=CLVDD thus transferred from VDD to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage [7].

In almost all digital processors, Comparator is a fundamental operation. In the last few years, a great deal of attention has received by the design of high-speed, low power, and area-efficient binary comparators since, as is well known, The examples of efficient architectures of binary comparators are demonstrated in [8]–[12]. In this paper, a comparative analysis about the Area and Power of different logic design of comparator has been presented. Furthermore, based on the comparator proposed in [13], a comparator is presented which consumes so much area and power on the other hand area can be reduced by making these circuit by semi custom technique. This modification results in considerably area efficient and power efficient when compared with the other one. 2-Bit Magnitude Comparator compares two numbers in which A0, A1, B0 and B1 are the two inputs and three outputs i.e $A > B, A = B, A < B$ and only one of the three outputs would be high accordingly if A is greater than or equal to or less than B. The truth table of 2-bit comparator with all possible combination is shown in Table 1

TABLE 1 Truth table of 2-bit comparator

Input				Output		
A1	A0	B1	B0	$A > B$	A=B	$A < B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0

0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

2. LOGIC STYLES

There are three types of Logic styles : CMOS, Pseudo NMOS and PTL Logic style. But here only two logic style is explained. CMOS uses both NMOS and CMOS transistors to implement logic gates in a complementary way. The symbol of CMOS Inverter is shown in fig 1. The output is shown by Y and also input is shown by A, if input A is provided by a logic 1 then both gates are at higher potential but NMOS is ON, PMOS is OFF & provide low impedance path between ground & output (Y). Therefore, output (Y) will go to level of 0V. If input A=0 (low logic) then both the gates are at zero potential & PMOS is ON & provide low impedance path from
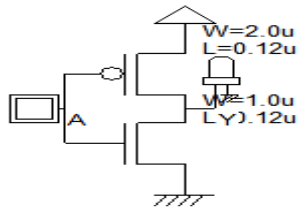
Fig. 1 Symbol of CMOS Inverter

V_{DD} to output (Y). Therefore output (Y) will go to high level of V_{DD} [14]. The principle of CMOS logic design says that Pull up network has only PMOS circuitry & Pull down network has only NMOS circuitry as shown in fig 2.
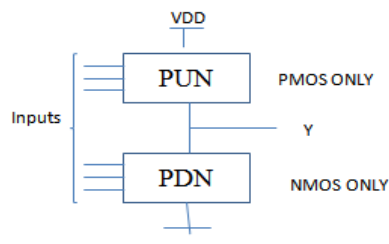

Fig. 2 Logic Network of CMOS Style

The function of PUN is to provide connection between output & VDD, similarly of PDN. This network is constructed in such a manner so that one & only one network is conducting at a time [15]. For logic operation PTL is to use purely NMOS Pass Transistors network. The source side of the logic transistor networks is connected to some input signals instead of the power lines as compared to the CMOS logic style which is the basic difference of Pass transistor logic style as shown in Fig.3. Here to pass logic levels from input to output transistor acts as switch [16].
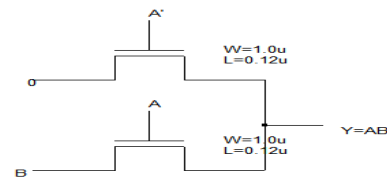

Fig. 3 AND Gate symbol using Pass Transistor Logic

3. PROPOSED COMPARATOR

Area comparison has been done using two layout designs namely auto generated, semi custom . The proposed Comparator the schematic of 2-Bit Comparator using CMOS Logic style is shown in Fig. 4. As for every input both NMOS & PMOS are used, the design requires large number of transistors. The general concept is Layout that describes the geometric representation of the circuits by means of layers and polygons. The timing diagram of Comparator is shown in below Fig.5
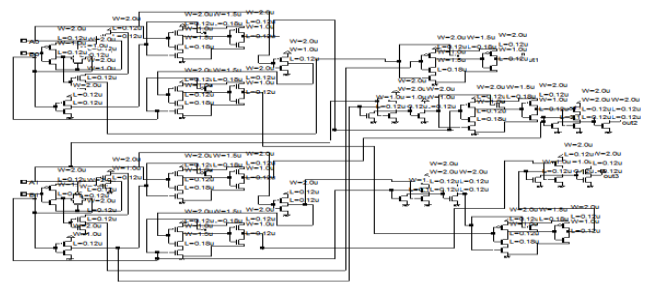

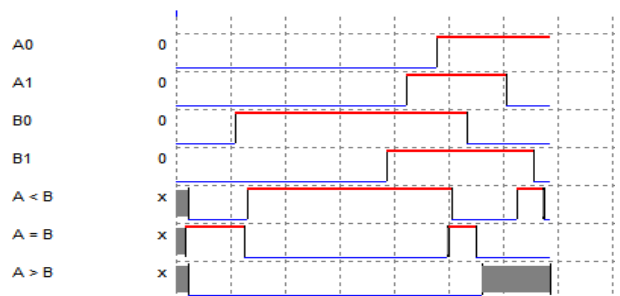**Fig. 4 Schematic of 2-bit Comparator using CMOS Logic**

Fig. 5 Timing diagram of Comparator

In this design the less number of transistors is used with respect to the CMOS logic styles because PTL uses less number of PMOS transistor as shown in fig. 6. As less number of transistor and less area is used, speed is increased.
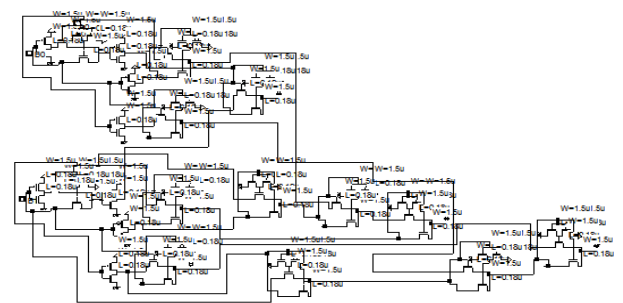

Fig. 6 Schematic of 2-bit Comparator using PTL Logic style

4. LAYOUT PERFORMANCE ANALYSIS

To generate the layout, designer used different logical layers. The automatic layout design of 2-bit comparator using CMOS logic style as shown in Fig. 7
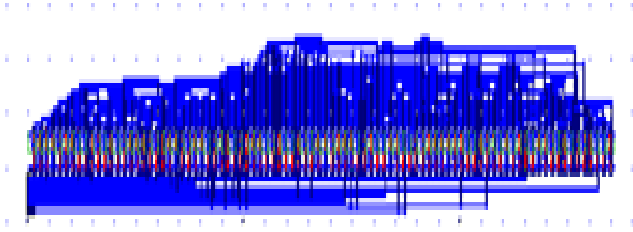

Fig. 7 Automatic layout design of CMOS logic

The automatic layout design using CMOS logic style is shown in Fig. 8. It uses less area with respect to the CMOS logic style.
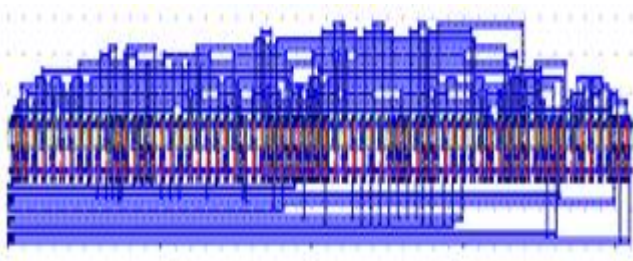

Fig. 8 Automatic layout design of PTL logic

The schematic of 2-bit Comparator is designed. Using Microwind software, the auto generated layout of 2-bit Comparator is created with 180nm foundary.
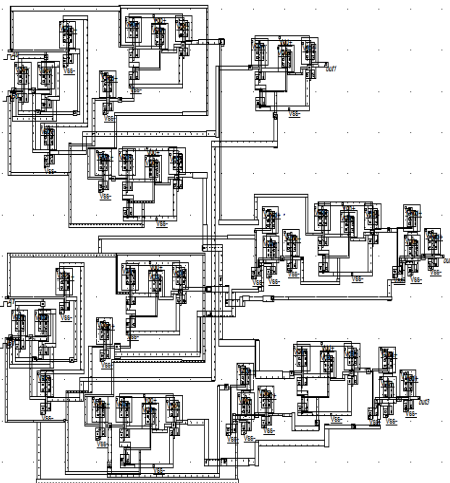

Fig.9 Semi-Custom layout of comparator using CMOS logic

The figure 9 represents the semicustom layout of CMOS logic style using nMOS, pMOS and the Comparator output waveform for the layout is shown in figure 10.
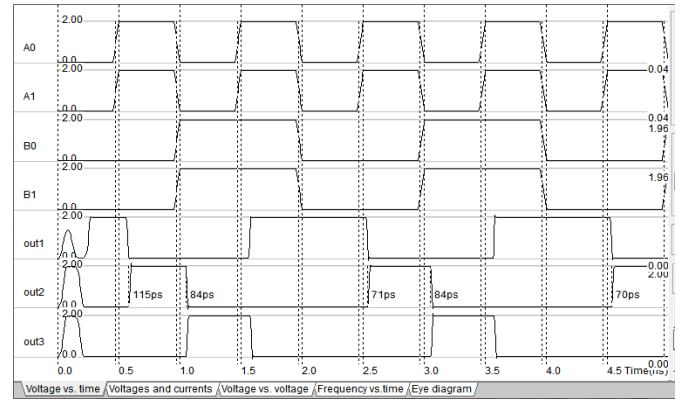

Fig.10 Comparator Output

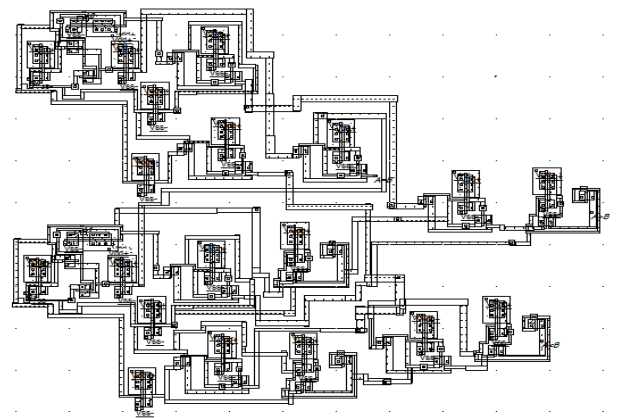The figure 11 represents the semicustom layout of comparator using PTL logic style.

Fig.11 Semi-Custom layout of comparator using PTL logic

The proposed 2-bit Comparator layout performance using different logic style is compared with semicustom approach. The performance in terms of Area is compared. Comparative analysis is shown in Table 2. The area comparison between auto generated and semi-Custom for PTL and CMOS is shown in Fig. 12 with the help of bar graph.

Table 2 Comparator Analysis for Area

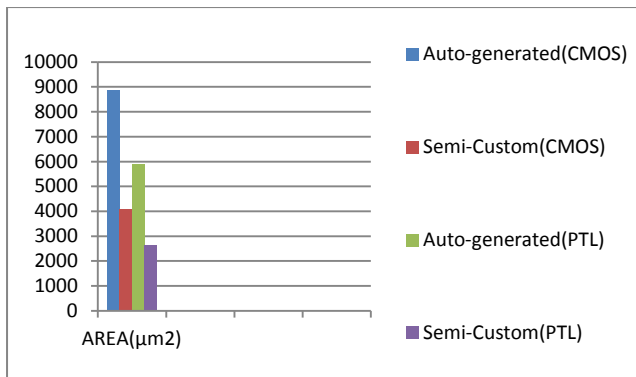| Parameter	Design Styles			
	Auto generated		Semi Custom	
	CMOS	PTL	CMOS	PTL
Area(μm^2)	8860.7	5885.9	4061.2	2629.0
Power(mW)	0.642	1.795	0.943	0.678

Fig.12 Bar graph representing Area

In terms of area the Semi-Custom layout has better performance among two design approaches using different logic style and also PTL consumes less area with respect to the CMOS logic design and power is almost the same.

5. CONCLUSION

This paper presents a comparator for 2-bit using different logic style. Area and Power estimation of PTL and CMOS logic design is shown by using semi custom and automatically generated technique. Results indicate that the proposed PTL logic style comparator occupies area 2629.0 μm^2 and 0.678 mW power than the comparable design because it uses less number of transistors or we can say speed can be improved. because of this in PTL logic style as purely NMOS transistors are used. Further improvements could be made in fully custom logic design to improve more area.

6. REFERENCES

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