Layout Design of Level Triggered Delay Register using 90 nm Technology

Meenakshi Thakur
M.E scholar ECE Department,
NITTTR, Chandigarh

Rajesh Mehra
Associate Professor ECE Department,
NITTTR, Chandigarh

ABSTRACT
This paper presents low area and power efficient delay register using CMOS transistors. The proposed register has reduced area than the conventional register. This delay register design consist of 6 NMOS and 6 PMOS. The proposed delay register circuit has been designed in logic editor and simulated using 90nm technology. Also the layout simulation and parametric analysis of modified layout has been done. Register has been designed using full automatic layout design, semicustom layout design and fullcustom layout design. Then the results of these different designs has been observed and compared in terms of area, delay and power. The simulation results show that circuit design of delay register saves the power by 17% when designed with fullcustom and area by 61.8% when designed in semicustom.

Keywords
Pass Transistor,CMOS, Power Dissipation, NMOS, PMOS,.

1. INTRODUCTION
The feature size of transistors in a VLSI becomes smaller, and switching delay becomes shorter with the advancement in process technologies. As the operation speed becomes higher, the delay variations caused by the change in process parameters, temperature, supply voltage noise, coupling noise, etc. have become a serious problem. In order to reduce the timing margin, methods for estimating delay variations more precisely were studied in [1]. Flip flops are the basic circuits used for storage of bits, in shift registers, amplifiers, counters and synchronizer applications. The demand of miniature and portable accessories is raising fast with time. So designer has to consider the various features like silicon area, longer life, high speed, reliability and weight of the device while designing. Also battery life and area consumption is limitation of many portable devices. Sophistication of the devices can be increased by using the proper CMOS designs. Moreover the improvement in term of reduction in feature size, metal interconnects are used to connect the CMOS devices within the chip [2]. So a plenty of logical styles have been developed to improve the power consumption and area, delays are also minimized [3,4]. Also latches and flip-flop straight away affect the speed and power consumption of systems [5]. Due to the reduction in the basic size of CMOS circuit the issue of power dissipation arises. The power in read and write operation can be reduced by introducing two tail transistor in pulldown path for reducing leakages [6]. Also forced sleep transistors are used which works during active mode and turned off during sleep mode to avoid the leakage [7]. The total power dissipation in cmos circuit is the some of static power dissipation, short circuit dissipation and dynamic power dissipation.

$$P_{total} = P_s + P_d + P_{sc} \quad (1)$$

Also to get optimized time domain performance it is required to adjust transistor dimensions individually [8,9]. Edge-triggered flip flops are used where delays match the adequate clock period, by changing the time of activation of registers the throughput of the circuit can be maximized[10].The D input must be held stable until the output Q appears. Also to increase the efficiency of the circuit double edge triggered flip flops can also be used [11]. Edge triggered register ensures that the result is written in instant and then the input close, and these allow the system to complete its operation in orderly and stable way.

2. REGISTER DESIGN
Flip flop is a two state circuit that is used to store the information. The circuit design can be positive edge triggered or negative edge triggered. The pulse at the control input cause the triggering of flip flop from one state to another [12]. The basic diagram for D flip flop is shown in Figure 1.

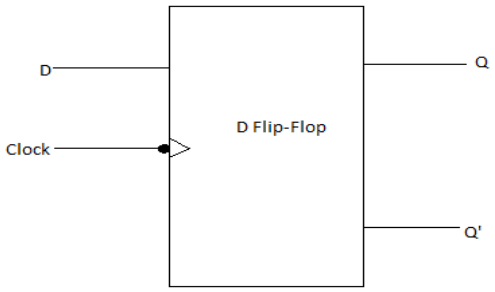

Fig 1: Diagram of D flip flop

In synchronous systems both the positive edge triggered and negative edge triggered circuits can be used. The observed output of D flip flop is shown in table 1. D flip flop hold the value of D input at a definite portion of the clock cycle, at rising edge or falling edge. The captured value becomes Q output.

Table 1. Function table of D latch

CLOCK	D	Q	Q’
Falling Edge	0	0	1
Falling Edge	1	1	0
Non-Falling Edge	X	Q	Q’

The clock output of delay register is shown in Figure 2, which shows the accurate working of delay register.

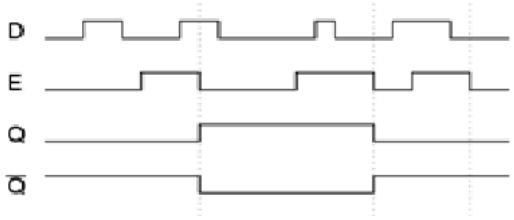

Fig 2: Wave shapes for negative edge delay register[13]

The flip flop equation is

$$Qn=D \qquad (2)$$

The logic diagram of Delay register using logic gate i.e five NAND gate is shown in Figure 3 .

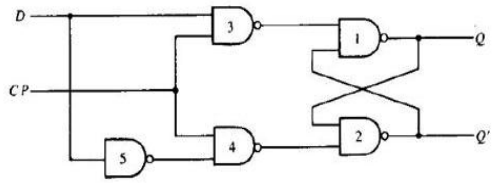

Fig 3: Logic diagram of delay register [12]

Conventional CMOS Technology uses two types of transistors which are nmos and pmos. And transistor operation is based on electric filed the devices are called Metal Oxide Semiconductor field effect Transistor (MOSFET). The cmos provides characteristics like high noise immunity and and low power consumption [14].

3. SCHEMATIC DESIGN

The delay register is designed using cmos logic on DSCH3.1 and shown in Figure 4.Here negative edge triggered register is shown at transistor level. In the circuit 12 cmos devices are used (6 pmos, 6 nmos).The proposed design provide an area efficient design.

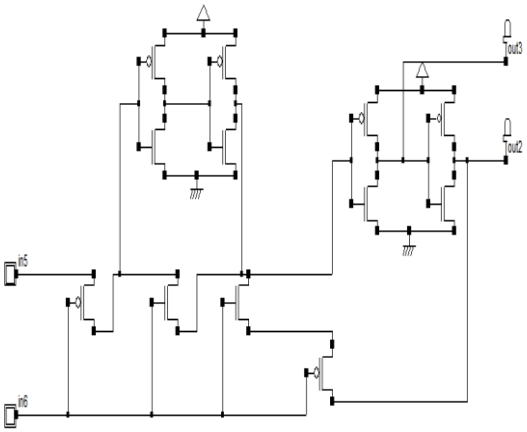

Fig 4: Logic diagram of delay register

In general , a fully complementary cmos gate has an nmos pull-down network to connect the output to 0 (GND) and pmos pull-up network to connect to output 1(VDD)[1].Now the verification and simulation of design is done .

Figure 5 shows the functioning or performance of the design.

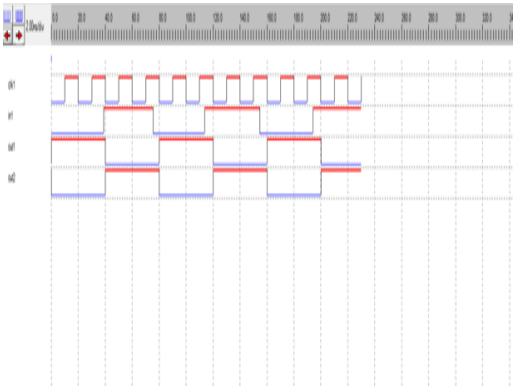

Fig 5: Simulation results on DSCH

Now the verilog file of the design is generated by the DSCH. This file is then compiled in microwind to generate the layout. The layout hence generated is fully automatic.

4. LAYOUT AND SIMULATION

Here layout using cmos logic is designed. In VLSI design manual layout designing for a very complex and will become very difficult to design large circuits. So for the accuracy over manual layout designing an automatic layout generation approach is preferred .The DSCH program is a logic editor and also provide feature of simulation. The layout of fully generated register is given in the figure 6.

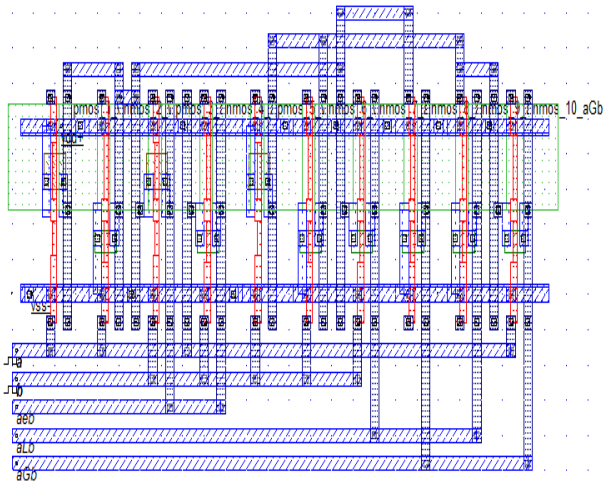

Fig 6: Full Automatic layout design

Figure 7 depicts the simulation results of the automatically generated delay register layout.

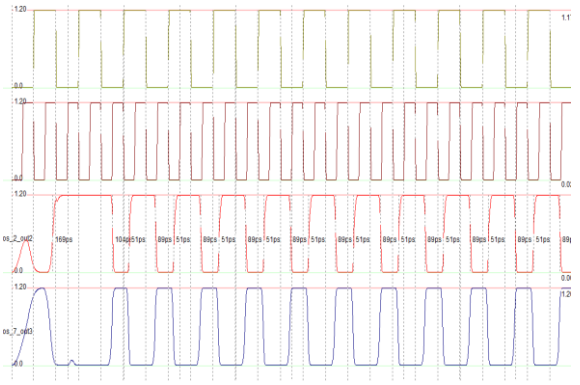

Fig 7: Full Automatic simulation results

It has been observe that in fully automatic delay register average power consumption is 27.220µw, area is 101.0µm^2.The no. of transistors used are 6 nmos and 6 PMOS.

Microwind 3.1 provides another flexible way to create the design using NMOS and PMOS devices. PMOS and NMOS cells are generated and connections are made. The advantage of this approach is that to avoid any design rule error . It has been observed that in semicustom design of delay register average power consumption is 87.731µw, area is 39.2µm ^{2}, no of transistor used is 6 NMOS and 6 PMOS. The layout of semicustom design is shown in Figure 8. Hence the complex automatic design is converted into simple design which also provide reduced area.

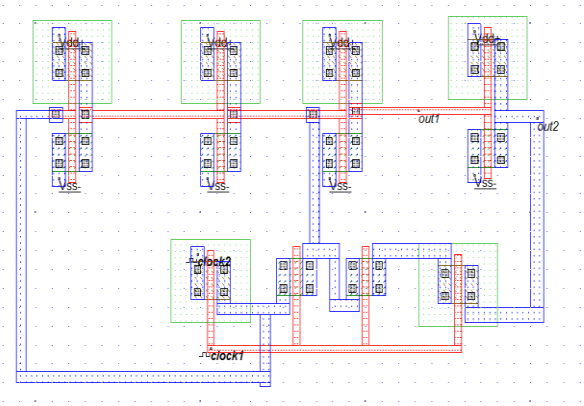

Fig 8: Layout of semicustom design on 90nm

Now the simulations results of semicustom design are are shown in Figure 9, which are similar to that of automatically generated design.

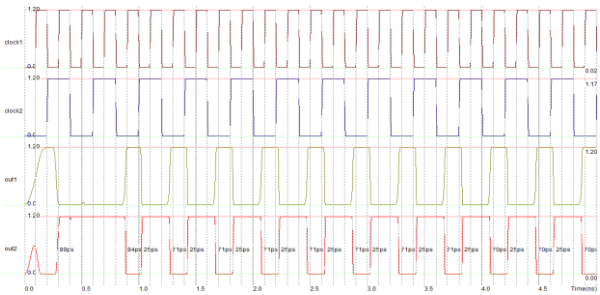

Fig 9: Semicustom simulation results

Microwind 3.1 has another important feature of designing the circuit at transistor level. The layout of PMOS and NMOS transistors is designed by selecting the p diffusion and polysilicon. After that connections are made to make the desired circuit. The routing of paths is chosen such that it uses less distance and metal which further results in the less area and power consumption. Figure 10 shows the layout design of Fully custom Design made in microwind 3.1.

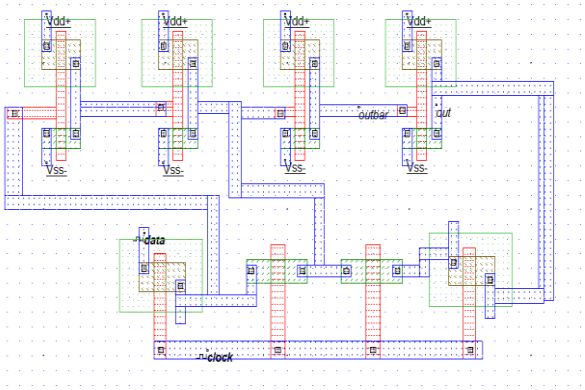

Fig 10: Fullcustom Design of Delay Register

Simulation results of fullcustom design are shown in figure 11.

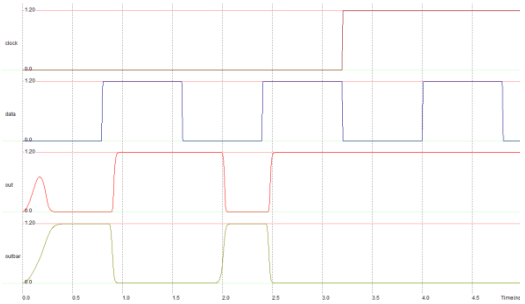

Fig 11: Simulation results of Fullcustom Design

5. RESULT ANALYSIS

In this paper a comparative analysis between fully automatic, semicustom design and fullcustom design of delay register is done which can be well analyzed in table 1. Here we compare no of gate, area, power between full automatic and semicustom layout result.

Table 2: Comparison of proposed delay register

	Fully Automatic (Design1)	**Semicustom (Design2)**	**Fullcustom (Design3)**
Power(µw)	87.220	87.731	15.425
Area (µm^2)	101.0	39.2	66.9
No. of mos devices	12	12	12

Figure 12 shows all the comparisons on bar graph as

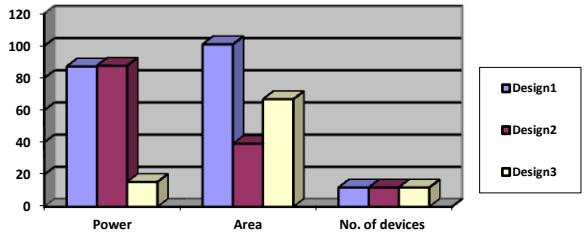

Fig 11: Simulation results of Fullcustom Design

6. CONCLUSION

Here automatic layout result with semicustom using 12 mos transistor are compared. Delay register design by fully automatic approach uses large area and power. But designing with semicustom approach the area as well as power is reduced. Area of proposed design is 101.0 on 90nm technology with fully automatic design while it is 39.2 using semicustom design. Hence area efficiency is increased by 68.1%.Also when the circuit is designed using fullcustom the consumed power is very less i.e. 15.425µw but here area increases to 66.9µm^2. Obvious, here this comparison gives better power efficiency in favour of fullcustom design.

8. REFERENCES

[1] S. Matsumoto, H. J. Mattausch, S. Ooshiro, Y. Tatsumi, M. Miura-Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N.Nakayama, "Test-circuit-based extraction of inter- and intra-chipMOSFET-performance variations for analog-design reliability," *Proc. CICC*, pp. 582–585, May 2001.

[2] Rachit Manchanda, Rajesh Mehra , "Low Propagation Delay Design of 3-bit ripple counter on 0.12 Micron Technology", International Journal of Research in Computer Applications and Robotics,Vol.1, Issue.2, pp. 7-15,March-April 2013.

[3] Neil H.E.Weste, David Harris and Ayan Banaerjee, "CMOS VLSI design " pp. 9-10.

[4] Eitenne Sicard,Sonia Delmas Bendhia, Basic of CMOS Cell Design,TATA Mc GRAW-Hill. I.S. Jacobs and C.P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, Vol. III, G.T. Rado and H. Suhl, Eds. New York, Academic, pp. 271-350, 1963.

[5] K. Rajasri, A. Bharathi, M. Manikandan, "Performance of Flip-Flop using 22nm CMOS Technology", International Journal of Innovative Research in Computer and Communication Engineering, Vol. 2, Issue 8,pp. 5272-5276,2014.

[6] Prashant Upadhyay and Rajesh Mehra, "Low Power Design of an SRAM Cell for Portable Devices'', International Conference on Computer & Communication Technology (ICCCT),pp. 255-259,2010.

[7] Pushpa saini, Rajesh Mehra, "Leakage Power Reduction in CMOS VLSI Circuits", International Journal of Computer Applications, Vol. 55, No. 8, pp. 42-48, 2012.

[8] Subodh Wairya,Rajendera Kumar Nagaria, Sudarshan tiwari, "New design methodologies for high speed mix mode full adder circuits", International Journal of VLSI and communication systems,Vol 2, Issue 2, pp. 78-98,2011.

[9] Subodh Wairya,Rajendera Kumar Nagaria, Sudarshan tiwari, "Comparitive performance analysis of XOR/XNOR Function based CMOS full adder circuit for low voltage VLSI design'', International Journal of VLSI and Communication systems,pp 221-242,2012.

[10] Boyer, aboulhamid, "optimal design of synchronous circuits using pipelining techniques'', International conference on Computer Design: VLSI in Computers and Processors(ICCD), pp. 62-67,1998.

[11] Kumar,V.M Senthil, "Design of delay buffer using shift registers for asynchronous data sampling" International conference on Power and Computing Technologies(ICCPCT), pp. 1748-1752,2014.

[12] M.Morris Mano, Digital Design, PHI, pp. 57,171.

[13] Wikipedia.org/wiki/flip-flop.

[14] Akhilesh Verma, Rajesh Mehra, "Design and Analysis of Conventional and Rationed CMOS logic", IOSR of VLSI and signal processing (IOSR-JVSR), Vol 2 , Issue 2, pp. 25-29, 2013.