Temperature Oriented Design of SRAM cell using CMOS Technology

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ABSTRACT
A set of components in a circuit which are called as modules or blocks are connected through interconnections called as 'wires'. Various computational techniques are used to calculate and minimize the area, power and speed. Single IC consists of number of Processing Elements (PE's), which works on various voltage ranges. Due to this the IC power consumption increases, thereby temperature of the chip also increases. The increased temperature in some parts is called as hotspots. The main goal of this paper is to focus on calculation of area, power and hotspot of SRAM memory circuit for 8T and 10T memory cell using Microwind.This may used to design of many complicated memory circuits for various temperature ranges. The Submicron Technology is widely used for designing any complex analog circuits.

Keywords
Submicron technology,8T memory cell,10T cell,hotspot

1. INTRODUCTION
Area minimization is also one of the major problems in chip design. In the design flow steps partitioning is used to calculate and minimize the delay and floor planning is used to calculate and minimize the area of the given circuit. In [2] a Mimetic Algorithm was used to reduce the delay in partitioning and reduce the area in floor planning method. To reduce the delay and area main concentration is to reduce clock period and power of a given circuit.

The Microwind is an EDA software used to design any complicated IC, in back-end chip design. For any circuit design the following steps are to be followed, circuit implementation, simulation, transistor level extraction and circuit verification. After all the above processes, to get an imaginary circuit layout. In [1] when power of each element increases total temperature of the circuit also increases. To avoid this increase in temperature we have to look at all current and voltage in each transistor in circuit.[14][15]

Temperature plays a major role in the design of CAD VLSI circuits. To calculate area and power of any complex circuit to find the hotspots where the temperature is high [12]. Once the hotspots are identified power and area is calculated for various temperature changes.

A memory in terms of computer hardware is a storage unit. There are many different types of hardware used for storage, such as magnetic hard drives and tapes, optical discs such as CDs and DVDs, and electronic memory in form of integrated memory or stand-alone chips. In this paper only the electronic memory, and more specifically, random access memories has been discussed. An electronic memory is used to store data or programs, and is a key component in all computers today. It is built up of small units called bits, which can hold one binary symbol of data (referred to as a '1' or a '0'). These bits are then grouped together into bytes (8 bits) or words (usually in the range of 16-64 bits). In a normal PC several layers of abstraction are then applied to make up the memory architecture, all the way from the processor's registers, for example, a file on the hard drive. Within these abstract layers of memory, several physical layers (e.g. RAM, hard drive) also exist. The main focus of this thesis is the RAM. There are four basic operations that have to be supported by a RAM. These are the writing and reading of '0' and '1' respectively.[8]

RAMs are read/write memories in which data can be written into or read from any selected address in any sequence. When a data unit is written into a given address in the RAM, the new data unit replaces address of the data unit which is previously stored in that. When a data unit is read from a given address in the RAM, the data unit remains stored and is not erased by the read operation. This non-destructive read operation can be viewed as copying the content of an address while leaving the content intact. A RAM is typically used for short-term data storage because it cannot retain stored data when power is turned off. It can be classified into SRAM and DRAM.
In this paper concentrates on design of SRAM memory cell with various transistors.

2. DESIGN OF 8T SRAM CELL
The 8T SRAM cell consists of two extra transistors MNLL and MNWL as compared to conventional 6T SRAM cell. Transistor MNLL is used to reduce gate leakage while transistor MNWL is used to make cell SNM free in the zero state. The complex 8T SRAM memory cell consists of 8 transistors, called as Processing Elements (PEs) are shown in Fig.1. The design of such complex circuit in PCB is very difficult. Only the electricians will be able to do the connections. But using EDA tools we can easily design any circuit and we can simulate for various values of input supply voltage and wirelength.

Interestingly, transistor MNLL also helps in improving SNM when cell holds logic '1'. The sign WLB is the complement of wordline (WL) signal. The timing diagram for signal WL and WLB in read/write cycle and standby mode is shown in fig.1. In this work, the basic read/write operations of 8T SRAM cells are preformed using single ended sense amplifier which are described as follows.[7]

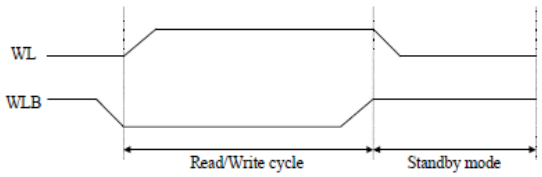

Fig.1 Timing Diagram

In write '0' operation, the bitline BT is pulled down to logic '0'. As soon as the signal WL rises from logic '0' to logic '1', transistor MNWL is turned off. The node XT starts discharging which turns ON transistor MP2 causing cell to flip and logic '0' is written into the cell. In write '1' operation, the bitline BB is pulled down to -VTN, where VTN is the threshold voltage of transistor MN4. The node XB starts discharging which turns ON transistor MP1. Once transistor MP1 is turned ON, the node XT is at logic '1' and hence logic '1' is written into the cell. In read operation, the bit lines BT and BB are held at logic '1' by the pre charged circuitry. In read '0' operation, the bit line BT starts discharging through transistors MN3 and MN1[11]. Various front end tools are available to draw the circuit with number of transistors. Fig 2 shows the pictorial model of 8T SRAM in front end using spice software [8] [9][11].

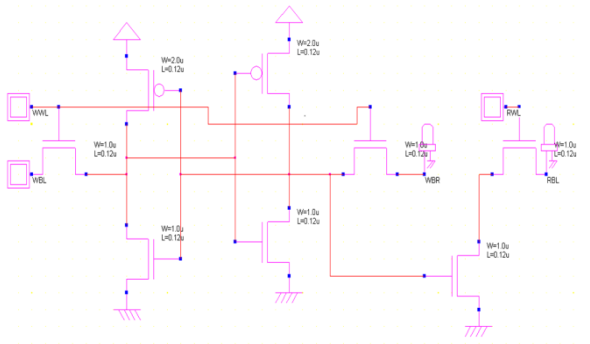

Fig.2 Design of 8T SRAM cell using Spice software

3. 8T SRAM CELL LAYOUT DESIGN

To reduce the total area and power we have to increase the length of the transistors present in the circuit. In 0.18µm technology, length of the transistor is varied from 0.6 µm to 0.12 µm, because of the increase in the length, surface area as well as power consumption of the total circuit elements will be reduced. Fig.3 shows the complete layout of the 8T cell with 0.18µmTechnology [9].

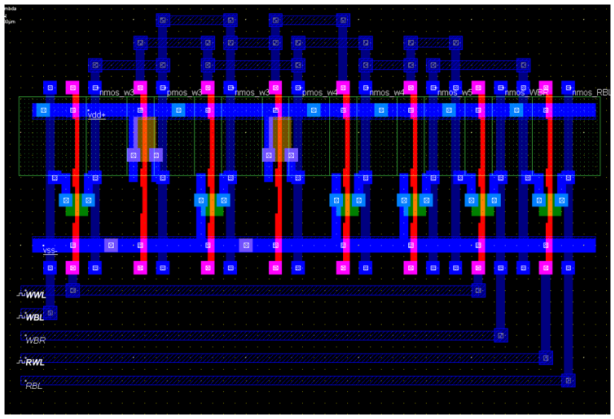

Fig.3 Layout of 8T SRAM cell

4. 8T SRAM TEMPERATURE VARIATIONS

Once the SRAM is designed using EDA tool some advanced techniques are used to model the temperature aware design. Fig 6.3 and 6.4 shows the temperature analysis design in microwind. The colors present in the design indicates the low, medium and high temperature parts in the above amplifier design. From this we observed that we have to introduce some of the resistors and capacitors to reduce the high temperature in dark color regions. Fig 6.3 shows the interconnect temperature in 0.18 micron technology. M1 and M2 represents the interconnects present in the memory cell. Fig4. shows the interconnect temperature in 0.18 micron technology. Various colors indicate total temperature spread over the total chip area. Dark color represents the hotspot i.e. high temperature present in 8T SRAM design.

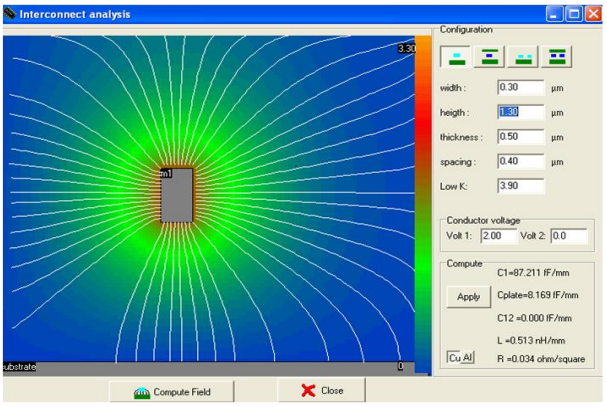

Fig. 4 Hotspot identification in 8T SRAM Cell

5. 10T SRAM CELL DESIGN

In the 10T bit cell, as shown in Fig. 5 , a separate read port comprised of 4-transistors was used, while write access mechanism and basic data storage unit are similar to standard 6T bit cell. This bit cell also offers the same benefits as the 8T bit cell, such as a non-destructive read operation and ability to operate at ultra low voltages. But the 8T bit cell does not address the problem of read bit line leakage current, which degrades the ability to read data correctly. In particularly, the problem with the isolated read-port 8T cell is analogous to that with the standard (non-isolated read-port) 6T bit cell discussed. The only difference here is that the leakage currents from the un-accessed bit cells sharing the same read bit-line, RBL, affect the same node as the read-current from the accessed bit cell. As a result, the aggregated leakage current, which depends on the data stored in all of the un-accessed bit cells, can pull-down RBL even if the accessed bit cell based on its stored value should not do so. This problem is referred as an erroneous read[3]. The erroneous read problem caused by the bit line leakage current from the un-accessed bit cells is managed by this 10T bit cell by providing two extra transistors in the read-port. These additional transistors helps to cut-off the leakage current path from RBL when RWL is low and makes it independent of the data storage nodes content.[5]

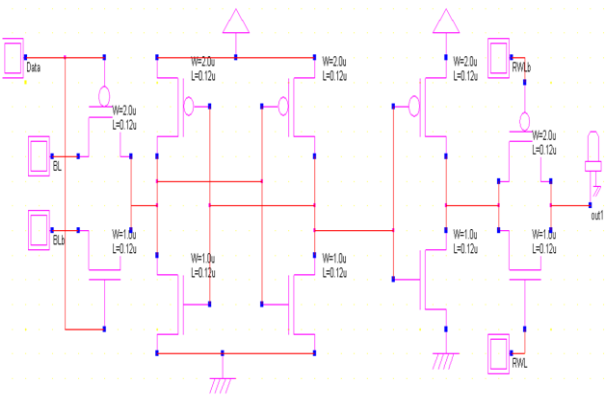

Fig 5 Design of 10T SRAM cell

6. 10T SRAM CELL LAYOUT DESIGN

To reduce the total area and power in 0.18µm technology, length of the transistor is varied from 0.6 µm to 0.12 µm, because of the increase in the length, surface area as well as power consumption of the total circuit elements will be reduced. Fig.6 shows the complete layout of the 10T cell with 0.18 µmTechnology[2].

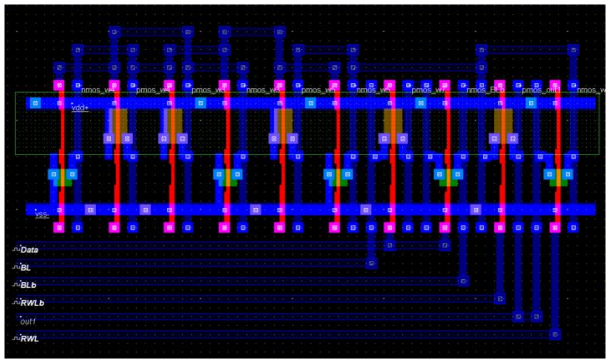

Fig. 6 Layout of 10T SRAM cell

7. 10T SRAM WITH TEMPERATURE VARIATIONS

Once the SRAM is designed using EDA tool some advanced techniques are used to model the temperature aware design. Fig. 7 shows the temperature analysis design in microwind. The colors present in the design indicates the low, medium and high temperature parts in the above amplifier design. From this we observe that we have to introduce some of the resistors and capacitors to reduce the high temperature in dark color regions. Fig 7. shows the interconnect temperature in 0.18 micron technology. M1 and m2 represents the interconnects present in the memory cell[3][4]. It also shows the interconnect temperature in 0.18 micron technology. Various colors indicate total temperature spread over the total chip area. Dark color represents the hotspot i.e. high temperature present in 10T SRAM design [12][13][16].

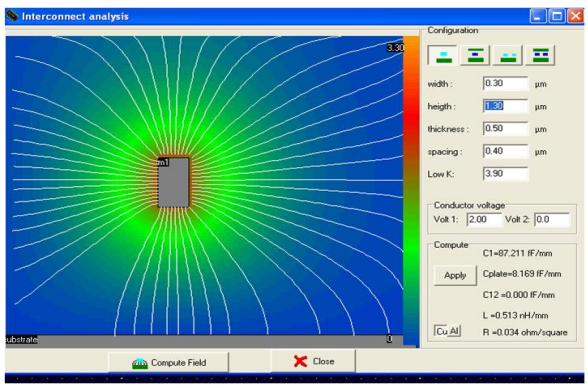

Fig.7 Temperature analysis of 10T SRAM cell

8. DESIGN OF ROW AND COLUMN DECODER

From the above results, 10T SRAM cell design is most widely used in CMOS circuits. This work explains the various circuit components present in 10T SRAM structure. First concentrate on design of decoder, decoder is a digital logic circuit which takes multiple coded input and converts to coded multiple outputs where the input and output codes are different. The decoding is necessary in applications like data multiplexing, 7 Segment display and memory address decoding. The simple example of the decoder is an AND gate, the AND gate output will be high when all the inputs are high, this output is also known as active high output. A little more complex decoder is the n-2n binary decoders. These decoders convert n coded input to 2n unique outputs. the decoder circuit for 2 coded inputs to 4 coded outputs. It consists of 2 NOT logic gates and 4 AND logic gates. The output of the 2:4 decoders further clarified from its inputs like r1, r2 and outputs like WL1, WL2, and WL3 AND WL4. Figure 3 and 4 shows the inputs r1, r2 and corresponding outputs [8].

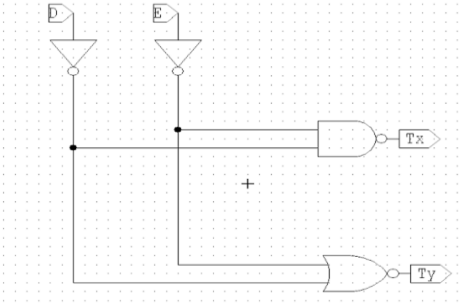

Fig. 8 Design of 4:2 Row Decoder circuit

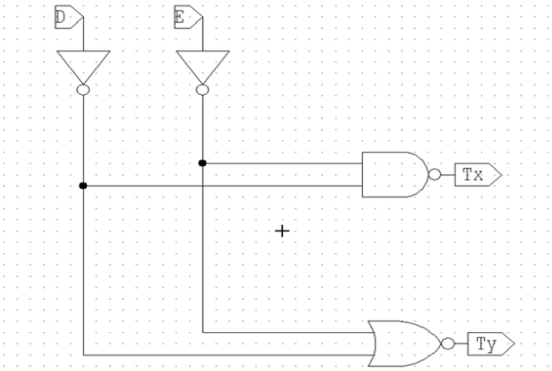

Fig. 9.Design of 4:2 Column Decoder circuit

9. DESIGN OF SENSE AMPLIFIER

Sense amplifiers (SA) are an important component in memory design. The choice and design of a SA defines the robustness of bit line sensing, impacting the read speed and power due to the variety of SAs in semiconductor memories and the impact they have on the final specs of the memory, the sense amplifiers have become separate class of circuits. The primary function of a SA in SRAMs is to amplify a small analog differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. Since SRAMs do not require data refresh circuitry after sensing, the sensing operation must be nondestructive. Architectures using column multiplexing can share a single SA among the multiplexed columns such that only one column is connected to the sense amplifier at any given time. [6]

The sensing starts with biasing the latch-type SA in the high-gain meta stable region by pre charging and equalizing its inputs. Since in the latch-type SA the inputs are not isolated from the outputs, isolation transistors are needed to isolate the latch-type SA from the bit lines and prevent the full discharge of the bit line carrying a “0”, which costs extra power and delay. Due to the presence of the column MUX/isolation transistors, two precharge/equalize circuits are needed to ensure reliable sensing.

In order to make the existing sense amplifier to perform the diagnosis task, i.e. to sense the voltage levels on bit lines, we must add circuitry as shown in gray in Figure 5. First, two voltage sources (VREFL and VREFH) are added on one input of the sense amplifier. Note that these voltage sources must be isolated from the sense amplifier during the normal functioning mode by using pass gates. Selection of one of them depends on which level (high or low) we have to diagnose[10][11].

10. REDUCING POWER IN SENSE AMPLIFIER

The function of the sense amplifier is to amplify small differential bit line voltages into logic levels. This operation should be performed as fast as possible. While numerous sense amplifiers exist, some of the common forms employed for SRAMs are either simple differential amplifiers or charge amplifiers that are similar to bit cells. A natural trade-off occurs between speed and power for such sense amplifiers. Larger currents improve sense amplifier speed. The analog nature of sense amplifiers often results in consuming appreciable fraction of the total power. Sense amplifiers are enabled by a sense amplifier enable signal.

Schemes employed for reducing the power requirements of sense amplifiers can be differentiated based upon the point at which they are activated. The first form limits sense amplifier currents by precisely timing the activation of the sense amplifier for just the period required. The second scheme employs sense amplifiers which automatically cut off after the sense operation.The self-timed ram core can be extended for obtaining the sense amplifier enable signal. The enable sense amplifier signal is used to set up an SR flip-flop in the set state. Once the dummy sense amplifier has finished sensing, it resets the SR flip-flop, which in turn disables the enable for the sense amplifiers. We rely on every sense amplifier having completed the sense action before the dummy sense amplifier.

An alternative method shapes the tail current of differential amplifiers by activating pull-down transistors of different transistors in sequence. Self-latching sense amplifiers accomplish a automatic limiting of currents after sense. The structure of a latched sense amplifier is shown in figure. The structure can be visualized as a cross-coupled amplifying inverter loop, with additional transistors to transfer bit line voltages to the inerter loop shown in Fig. 10.Various power can be calculated using the designed sense amplifier in fig.11.[10][11]

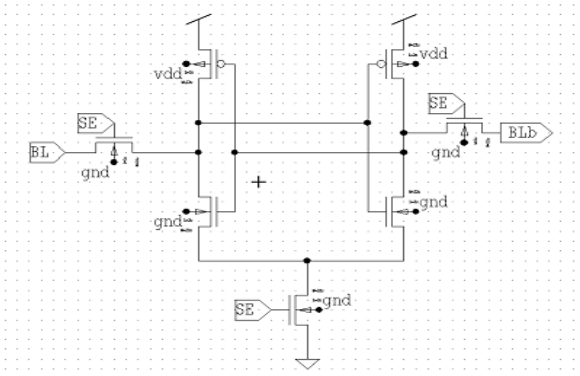

Fig. 10.Designed sense amplifier for 10T SRAM cell

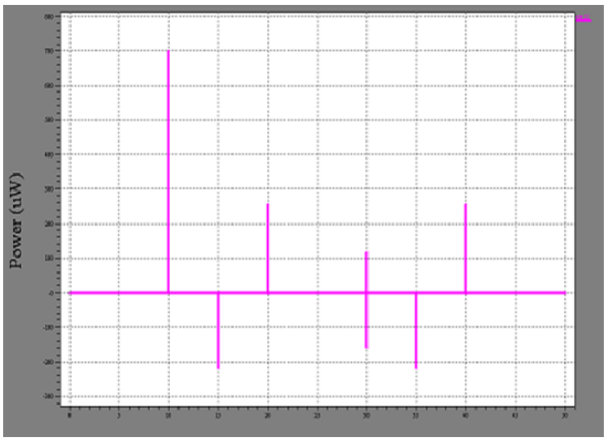

Fig.11. Power output of sense amplifier circuit in 10T SRAM cell

Table 1. Comparison between 8T and 10T SRAM cell

S.No.	Parameters	8T SRAM Cell	10T SRAM Cell
1	No of Transistor's	8	10
2	Supply Voltage	1.8V	1.8V
3	Operating frequency	5Hz	5Hz
4	Surface area	10707.0μm^2	13992.0 μm^2
5	Power Consumption	0.949mW	0.5675mW

11. CONCLUTION

The SRAM memory cell is designed for both 8T and 10T with 0.18 micron technology. The supply voltage and frequency are also same for the two circuits. But the area and total power consumption will be in diverse if the length is varied in micron technology. Further the change of temperature above and below the room temperature, the drain source voltage and drain source current of nMOS transistors in the layout are also varied. Below the room temperature there is a slight variation in voltage, power and current. But in case of above room temperature, a sudden increase in current, will affect the total operation of the circuit. So we put CMOS instead of nMOS and other transistors. Thus the area and power of any complicated circuit is reduced for all the temperature changes. The hotspot are also indentified in 0.18 micron technology in 8T SRAM cell and 10T SRAM cell. Because the no of interconnects reduces in 10T SRAM cell design. To avoid this we have to increase the number of energy storing elements in the layout design. From the above analysis it is found that 10T SRAM cell design is best for temperature variations for low power applications.

12. ACKNOWLEDGMENTS

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