Development and Verification of Iterative Decoder for LDPC-RS Product Codes

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ABSTRACT

LDPC codes provide good random error performance nearer to Shannon limit. The LDPC codes have some residue errors which cannot be corrected even after large number of iterations such errors can be corrected by concatenating LDPC codes with RS codes. This paper describes the development of an iterative decoder scheme for LDPC-RS product codes which made LDPC codes and Turbo codes popular. The iterative structure consists of a soft decision decoding of LDPC codes and hard decision decoding of RS codes. The concatenated scheme provides higher performance than the iterative decoder for LDPC codes. The iterative scheme is developed in MATLAB and FPGA kit is used for practical verification.

General Terms

Error correction codes with error correction capability of the decoder nearer to Shannon limit.

Keywords

LDPC-RS, SVM, EE, Log-SP, SSD, BMA, Product codes, Iterative decoder

1. INTRODUCTION

Error Correction Codes play a very important role in any communication system. The errors occur due to the non-idealities of the unreliable channel. Shannon [1] provided the theoretical limit for successful transmission and reception of data in the presence of errors introduced by the channel. Many researchers introduce their own methods to achieve the theoretical limit. But, the performance nearer to Shannon theoretical limit was achieved after the rediscovery of LDPC codes of Gallager [2] codes by Mackay and Neil [3] [4] and Turbo codes. The rediscovery was based on Gallager codes and Tanner [5] graph. The linear property of block codes and systematic encoding to form of the codeword make LDPC codes simple to construct.

The soft decision decoding algorithm provides much better performance than hard decision decoding algorithms due to the information they carry during the decoding process. Various decoding algorithms like Sum-Product, Sum-Subtract, Log-Sum-Product (Log-SP), Soft Distance and Simplified Soft Distance (SSD) [5] [6] [7] have been developed in the past. Due to the complexity of the previous algorithms Log-SP decoding algorithm became more popular. But Log-SP decoding algorithm requires the information of the channel which is not always possible. Hence, SSD algorithm is proposed which has similar performance to Log-SP decoding algorithm but it does not require the information of the channel.

The SSD decoding algorithm has almost same complexity as that of Log-SP decoding algorithm. Hence Log-SP decoding algorithm can be replaced by SSD decoding algorithm. The systematic encoding allows to simply dropping the check bits added during encoding process. The syndrome provides the information whether the original codeword is recovered or not. If syndrome is zero, codeword is recovered.

The LDPC codes are encoded by multiplying the message with Generator Matrix (G) to obtain a codeword. A Parity Check Matrix (H) is generated such that G multiplied with transpose of H is equal to 0. But to generate a sparse H matrix for LDPC codes the H matrix is generated such that it has very less number of 1s as described by Mackay [3] and the Generator Matrix (G) is generated by using Gaussian elimination method.

The sparse nature of the matrix reduces the complexity of the overall algorithm with a considerable reduction in the minimum distance of the code which describes the error correction capability of the code.

The trapping set in the LDPC code is a major problem because it is not possible to recover many bits which cause a single bit of syndrome to be error. This condition is mainly obtained when the consecutive bits in the codeword are erroneous. But encoding LDPC codeword with RS is not suitable. Hence to distribute the errors in the codeword a simple row-column interleaver is used so that obtained codeword forms a 2 dimensional structure called LDPC-RS product codes.

This paper is organized as follows; Section II gives an introduction to LDPC-RS product codes. Section III describes the proposed method. Section IV gives the complexity analysis of the different methods. Section V concludes the whole paper with a note on future work.

2. LDPC-RS PRODUCT CODES

These codes are the extension of LDPC codes to reduce the Bit Error Rate (BER) for the given SNR. The Product codes are formed by serial concatenation of two short codes either of binary form or non-binary form. The trapping set or error floor in LDPC codes does not allow correcting the codeword. This error floor can be easily corrected by RS codes which provide good burst error correction capability. The overall LDPC-RS structure is best suited for almost all the conditions.

The two dimensional structure of LDPC-RS product codes is formed as follows; A RS encoder of Galois field 2^m encodes different set of 'p' symbol inputs for 'r' number of times and

arranges it row-wise to form k-bit codeword. Then the LDPC encoder encodes the RS codeword column-wise such that the message for LDPC contains 'r' bits and the codeword contains 'n' bits. The LDPC encoder repeats it for k*m times to form a two dimensional structure of 'n' rows and 'k*m' columns. The diagrammatic representation of 2-dimensional structure is as shown in figure 1.

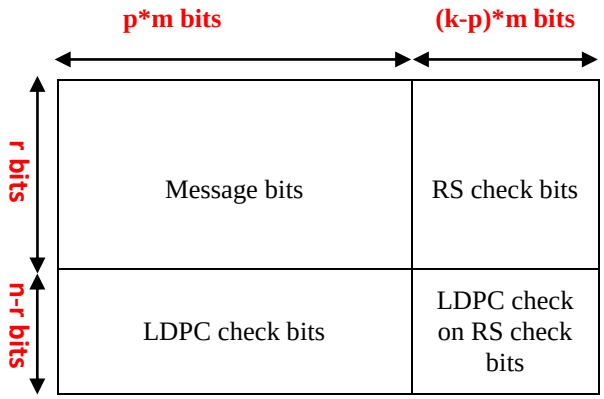

Figure 1: LDPC-RS Product Codes Structure

The LDPC-RS product codes have the following properties. The overall code rate is the product of individual code rates. The minimum distance is the product of minimum distances of individual codes.

The soft decision decoding of LDPC-RS product codes provide random-error correction capability nearer to Shannon limit. To improve the performance of LDPC-RS serial concatenated codes soft decision RS codes can be used. The soft decision decoding complicates the design with a small improvement in performance. Hence hard decision RS codes will be used.

3. ITERATIVE STRUCTURE FOR LDPC-RS PRODUCT CODES

The improvement in the design of LDPC-RS product codes and its iterative structure was proposed by Vo Tam Van et.al [8]. The Error Detection algorithm (EDA) is used to detect and erase hard errors. If multiple errors occur then Product Decoding algorithm (PDA) is used which corrects errors by using SPA decoding for LDPC codes. This design works well for magnetic recording channels.

Yaqi Li et.al [9] proposed a different iterative structure by employing two techniques called Error Estimation (EE) and Soft Value Modification (SVM). The EE technique reduces the number of iterations and SVM technique allows iteration of LDPC-RS combination.

The first method requires erasure information and uses a complex Sum-Product algorithm. For the second method same SPA soft decision decoding algorithm is used. [10] It is not always possible to predict the channel information for the received data.

3.1. LDPC-RS Product codes decoder

The simplified soft distance (SSD) based on SPA algorithm is less complex and does not require channel variance for successful decoding of the received data. The SSD decoding algorithm for LDPC codes along with a Reed Solomon codes form Product codes.

The reduction in Bit Error Rate (BER) with the increase in SNR for LDPC-RS product codes over LDPC codes is as shown in figure 2.

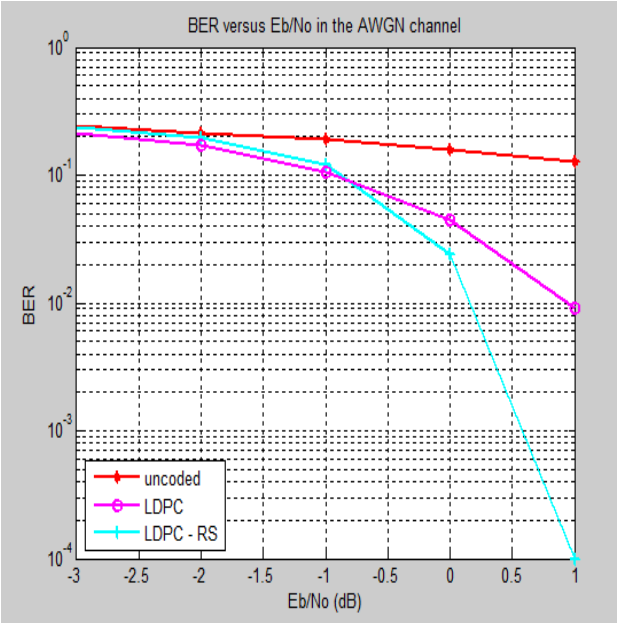

Figure 2: BER vs. E_b/N_0 of LDPC-RS Product codes over LDPC codes.

The (96, 32) LDPC decoder is compared with the (5760, 1152) LDPC-RS decoder constructed from (96, 32) LDPC codes along with (15, 9) RS codes under GF (2^4). [11] [12]

The LDPC-RS [13] codes provide the advantage of increase in number of message bits that are transmitted once. There is an improvement in performance over LDPC codes. These codes are simple to construct. The overall code rate of the constructed codes is 1/5, which is reduced compared to LDPC codes used for construction of LDPC-RS product codes.

3.2. LDPC-RS Product codes decoder with Error Estimation (EE) Technique

The Error Estimation (EE) technique is described as follows:

- The syndrome of all the LDPC decoders is stored.
- Depending on the ones in the parity check matrix the number of errors are computed.
- If the errors are estimated to be corrected by RS decoder then RS decoding is done, otherwise another iteration of LDPC decoding is done.
- The whole process is repeated until the errors estimated can be corrected by RS decoder or the maximum limit for the LDPC decoder is reached.

The EE technique basically group the number of bits into the RS designed Galois field and it then checks whether the number of groups that can be corrected is within RS correction capability. This grouping process converts the bit-error pattern to a symbol error pattern for RS codes.

The EE technique introduced in between LDPC codes and RS codes allows stopping LDPC decoding and starting RS decoding to get the result. This design allows reducing the number of iterations of LDPC decoder. This reduction allows faster decoding of LDPC-RS product codes with same performance. The performance of LDPC-EE-RS with LDPC-RS is as shown in the Figure 3.

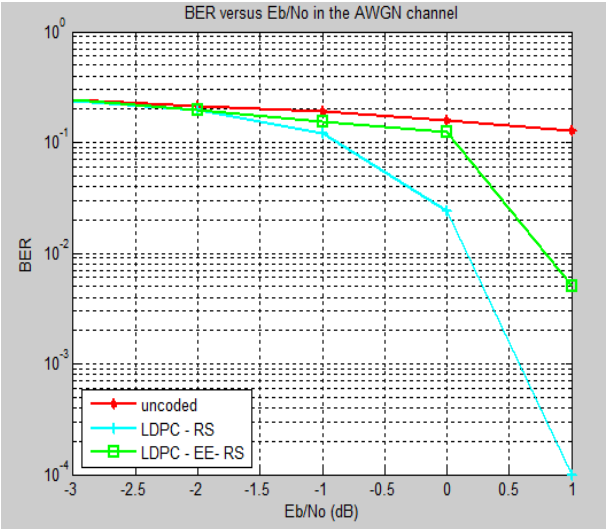

Figure 3: BER vs. E_b/N_0 of LDPC-RS product codes with and without EE technique.

The (5760, 1152) LDPC-RS code and the same LDPC-RS code with EE technique is introduced. But most of the times the EE technique fails to recover the message.

The degradation of the performance is very high due to inaccurate estimation of errors. Hence to overcome this disadvantage a new technique named Soft Value Modification (SVM) is used.

The SVM technique improves the performance of LDPC-EE-RS code by forming the iterative structure for decoding of LDPC-RS product codes.

3.3. LDPC-RS Product codes decoder with EE and SVM Technique

The Soft Value Modification technique is described as follows:

- The successful decoding of the RS decoder is used to improve the information of LDPC decoder by improving the probabilistic values of the codeword.
- The improvement is done by fixing the values very high.
- If RS decoding is unsuccessful the values are retained from the LDPC decoder.
- The passing of information allows forming iterative structure.
- The whole process is carried until the codeword is decoded correctly or the maximum number of iterations is reached.

The degraded performance of the LDPC-EE-RS decoder can be improved by forming an iterative structure using the SVM technique. The SVM technique forming an iterative structure for LDPC-EE-RS codes improve the performance over LDPC-EE-RS codes as shown in Figure 4.

This decoder needs to store and modify the probability values which increase the complexity of the design. The improvement in performance is better than LDPC-EE-RS decoder but not good as LDPC-RS decoder. The degradation of the performance after using EE technique is due to the inaccurate estimation of the errors that are passed to the RS decoder.

The SVM technique improves the performance of the decoder. So to further improve the performance SVM technique is used to form the iterative decoder for LDPC-RS product codes.

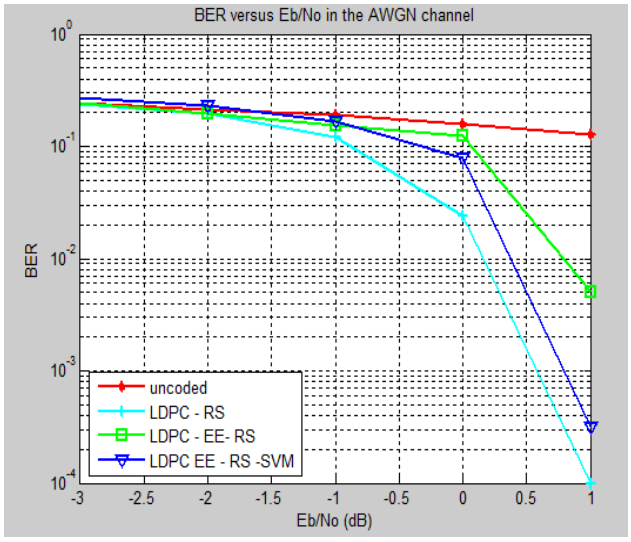

Figure 4: BER vs. E_b/N_0 of LDPC-EE-RS decoder with and without SVM technique and LDPC-RS product codes.

3.4. LDPC-RS Product codes decoder with Soft SVM Technique

The LDPC decoding is fixed to less number of iterations and it is switched to RS decoder and back to LDPC decoder again and again also for a fixed number of times. If decoding is successful the decoding can be stopped either at LDPC decoder or at the RS decoder.

The successful decoding is known by the syndrome of all the LDPC decoded columns to be zero or by the syndrome of all RS decoded rows to be zero. Hence it reduces the decoding time. The improvement in performance of the LDPC-RS-SVM iterative decoder structure for the LDPC-RS product codes is as shown in Figure 5.

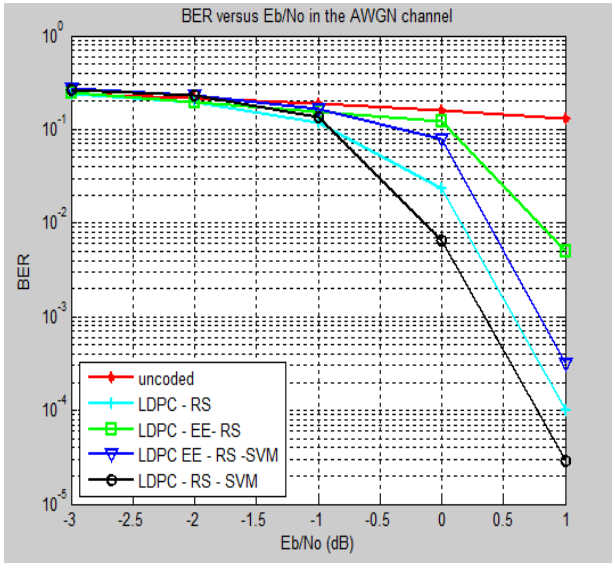

Figure 5: BER vs. E_b/N_0 of LDPC-RS-SVM iterative decoder compared to other decoders.

The LDPC-RS-SVM iterative decoder is better than the other decoding algorithms. So, this design is verified for other LDPC-RS product codes of length (600, 180) and (16380, 6876). The probability of errors depends on the strength of the signal, the improvement in BER at low SNR decrease the strength of the signal required to correct errors.

4. FPGA IMPLEMENTATION

The LDPC-RS encoder and decoder are designed and modeled in Verilog. Using Xilinx ISE Design Suite 14.7 the encoder and decoder designs are targeted for Artix-7 Nexys 4 FPGA board. Functional verification is performed using Mentor Graphics Modelsim PE Student Edition 10.4. The fixed point arithmetic is used to perform calculations in the Verilog code. Two 256 entries look-up-tables and memory for storing the real values received at the receiver are used. Longer length fixed point values provide more information during decoding process. Hence, there is a tradeoff between complexity of the design and performance. Simulation results for encoder, decoder and iterative decoder are as shown in figure 6, 7 and 8 respectively.

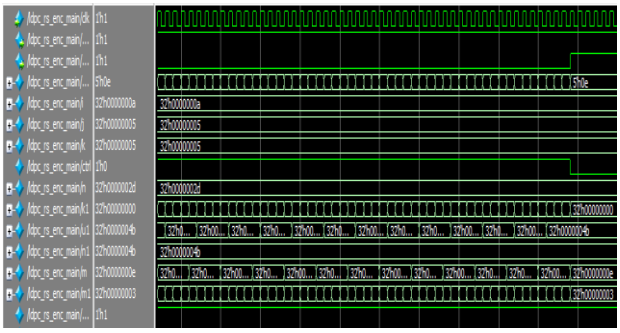

Figure 6: Simulation results for LDPC-RS encoder

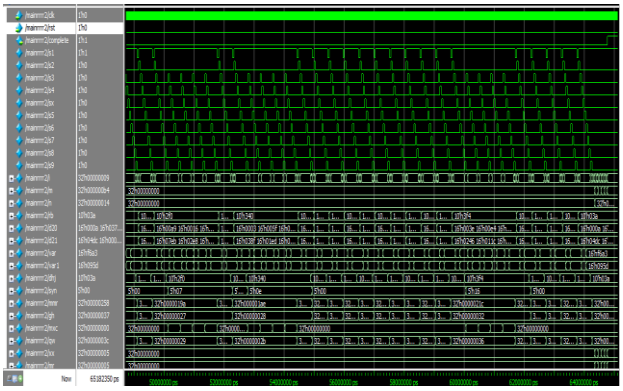

Figure 7: Simulation results for LDPC-RS decoder

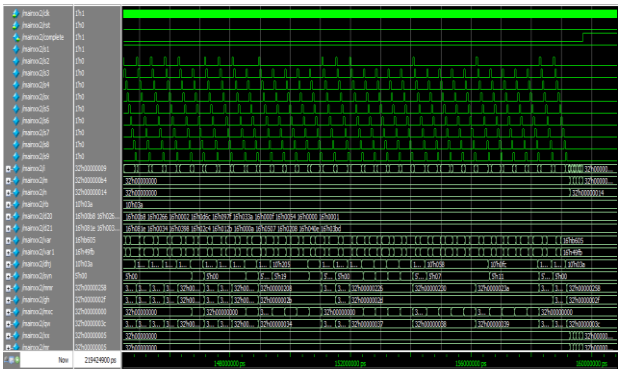

Figure 8: Simulation results for iterative LDPC-RS decoder

The iterative structure is more complex than the LDPC-RS product codes due to more information storage for passing information from RS decoder to LDPC decoder. The designed iterative decoder is targeted on Kintex 7 KC705 Evaluation Platform due to the requirement of more resources to store the probability values.

5. CONCLUSION

In this paper different decoder designs for LDPC-RS product codes are presented. After a thorough analysis of the different designs it is observed that the BER performance of the LDPC-RS-SVM iterative decoding scheme is much better compared to other designs. This decoder is verified for LDPC codes of different code rates of 0.7, 0.5 and 0.33 using MATLAB R2014a. All these LDPC-RS product codes show improvement in performance over other decoder designs. Since, longer length LDPC codes perform better than short codes. To construct long length LDPC-RS product codes can be targeted on Virtex 7 FPGA for implementation.

The future work includes improving the EE technique so that the errors are estimated accurately, which reduces the decoding time. The Rate-Compatible LDPC codes in the LDPC-RS product codes with less complexity is required to be implemented so that these codes can be used at different environments. The study of concatenation of different codes and formation of a multi-dimensional structure allows improving the performance at less complexity and reduction in decoding time.

6. REFERENCES

[1] C. E. Shannon, “A mathematical theory of communication,” Bell Syst. Tech. J., vol. 27, pp. 379–423, 623–656, 1948.

[2] R. G. Gallager, “Low density parity check codes,” IRE Trans. Inform. Theory, vol. IT-8, pp. 21–28, Jan. 1962.

[3] D. J. C. MacKay and R. M. Neal, “Near Shannon limit performance of low density parity check codes,” Electron. Lett., vol. 32, no. 18, pp. 1645–1646, Aug. 1996. Reprinted Electron. Lett., vol. 33, no. 6, pp. 457–458, Mar. 1997.

[4] David J. C. MacKay, “Good Error-Correcting Codes Based on Very Sparse Matrices,” IEEE Trans. Inform. Theory, vol. 45, no. 2, Mar. 1999.

[5] R. M. Tanner, “A recursive approach to low complexity codes,” IEEE Trans. Inform. Theory, vol. IT-27, pp. 533–547, Sept. 1981.

[6] L. Arnone, C. Gayoso, C. Gonzlez and J. Castieira, "Sum-Subtract Fixed Point LDPC Decoder," Latin American Applied Research, vol 37, pp 17-20, 2007.

[7] J. Castineira Moreira, M. Rabini, C. Gonzalez, C. Gayaso, L. Arnone, “FPGA implementation of two very low complexity LDPC decoders,” Programmable Logic (SPL), IEEE Int. Symp, pp. 7-12, April 2011.

[8] P.G. Farrell, L.J. Arnone and J. Castineira Moreira, “Euclidean distance soft-input soft-output decoding algorithm for low-density parity-check codes,” IET Commun., vol. 5, Iss. 16, pp. 2364–2370, 2011.

[9] Tam Van Vo and Seiichi Mita, “ A Novel Error-Correcting System Based on Product Codes for Future Magnetic Recording Channels”, IEEE Trans. Magnetics, vol 47, no.10, Oct. 2011.

[10] Y. Li, B. Liu, B. Rong, Y. Wu, G. Gagnon, L. Gui, et al., “On the performance of LDPC-RS product codes for mobile DTV,” IEEE Int. Symp. BMSB, pp. 1–5, 2012.

[11] S. Lin and D. J. Costello, Jr. , “Error Control Coding: Fundamentals and Applications,” 2nd edn., Upper Saddle River, NJ, Prentice-Hall,2004.

[12] Moon T. K.: “Error correction coding- mathematical methods and algorithms”, Wiley (2005).

[13] W. E. Ryan and S. Lin, *Channel Codes: Classical and Modern*. Cambridge, U.K.: Cambridge Univ. Press, 2009.