# Area Efficient Design Analysis of Carry Look Ahead Adder

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## ABSTRACT
This paper provides a low power solution for Very Large Scale Integration. Power consumption of a circuit and its area occupied are major constraints for a VLSI designer. So in this paper we focused mainly on these two parameters by using different design methodologies such as Fully Automatic, Semi-custom and Fully Custom. Addition is basic operation in any system, but it requires more time as the number of bits are increased. So we use carry look ahead adder to reduce the processing time in circuits like processors or any other circuit. Design of CLA adder using semi-custom and fully custom approach can reduce the area and power consumption to a great extent.

## Keywords
Carry Look Ahead Adder, VLSI, Automatic approach, fully custom approach.

## 1. INTRODUCTION
Fast addition is the arithmetic function for digital systems. It heavily impact the performance of digital systems [1]. Addition is also used to compute virtual physical address in fetching operation in all computers [2]. Many fast adders are available in market but the high speed with low power and less area is still challenging [3]. High performance circuits are continued to be a topic of interest. Addition circuits are fall under this group. The adders are need to be very fast because they are logic circuits designed to perform high speed arithmetic operations and are important block in digital systems because of their extensive use in all basic operations as subtraction, multiplication and division[4]. VLSI technology is a technology by which we can design complex system on chip where all elements of system like analog and digital circuit, passive element are integrated on single chip [5]. Therefore for a VLSI designer it is a major challenge to reduce the area of chip by using efficient optimization technique [5, 6]. Carry look ahead adder is proposed as an alternative for speed enhancements. Speed of Carry look ahead adder is usually determined by critical carry path delay and the carry critical path is data dependent and changes during the addition operation [7]. Carry look ahead adder is very basic building block for any digital circuit.

In VLSI, there are three domains structural domain, behavioral domain and physical domain. The structural domain deals with the schematic of transistors, gates, block diagram of circuit using flip-flops. In structural domain, the VLSI designer can design its circuit using transistors or gates. The paper is organized is as follows. The section I describes the overview of carry look ahead adder in which basic gate level diagram is described, section II describes the schematic of carry look ahead adder using transistors, section III describes the layout of carry look ahead adder which is obtained by VLSI tool. Simulation results are explained in section IV. Section V gives the conclusion of this paper [8].

There are three domains, structural domain, behavioral domain and physical domain. The structural domain deals with the schematic of transistors, gates, block diagram of circuits using flip-flops. In structural domain, the VLSI designer can design its circuit using transistors or gates by using wires. The behavioral domain deals with the front end technique in VHDL. The VLSI designer enters his design in form of equations. This domain cones under the front end design tool. Where designer does not know about what is going on at back end. The physical domain deals with the exact dimensions of the transistors. In this domain designer designs the transistors using rectangular strips of various layers. The physical domain is back end process.

## 2. OVERVIEW OF CLA ADDER
In ripple carry adder, the carry propagation time is the speed limiting factor. So if numbers of bits are increased then the delay in ripple carry adder is accordingly increased. So reducing the carry propagation is of great importance. Different design approaches have been employed to overcome the carry propagation. One widely used approach use principle of carry look ahead, which calculates the carry signal in advance. This type of adder is called carry look ahead adder [9]. Let A and B be the two four bit binary numbers and S and Cout being their sum and carry out respectively.

A= 0101

B= 0110

Sum= 1011 and carry out=0

$$P_i = A_i \oplus B_i \qquad (1)$$

$$G_i = A_i \cdot B_i \qquad (2)$$

$$S = P_i \oplus C_i \qquad (3)$$

$$C_{i+1} = (A_i \oplus B_i) \cdot C_i + A_i \cdot B_i \qquad (4)$$

Equation (1) shows the sum of two numbers A and B, eq (2) shows the product term of A and B, eq (3) shows the final sum of the two binary bits and previous carry if any, eq (4) shows the final carry out signal which gives the result whether the final carry is generated or not. $P_i$ is known as carry propagate when $P_i$ is 1 the input carry is propagate to output carry. $G_i$ is known as carry generate signal because carry is generated when $G_i$=1.

$$S_0 = A_0 \oplus B_0 \oplus C_0 \quad (3.a)$$

$$S_1 = A_1 \oplus B_1 \oplus C_1 \quad (3.b)$$

$$S_2 = A_2 \oplus B_2 \oplus C_2 \quad (3.c)$$

$$S_3 = A_3 \oplus B_3 \oplus C_3 \quad (3.d)$$

The above equations are used to calculate the sum of two 4 bit binary numbers. The XORing of two numbers A and B is done and the resultant is again XORed with initial carry to generate the Sum.

$$C_1 = (A_0 \oplus B_0)C_0 + A_0 \cdot B_0 \quad (4.a)$$

$$C_2 = (A_1 \oplus B_1)C_1 + A_1 \cdot B_1 \quad (4.b)$$

$$C_3 = (A_2 \oplus B_2)C_2 + A_2 \cdot B_2 \quad (4.c)$$

$$C_4 = (A_3 \oplus B_3)C_3 + A_3 \cdot B_3 \quad (4.d)$$

The above equations show how the carry is calculated from previous carry and inputs bits. The four bit carry look ahead adder consists of 3 level of logic. First level generates all P and G logic. The output signals from this level will be available after one propagation delay. In second level, the carry look ahead block will consists of four two level implementation logic. It generates carry signals and result will be available after three propagation delays. The third level includes the XOR gates which generate sum signals. The output of this signal will be available after four propagation delay [10].

## 3. SCHEMATIC OF CLA ADDER

The schematic of carry look ahead adder is designed in DSCH. The schematic is designed using transistors or by logic gates. The first of all modules of gates are designed using transistors and then they are combined to form one complete module of one bit adder. In this design we have used three gates namely Exclusive OR(XOR) gate, OR gate and AND gate.

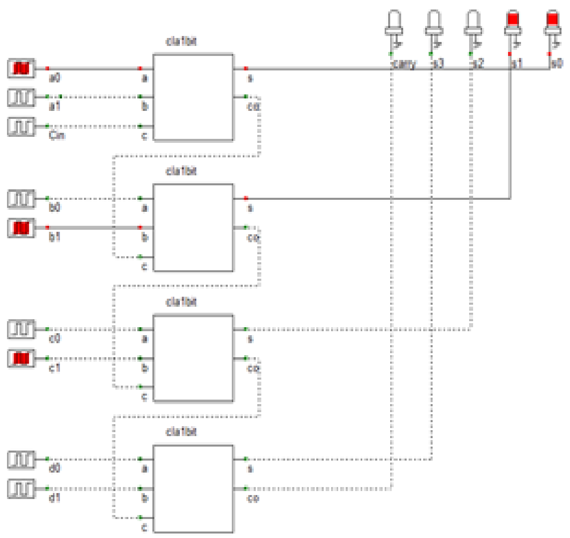


**Fig 1: Block diagram of CLA addder**

Fig 1 shows the block diagram of carry look ahead adder using modules created in DSCH tool. These modules contain the complete diagram for one bit addition. For four bit addition we connected four similar modules and made connections accordingly.

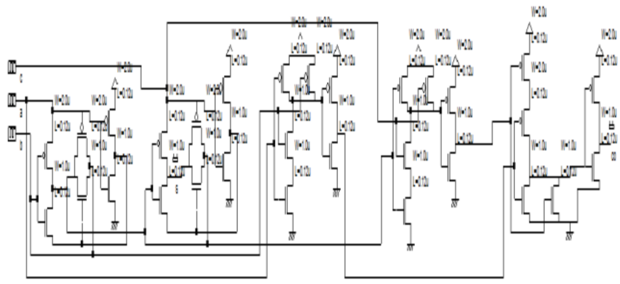

**Fig 2: Transistor level schematic of one module**

Fig 2 shows the internal schematic diagram of one module. The schematic consists of transistors.

## 4. LAYOUT OF CLA ADDER

In this paper we have used three approaches to design the carry look ahead adder and compared their results. The first approach is fully automatic. In fully automatic approach we first created the schematic in DSCH. DSCH is the Digital Schematic tool which is used to create a circuit diagram at gate or transistor level. After creating a design in DSCH tool, we have created a Verilog file and that Verilog file was compiled in micro-wind tool to auto-generate the layout. After this step auto-generated layout appeared on screen.

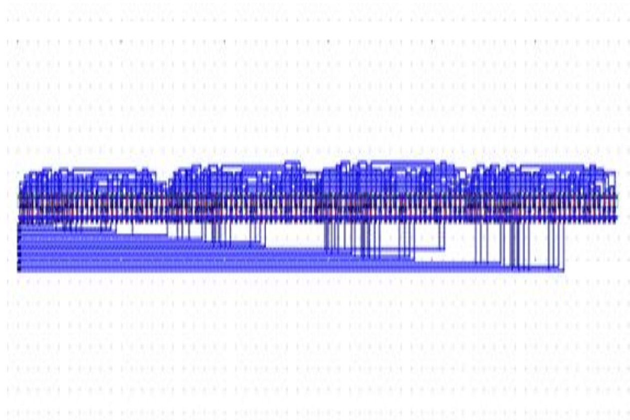

**Fig 3: Layout of Fully Automatic design**

Next step is semi-custom design. In this step we used only one VLSI tool i.e. micro-wind to create the layout directly without going to its schematic side. The layout was manually generated by us and its errors can be checked by DRC (Design Rule check).

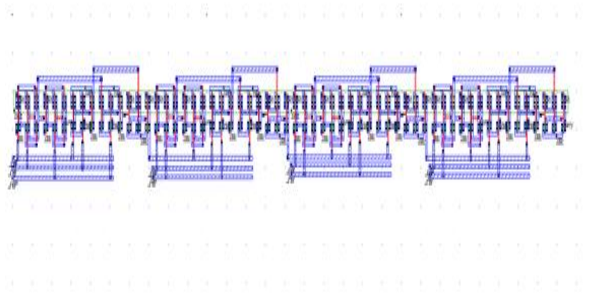

**Fig 4: Layout of Semi-custom design**

Fig 4 shows the layout of semi-custom approach which is obtained by creating the layout using transistors already available in the library. Connections are made using metal layers in layout.

There is one more approach called fully custom approach. In this we have started our design from scrap i.e. by first creating NMOS and PMOS transistors and then using these manually generated transistors to design gates and modules. When designing all the layout we have simulated the design and timing diagram is available with us. Fig 5 shows the Full custom design.

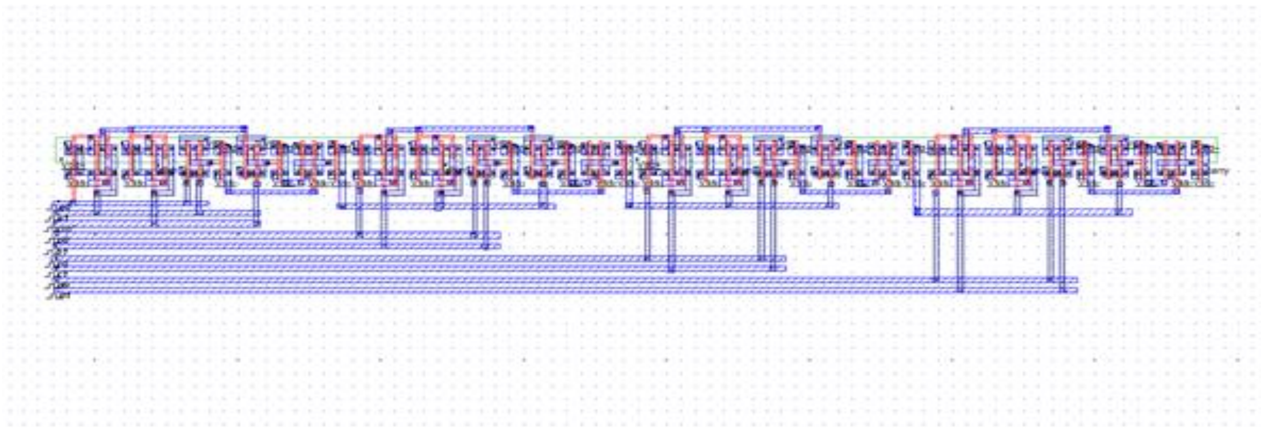

**Fig 5: Layout of Full-custom design**

## 5. SIMULATION RESULTS

Fig 6 shows the timing diagram of carry look ahead adder. This is the simulation result of schematic as shown in fig1. All the three designs have been simulated and result is as shown.

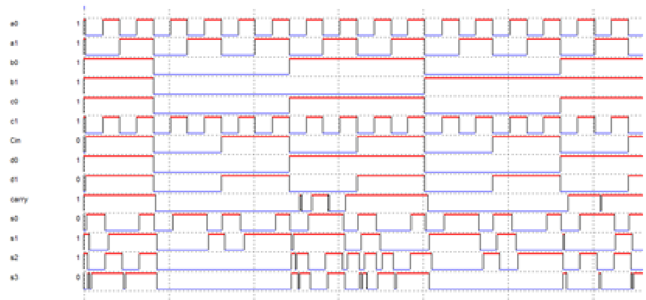

**Fig 6: Timing Diagram of schematic of CLA adder**

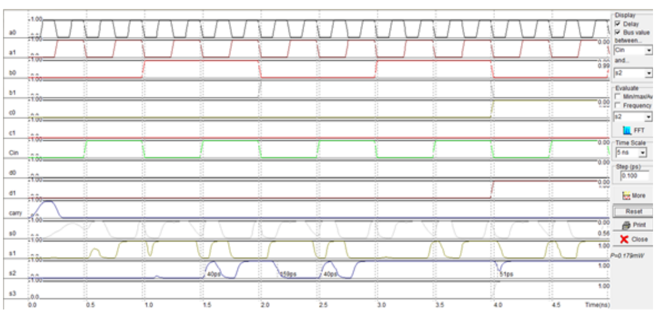

**Fig 7: Simulation result of Fully Automatic design**

Fig 7 shows the simulation results of fully automatic approach, and it has been shown that the power consumption is 179µw.

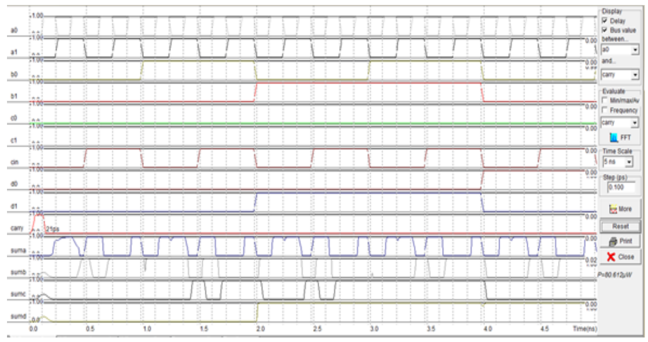

**Fig 8: Simulation result of Semi-custom design**

Fig 8 shows the simulation results of semicustom approach and the power consumption is 80.61µw.

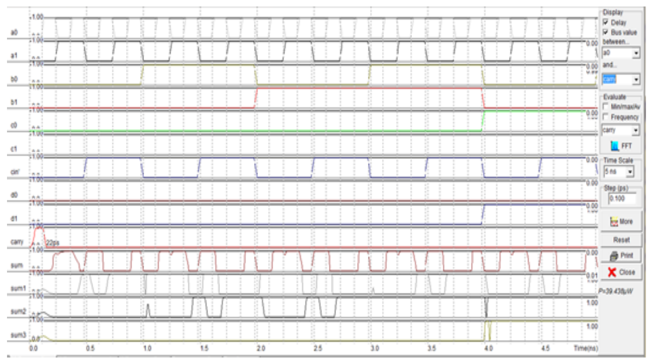

**Fig 9: Simulation result of fully custom design**

Fig 9 shows us the simulation results of fully custom design approach and power consumption of this design is 39.43µw, which is least among the three. All the above simulation results are satisfying with the truth table of carry look ahead adder.

**Table 1: Comparison of design approaches**

| Para-meters | Area ($\mu m^2$) | Electrical nodes | Power consumption ($\mu w$) | Current ($mA$) |
|---|---|---|---|---|
| Fully automatic | 1825.7 | 64 | 179 | 2.547 |
| Semi-custom | 529.8 | 115 | 80.61 | 1.71 |
| Fully custom | 269.3 | 127 | 39.43 | 0.887 |

Table 1 shows the comparison of three design approaches with area and power. It can be seen that the power consumption is least in fully custom approach and same as the area.

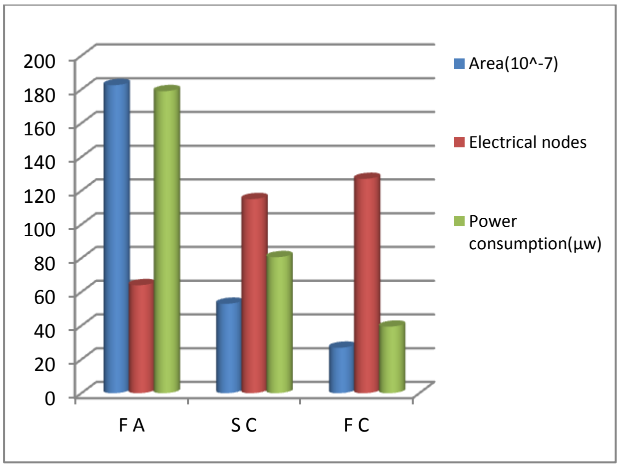


**Fig 10: Comparison of various techniques**

Fig 10 shows the graphical view of the comparison of all three approaches described above. FA stands for Full Automatic design, SC stands for semi-custom design and FC stands for fully custom design. It can be seen that power consumption and the area is greater in fully automatic approach, but as we decrease the area and power consumption the electrical nodes are automatically increased.

## 6. CONCLUSION

In this paper we have given a comparison of three design methods and concluded that the fully custom approach is best among the three where we can reduce the chip area and the power consumption as well. The semi-custom approach is moderate in which the area and power consumption is less than fully automatic but more than fully custom. In semi-custom design the area has been reduced up to 71% if we compare with fully automatic design and in fully custom the area has been reduced up to 85.2% as compare to fully automatic and 49% as compare to semi-custom design. As compare to fully automatic design the power consumption has been reduced up to 55% in case of semi-custom design and 77% in case of fully custom design.

## 7. REFERENCES

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