A Simulation Algorithm for Prediction of Random Variations in Digital Circuits

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ABSTRACT
A novel simulation algorithm capable of capturing statistical variability manifests in digital design is proposed. The only estimations for the algorithm inputs are the standard deviations of channel length and the gate voltage. Implementing the algorithm for the simulation of propagation delay times of the basic digital building blocks such as inverter, NAND2 and NOR2 circuits gives errors less than 7% against the most accurate results obtained from 'atomistic' HSPICE simulations.

Keywords
Statistical variability, Digital design, Monte-Carlo simulation, statistical modeling, nano-CMOS

1. INTRODUCTION
Aggressive scaling of device dimensions into ultra short channel regime leads to significant process and intrinsic parameter fluctuations [1-3]. These fluctuations have caused reliability issues which in turn results in a waste of both time and cost. It is therefore important that a circuit designer can incorporate these effects in early simulation stage. A variability-aware design approach needs a right prediction of random variations [4-7]. The investigation and analyze of these variations using accurate 'atomistic' simulations needs both long times and powerful computational resources [1]. On the other hand, the outcomes of 'atomistic' simulations are not widely accessible for the designers.

An extensive study has been carried out in the literature to incorporate the impact of random variations into analytical expressions in digital circuit design and thus, simplifying the complexity of 'atomistic' simulations. However, those expressions suffering from common issues: (i)-they are all circuit specific, (ii)-their accuracy depends to input slew rate and load capacitance[8-11]

This paper organizes as follows. Section 2 reviews some analytical expressions capable of dealing with variations in inverters as the most important digital building blocks. Section 3 proposes an algorithm to account for the random variations inthe gate propagation delay time using appropriate Gaussian sources in series with the device and embedding length variations in HSPICE circuit netlist. Section 4 implements the algorithm and extends its usage on NAND2 and NOR2 gates. Accurate Monte-Carlo statistical simulations have been carried out to compare the accuracy of the proposed algorithm against 'atomistic' results.

2. ANALYTICAL MODELING OF PROPAGATION DELAY TIME
Due to CMOS short channel effects arising from the device scaling into deca-nanometer dimensions, prediction of device current (Ids) using standard Shockley model results in significant errors.The Alpha power law model introduced by Sakurai and Newton is among the first ones incorporating carrier velocity saturation effects [8]. However, this model ignores the saturation current variations and thus, results in large deviations in Ids and the inverter propagation delay time (Tpd). Some other useful models have been introduced in the literatures which have their advantages and drawbacks [9,10]. For instance, some modifications in Alpha-power law have been proposed resulted in reduced errors in Ids but they ignore gate-drain capacitance or over-shoot and short circuit current [11].

Since any deviation in Ids causes significant error in the Tpd, the Alpha-power law will not be used for sub-50nm technologies. This is due to the fact that the channel length modulation effect is not considered effectively in this model. The selected model should take the device channel modulation effect into account. The current in this model is given by [12]:

$$I_D = \begin{cases} 0, & (V_{GS} \le V_{th} : cutoff) \\ \beta_l (V_{in} - V_{th})^{\alpha} V_{DS}, & (V_{DS} < V_{DSAT} : linear) \\ \beta_s (V_{in} - V_{th})^{\alpha} \left[1 + \lambda (V_{DS} - V_{DD})\right], & (V_{DS} \ge V_{DSAT} : saturation) \end{cases} \quad (1)$$

Where:

$$\beta_l = \frac{\beta_s \left[1 + \lambda (V_{DSAT} - V_{DD})\right]}{V_{DSAT}}$$

$$\beta_s = \frac{I_{D0}}{\left(1-\frac{V_{th}}{V_{DD}}\right)^{\alpha}}$$

Where$V_{DSAT}$is the drain saturation voltage atV_{GS}=$V_{DD}$and α is the velocity saturation index. Solving differential equations at the output node of an inverter gives the Tpd. Depending on the input slew-rate and the load capacitance, the propagation delay time can fall in two following category[11,12]:

a) For slow input or small load capacitance:

$$T_{phl} = \frac{t_r}{V_{DD}}\left[\sqrt{K_{\log}} + V_{th}\right] - \frac{t_r}{2} \qquad (2)$$

Where:

$$K_{\log} = \frac{1}{K_y}\ln\left[\frac{0.5V_{DD} - \frac{1}{\lambda}}{V_{DD} - \frac{1}{\lambda}}\right]$$

$$K_y = \frac{\beta_s t_r \lambda}{C_L(\alpha+1)V_{DD}}$$

b) For fast input or large load capacitance:

$$T_{phl} = \frac{1}{K_z}\ln\left[(0.5V_{DD} - K_2)\Big/\left(V_{DD} - \frac{1}{\lambda}\right)\right] - \frac{t_r}{2} \qquad (3)$$

Where:

$$K_z = \frac{\beta_s \lambda (V_{DD} - V_{th})^{\alpha}}{C_L}$$

3. PROPOSED ALGORITHM FOR SIMULATION OF RANDOM VARIATIONS

In the proposed approach, it is possible to predict the statistical behavior of one or more parameters. It means that by adding a few Gaussian voltage or current sources, the statistical behavior of important parameters can be replicated. Since two important sources of statistical variations arise from Random Dopant Fluctuations (RDF) and Line Edge Roughness (LER) [13,14], it will be physically meaningful to add one Gaussian source in series with the MOSFET gate to produce appropriate VTH variations roughly close to the amount which is produced by the impact of RDF and to incorporate L variations in HSPICE netlist close to the amount that is produced by LER. Fig.1 represents the block diagram for two important inputs and one output of the proposed algorithm. The statistical information of target parameters includes the mean and standard deviation of those parameters. The netlist file should be given to the input of the algorithm as well. Then, adding variations in the input file as shown in Fig.2, the target parameter variations are investigated using HSPICE Monte-Carlo simulation results. Parameter X represents the error introduced in the statistical simulations. Monte-Carlo HSPICE simulations are carried out for 1000 iterated simulations and the statistical behavior of target parameters are extracted.

Using just *σ(L)* will be generally insufficient to produce small error and it is observed that adding Gaussian voltage in series with the gate *σ(V_G)* will be essential to decrease the introduced statistical error. Based on the modeling requirement, the loop will be executed in consecutive iterations until it reach the minimum assumption of X=7% or less. The output of the algorithm will be the final values for *σ(L)*and*σ(V_G)*.

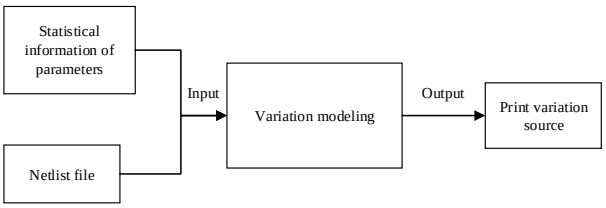

Fig.1:Block diagram of proposed variation modeling.

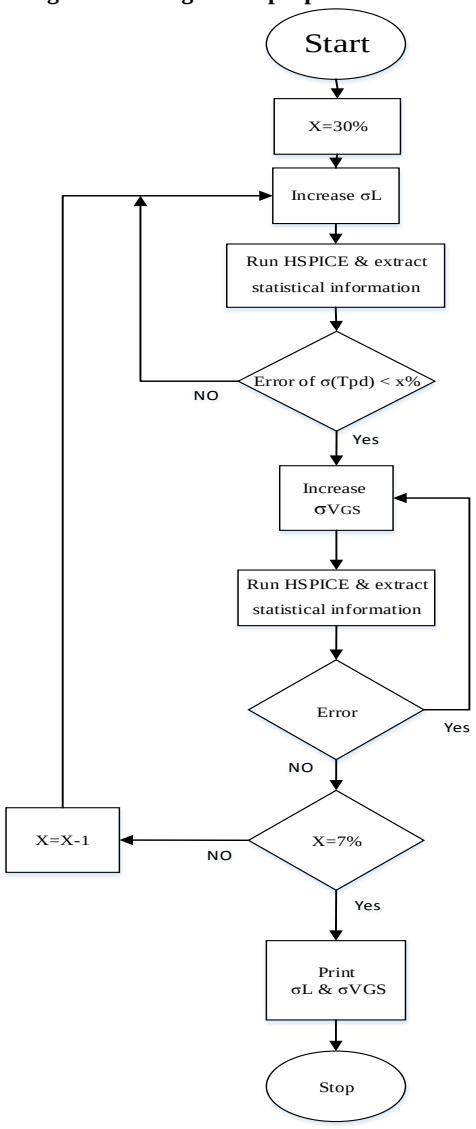

Fig.2: Proposed Algorithm of variation modeling.

4. STATISTICAL MODELING OF T_{PD} FOR BASIC DIGITAL BLOCKS

In this article, we have used atomistic simulation results as a reference of comparison to accurately evaluate the accuracy of our results. The statistical compact models arising from atomistic simulations serves as gold standard because they are

calibrated against experimental results [15,16]. Fig.3 shows schematic circuit of a CMOS inverter as the most important basic digital building block. The proposed algorithm has been implemented on the inverter to replicate Tpd of the output node. The statistical input information of Tpd is derived from 'atomistic' simulations using 1000 accurate HSPICE model cards in 35nm technology nodeThe variation inputs are then calculated for the proposed algorithm as $\sigma(L)$=5.5nm and$\sigma(V_G)$=53mv. Fig.4 depicts the comparison of Tpd histogram using both 'atomistic' model cards and the proposed algorithm. Table 1 represents the relative errors introduced in the mean and standard deviations of Tpd obtained from the proposed algorithm in respect to the corresponding values from 'atomistic' simulations.Fig. 5 and Fig.6 show the NAND2 and NOR2 gates which are used to investigate the implementation of the proposed algorithm on other basic digital building blocks. It should be noticed that in these cases, 3 different transitions of input combinations to a reference of "00" state are simulated and the errors should be acceptable in all 3 transitions.

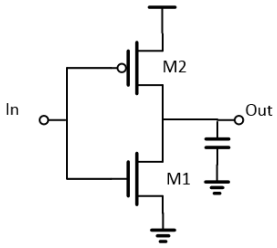

Fig.3: Schematic of Inverter gate.

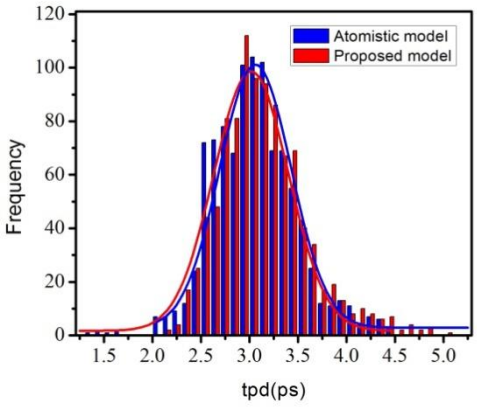

Fig.4: Histogram graph of variations of Tpd in Inverter. The red bins are for Atomistic model and blue bins are proposed model.

Table 1.Statistical variation of Tpd for basic inverter.

Atomistic	4.31E-12	4.66E-13
Proposed model	4.25E-12	4.65E-13
Error(%)	1.45	0.18

For NAND2 circuit, the standard deviations of σ(L)=4.6nm and $\sigma(V_G)$=50mvare used but we have introduced another Gaussian source of $\sigma(W)$=5nm to reduce errors to less than 7% in all of cases. The minimum error belongs to the transition from "01" to "00" state as shown in Table 2. The statistical variation of Tpd for NOR2 gate is represented in Table 3. The statistical modeling of Tpd is carried out with $\sigma(L)$=6nmand $\sigma(W)$=5nmfor this case and the maximum error is for a "11" to "00" transition. Nevertheless, the errors remain less than 7% for all transitions.

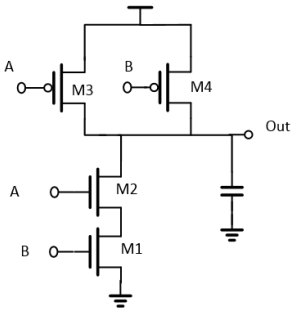

Fig.5: Schematic of NAND2 gate.

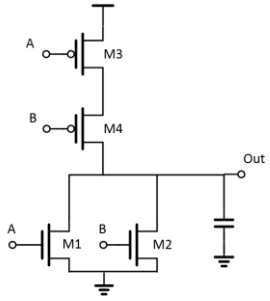

Fig.6: Schematic of NOR2 gate.

5. CONCLUSION

A random variability simulation algorithm has been proposed in this paper. It is based on initial assumptions for channel length variations caused by LER, and V_{TH} variations based on RDF.The promising conclusions stemmed from the accuracy of our results make a new roadmap for the future work in this field. The proposed algorithm can be extended for different channel length transistors in the state of the art technologies. Moreover, it can be used to benchmark modeling of statistical and random variability in a broad range of digital circuits.The

Table 2.Statistical variation of Tpd for NAND2.

state	00		10		01	
	mean	STD	mean	STD	mean	STD
Atomistic	6.30E-12	4.96E-13	6.77E-12	5.40E-13	8.21E-12	7.02E-13
Proposed model	6.37E-12	4.64E-13	6.56E-12	5.34E-13	8.37E-12	7.45E-13

Error (%)	-1.10	6.41	3.09	1.06	-2.00	-6.11

Table 3.Statistical variation of Tpd for NOR2.

State	11		01		10	
	mean	STD	mean	STD	mean	STD
Atomistic	6.07E-12	3.85E-13	6.04E-12	4.96E-13	8.63E-12	7.67E-13
Proposed model	5.82E-12	3.60E-13	5.96E-12	5.18E-13	8.38E-12	7.49E-13
Error (%)	4.11	6.37	1.25	-4.44	2.92	2.33

main advantages of the proposed algorithm are: (i)- it can be easily extended to any target circuit with multi parameters.(ii)- it consumes much less computational resources compared with 'atomistic' simulations while the error remains less than 7% for inverter, NOR2 and NAND2 circuits.

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