Improved Maximally Flat Wideband CIC Compensation Filter using Sharpening Technique

Kalpana Devi M.E. Student, Department of ECE NITTTR Chandigarh, UT, India

ABSTRACT

This paper presents the design and implementation of sharpening of maximally flat cascaded integrator comb compensation filters. The modified sharpened cascaded integrator comb compensation filter is used to improve magnitude response and gain. For wide-band compensation fourth-order linear phase filters is considered. The decimation factor of CIC filter is D and number of adders are depends upon decimation factor D. The compensation filter is a multiplier less design which works at low rate. The comparison within some methods reported in the literature is provided.

Keywords

Cascaded Integrator Comb Filters, Compensation, Decimation, Finite Impulse Response filter, Sharpening

1. INTRODUCTION

The simplest multiplierless decimation filter is cascadedintegrator comb filter proposed in [1] used in communication systems first. But the magnitude response of this filter has high passband droops, which is not desired in many applications. A CIC structure consists of a cascade of N integrators running at a high sample rate and N comb filters, which run at the down sample rate. No multipliers are needed and the storage requirement is minimal which can be viewed in [1]. The transfer function of CIC filter is given by:

$$H_{CIC}(z) = \left(\frac{1}{D}\frac{1-Z^{-D}}{1-Z^{-1}}\right)^{N} = \left[\frac{1}{D}\sum_{i=0}^{N-1}Z^{-i}\right]^{N}$$
(1)

Where, D= Decimation factor

N= Number of stages

However there is droop in pass band gain which depends upon decimation ratio, but can be compensated using FIR filter at second stage in the decimation process. The sharpening filter proposed in [2] can be used to overcome the disadvantages of CIC filter in [1]. The transfer function for sharpened CIC filter is given as [3]:

$$H_{\text{SCIC}}(z) = 3H_{\text{CIC}}^2(z) - 2H_{\text{CIC}}^3(z)$$
(2)

The CIC filter also has the disadvantages that the frequency response of comb filter does not satisfy the design and also required more power. To solve these problems various methods were developed, but if one method is suitable to solve one problem then another problem cannot be solved by that method. The recursive and non-recursive structures can also be used. The non-recursive method results in increase in speed and lower power consumption. The polyphase decomposition also used to reduce the sampling rate of sharpening filter [3]. The sharpening methods of Kaiser and Hamming does not always work so if sharpening a filter twice can overcome the problems with the sharpening method proposed in [4]. Rajesh Mehra Associate Professor, Department of ECE NITTTR Chandigarh, UT, India

Another design of decimation filter called GCFs are suitable for $\sum \Delta$ modulator in terms of better selectivity and quantization noise rejection as compared to conventional comb decimation filter [5]. The decimation filter without multipliers is based on IFIR filter and rounding and sharpening techniques is proposed in [6]. Various investigators also proposes the simple second-order compensation filters for both narrow and wide band compensation with low computational complexity [7] – [9]. The sharpening technique proposed in [10, 11] reduces the pass band droop as well as increase the attenuation in folding band.

Moreover, compensators based on closed form equations are suitable for application in narrow-band software radio receivers. Interpolator has designed by using direct form polyphase serial and Parallel structures and DALUT algorithm based decimator are used to enhance speed and to reduce area proposed in [12]. In [13] authors proposed a high speed CIC decimator SDR and GSM which increases the speed and also saves the resources. A high speed interpolator using embedded LUT structure for software defined radios is proposed in paper [14]. The proposed design increases the speed and also save the resources. In paper [15] compensator based on maximally flat criterion is suitable for narrow-band as well as wide band applications is proposed. The nonrecursive methods proposed in [16, 17] is used to improve the alias rejection in first folding band.

In paper [18] author proposed an optimized half band polyphase decomposition technique used for decimator in multi-rate applications. Paper [19] proposed a hybrid approach for GSM digital down converter. This proposed technique reduces the cost, filter order and hardware complexity. A multirate structure of decimation is proposed in paper [20] is used in many applications.

Optimized hardware co-simulation approach is proposed in [21] for GSM based digital down convertor, which reduces resource requirement. Polyphase decomposition structure is used to improve the hardware complexity and system performance in terms of speed and area is enhanced using embedded multipliers, LUTs and BRAMs.

The main goal of this study is to extend the results given in [15] for wideband CIC compensation filter. Multiplierless design is proposed and closed form equations are used to compute filter coefficients. The forthcoming section represents wideband CIC compensation filters with multiplierless design along with results and discussion followed by conclusion.

2. WIDEBAND CIC COMPENSATOR

Even increasing the number of stages wide and flat pass band frequency response of CIC filters cannot be obtained. So to overcome the resulting response, an FIR filter is used, which has a magnitude response that is the inverse of the CIC filter. Such filters are called "compensation filters." The compensation filter follows the CIC filter for down sampling and for up sampling the compensation FIR filter is placed before a CIC filter.

Here design of linear phase FIR compensation filter, with maximally flat magnitude response is described. The proposed compensation CIC filter is expressed as:

$$G(z) = H(z)P(z)^{D}$$
(3)

Where, H (z) is CIC filter defined in (1) and P(z) is a Type I linear phase FIR filter. CIC decimator is usually followed by second decimator stage. The second stage having decimator factor v and passband edge frequency w_p . The worst case droops occur at $w_p = \frac{\pi}{Dv}$. If $v \ge 4$ filter is narrow band, otherwise it is considered wide-band. From (1), the frequency response of the CIC filter is given by:

$$H(e^{jw}) = e^{-j(D-1)N_w/2}H_R(w)$$
(4)

Where, $H_R(w)$ is a real valued function. The Type I linear phase FIR compensation filter P(z) is given as:

$$P(z) = \sum_{n=0}^{L} a_n z^{-n}$$
(5)

Where, L is an even integer and is the order of P (z) and $n=0,1,\ldots,K$. To design a compensation filter P (z), the error function is defined as:

$$E(w) = P_R(w)H_R(w) - 1 \tag{6}$$

Where,

$$P_{R}(w) = a_{K/2} + 2\sum_{n=0}^{K/2-1} a_{n} \cos\left(w\binom{K}{2} - 1\right)$$
(7)

For maximally flat condition E (0) = 0 and $P_R(0) = 1$

For the design of wide-band compensator L=4 so the transfer function P(z) is:

$$P(z) = a + bz^{-1} + a_1 z^{-2} + bz^{-3} + az^{-4}$$
(8)

By using maximally flat conditions, we get:

$$a = 2^{-8} N.B(2^{-3} N.B + 1 - 2^{-2}C)$$
(9)

$$= -2^{-6}N.B(2^{-3}N.B + 3 - 2^{-2}C)$$
(10)

$$a_1 = 1 - 2a - 2b$$
 (11)

Where, B and C are given as:

$$B = \frac{1 - D^{-2}}{1 - 2^{-2}} , \quad C = \frac{1 - (2D)^{-2}}{1 - 2^{-4}}$$
(12)

For multiplierless design the decimation factor is the power of two in such $asD = 2^{2M-1}$, where M is positive integer. For the design parameters D= 32, N= 5 and v= 2, the resulting passband edge frequency $w_p = 0.0156 \pi$ rad. WB CIC and WB compensated CIC filters at edge frequency having gains -5.54 and -0.58 dB as shown on Fig. 1 and Fig. 2. Blue solid lines represent the wideband compensated CIC and red dotted line represents basic CIC filter magnitude responses. the fig.2 shows the resultant flat pass band of WB CIC compensator, which is obtained by multiplying basic CIC and compensator filter.

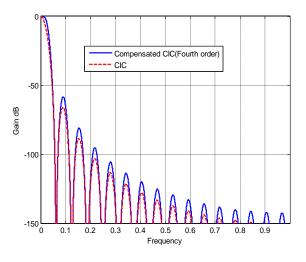


Fig 1: Magnitude Response of the Wideband CIC

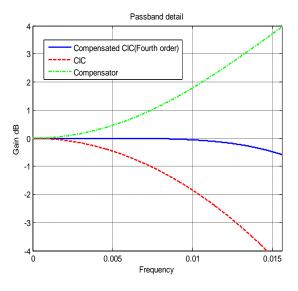


Fig 2: Passband Details of Wideband CIC

3. PROPOSED SHARPENED CIC COMPENSATORS

By using equations (13), (14),(15) for the sharpening of filter coefficients before compensation without changing them, a wideband CIC compensators results in the improved gain , sideband attenuation and also reduces the passband droops. The improved magnitude response is shown in figure 3.

$$H_2(z) = 2 H_{CIC}(z) - H_{CIC}^2(z)$$
 (13)

$$H_{3}(z) = H_{CIC}^{2}(z) - 2H_{CIC}^{3}(z)$$
(14)

$$H_4(z) = H_{CIC}^3(z) - 3H_{CIC}^2(z) + 3H_{CIC}(z)$$
(15)

Figure 3 represents the different magnitude responses of basic CIC, WB compensated CIC, WB 2nd order sharpened compensated CIC, WB 3rd order sharpened compensated CIC and WB 4th ordered sharpened compensated CIC filters.

Magnitude Response

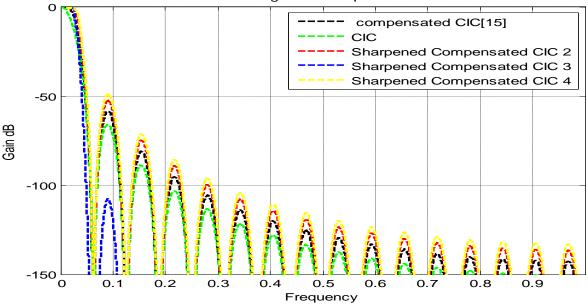


Fig 3: Magnitude Responses Comparison for Wideband CIC Compensators

4. RESULTS AND DISCUSSION

The proposed sharpening technique is applied for maximally flat wideband CIC compensation method. The resulted magnitude 3, and also, Table 1 shows the gain and stop band attenuation of basic CIC [1], maximally flat CIC compensator and proposed 2^{nd} , 3^{rd} and 4^{th} ordered wideband sharpened CIC compensation filter. It is observed that proposed 4th ordered CIC structure after sharpening gives gain 0.034 dB with -49.15 dB stop band attenuation. It is observed that the proposed 2nd, 3rd and 4th ordered sharpening of filter coefficients before compensation provide better attenuation as well as gain than the basic CIC and existing methods of [15]. Proposed 3rd ordered sharpening of CIC compensator gives better side band attenuation among all the techniques. The proposed sharpening of coefficients also improves the passband droops. Proposed 2nd, 3rd and 4th ordered sharpened wideband CIC has -2.91 dB, -4.17 dB and - 3.04 dB, while basic wideband CIC has -3.00 dB passband droop.

Table 1: Wideband	sharpened	CIC compensator details
-------------------	-----------	-------------------------

Filter Type	Gain(dB)	Stopband Attenuation (dB)
CIC [1]	-3.903	-66.17
Reference [15]	-0.4019	-58.53
Proposed 2 nd order sharpening	0.161	-52.53
Proposed 3 rd order sharpening	0.423	-107.5
Proposed 4 th order sharpening	0.034	-49.15

5. CONCLUSION

This paper discusses the design and implementation scheme of sharpening of maximally flat compensated CIC decimation filter employing a fourth order compensator used for wideband applications. Random search algorithm is employed in order to find power-of-2 coefficients for the sharpening polynomial. It is concluded that the proposed 2nd, 3rd and 4th ordered sharpening before compensation provide better attenuation and gain. All the results are carried out using MATLAB simulation. However, as future implementation 2nd ordered sharpened CIC compensator in cascaded combination form can be used to give optimized multiplierless design along with improved magnitude characteristics.

6. ACKNOWLEDGMENTS

The authors would like to thank Director, National Institute of Technical Teachers' Training & Research, Chandigarh, India and Head of Electronics and Communication Engineering Department, National Institute of Technical Teachers' Training & Research for constant inspirations throughout this research work.

7. REFERENCES

- E.B. Hogenauer, "An Economical Class of Digital Filters For Decimation and Interpolation", IEEE Transactions on Acoustics, Speech and Signal Processing, Volume 29, No.2, pp: 155-162, 1981
- [2] G. Stephen, R.W. Stewart, "High-Speed Sharpening of Decimating", Electronics Letters, Volume 40, No.21, pp: 1383-1384, 2004
- [3] G. Jovanovic Dolece, S.K. Mitra, "A New Two-Stage Sharpened Comb Decimator", IEEE Transactions on Circuits and Systems-I, Volume 52, No.7, pp: 1414-1420, 2005
- [4] Shlomo Engelberg, "A More General Approach to the Filter Sharpening Technique of Kaiser and Hamming", IEEE Transactions on Circuits and Systems- II, Volume 53, No.7, pp: 538-540, 2006
- [5] Gordana Jovanovic Dolecek, Naina Rao Nagrale, "On Multiplierless FIR Decimation Filter Design", IEEE Conference On Electronics, Circuits and Systems, pp: 967-970, 2007
- [6] M. Laddomada, "Generalized Comb Decimator Filter for ΣΔ A/D Converters: Analysis and Design", IEEE

Transaction on Circuits and System-I, Volume 54, No.5, pp: 994–1005, 2007

- [7] Gordana Jovanovic Dolecek, Sanjit K. Mitra, "On Design of Two-Stage CIC Compensation Filter", IEEE International Symposium on Industrial Electronics, pp: 903-908, 2009
- [8] G. Jovanovic Dolecek, "Simple Wideband CIC Compensator", IEEE Electronics Letters, Volume 45, No.24, pp: 1270-1272, 2009.
- [9] G. Jovanovic Dolecek, L. Dolecek, "Novel Multiplier less Wideband CIC Compensator", IEEE International Symposium on Circuits Systems, pp: 2119–2122, 2010
- [10] Gordana Jovanovic Dolecek, Vlatko Dolecek, "Novel Sharpened Compensated Comb Decimator", International Research Conference on Trends in the Development of Machinery and Associated Technology, pp: 409-412, 2010
- [11] Shiqian Zhang, Jing Qi, Jie Bao, "The Improvement of Design for CIC Compensation Filter", IEEE International Conference on Electronics Communication and Control, pp: 1712-1715, 2011
- [12] Shiqian Zhang, Jing Qi, Jie Bao, "The Improvement of Design for CIC Compensation Filter", IEEE International Conference on Electronics Communication and Control, pp: 1712-1715, 2011
- [13] Goran Molnar, Mladen Vucic, "Closed-form Design of CIC Compensators Based on Maximally Flat Error Criterion", IEEE Transactions on Circuits and Systems-II, Volume 58, No.2, pp: 926-930, 2011
- [14] Rajesh Mehra, Rashmi Arora, "FPGA-Based Design of High-Speed CIC Decimator for Wireless Applications", International Journal of Advanced Computer Science and Applications, Volume 2, No. 5, pp: 59-62, 2011
- [15] Rajesh Mehra, Sumana Chatterjee, "FPGA Based Design of CIC Interpolator Using Embedded LUT Structure",

ISP Journal of Electronics Engineering, Volume 1, Issue 1, pp: 1-4, 2011

- [16] Fernandez-Vazquez, Alfonso, G. Jovanovic Dolecek, Maximally Flat CIC Compensation Filter: Design and Multiplierless Implementation", IEEE Transactions on Circuits and Systems-II, Volume 59, No.2, pp: 113-117, 2012
- [17] G. Molina Salgado, G. Jovanovic Dolecek, "Non-Recursive Comb Decimation Filter with an Improved Alias Rejection", IEEE Symposium on Circuits and Systems, pp: 1-4, 2012
- [18] Rajesh Mehra, Lajwanti Singh, "FPGA Based Speed Efficient Decimator using Distributed Arithmetic Algorithm", International Journal of Computer Applications, Volume 80, No.11, pp: 37-40, 2013
- [19] Rajesh Mehra, S S Pattnaik, "Reconfigurable Design of GSM Digital Down Converter for Enhanced Resource Utilization", International Journal of Computer Applications, Volume 57, No.11, pp: 41-47, 2013
- [20] Suraj R. Gaikwad, Gopal S. Gawande, "Implementation of Efficient Multirate Filter Structure for Decimation", International Journal of Current Engineering and Technology, Volume 4, No.2, pp: 1008-1010, 2014.
- [21] Rajesh Mehra, Swapna Devi, "Efficient Hardware Co-Simulation of Down Convertor for Wireless Communication Systems", International Journal Of Vlsi Design & Communication Systems, Vol.1, No.2, 2010
- [22] Rajesh Mehra, Shailly Verma, "FPGA Based Design of Direct Form FIR Polyphase Interpolator for Wireless Communication", International Journal of Electrical Electronics &Telecommunication Engineering, Vol. 44, Issue 1, pp.1108-1113, 2013
- [23] Rajesh Mehra, Swapna Devi, "FPGA Based Design of High Performance Decimator using DALUT Algorithm", International Journal Of Signal and Image Processing, Vol.1, No.2, pp.9-13, 2010