Design of NoC Router Architecture using VHDL

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ABSTRACT
Network-on-Chip (NoC) is an advance design method of communication network into System-on-Chip (SoC). It provides solution to the problems of traditional bus-based SoC. It is widely considered that NoC will take the place of traditional bus-based design and will meet the communication requirements of next SoC design. A router is the key component and called as the communication backbone in NoC. This paper presents NoC router architecture which has low latency and requires less area. The design is implemented in VHDL and simulated in Xilinx ISE Design Suite 13.1.

Keywords
Network-on-Chip (NoC); System-on-Chip (SoC); Processing Element (PE); Network Interface (NI); Virtual Channel (VC).

1. INTRODUCTION
As the feature size is continuously diminishing and integration density is enhancing, interconnections have become a predominating element in determining the overall quality of a chip. Due to the fixed scalability of system bus, it cannot meet the necessity of current System-on-Chip (SoC) implementations where only a limited number of functional units can be supported. Long global wires also induce many design troubles, such as noise coupling, routing congestion, and hard timing closure. Network-on-Chip (NoC) architectures have been suggested as an alternative to solve the above problems by using a packet-based communication network [1, 2, 3].

A generic NoC implementation consists of a several Processing Elements (PEs). These processing elements can be placed in different topologies. Most NoCs adopt network topologies like mesh and folded torus for regularity and modularity. Fig.1 shows the NoC architecture using mesh topology. The Processing Elements (PEs) can be various processors, memory elements and dedicated hardware like audio cores, video cores, wireless transceivers etc. Each PE is linked to a local router through a Network Interface (NI). The NI is used to packetize or de-packetize the data into / from the underlying interconnection network. Router finishes the data transmission from source to its destination, based on several routing algorithms and control flow mechanisms. Each router linked to its adjacent routers by physical link forming the packet-based communication network for on chip systems.

The heart of an on-chip network is the router, which undertakes the essential task of guiding and coordinating the data flow. Performance of Network-on-chip is determined by the router architecture to a large extend and virtual-channel router is said to be a promising choice for NoC [4].

The rest of this paper is prepared as follows. Section II will present an overview of routers for Network-on-Chip; section III will introduce NoC router architecture; section IV is about the implementation and results of the design and the last section is conclusion.

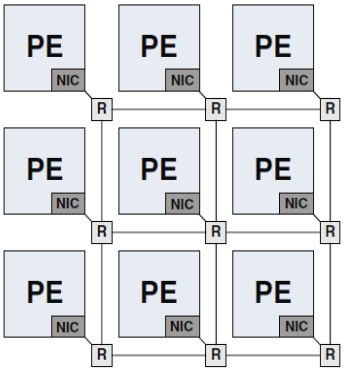

Fig 1: Generic NoC architecture.

2. RELATED WORK
In NoC different switching techniques are used for forwarding information through the network and these techniques have significant effect on the design of router architecture. Switching techniques are broadly categorized into circuit switching and packet switching. Today's NoC designs are based on Packet switching [5].

Packet switching is further categorized into Store and Forward (SAF), Wormhole (WH) and Virtual Cut Through (VCT). But all these techniques face Head-on-Line (HoL) blocking problem, which results from input buffering contention in routers.

To overcome the problems in router switching techniques, researchers have proposed various buffering allocation techniques, micro architectural buffer structures, and effective buffer arbitration algorithms. In [6] J. Dally introduced the idea of virtual channel for deadlock-free routing for networks. The most important improvement in switching technique is the introduction of virtual channels (VCs) [7].

Dally and Towels illustrate the basic virtual-channel router architecture [8] and showed that virtual-channel router works in a pipeline to decrease router delay. In [9] authors introduced low latency virtual-channel router in which a single flit can travel through VC router within only one cycle. In [10], authors introduced a low latency router which uses adaptive routing.

In [11] Virtual channel router is used to solve network deadlock by adopting adaptive routing, and provide guaranteed service and best-effort service in [12].

As Network-on-Chip is strict resource constrained, so a good virtual-channel router should make a better tradeoff between performance and implementation cost.

3. NOC ROUTER ARCHITECTURE
A NoC router consists of number of input ports, a number of output ports, a crossbar switch which connects the input ports to the output ports, and a local port for accessing the Processing Element (PE) connected to this router. In addition

to this, router contains a logic block that decides the overall routing strategy for moving data through the NoC.

When the data in the form of packet is moved from source to its destination, it is sent on the network based on the routing decision taken by each router. At each router the packet is first collected and stored in buffer then the routing decisions are taken and channel arbitration is made by the control logic. Finally the granted packet crosses through the crossbar and reach to the next router. This process repeats until the packet reaches to its destination. The routing unit's control logic is a finite state machine (FSM). It processes the packet header to compute an appropriate output channel and generates requests for that output channel accordingly.

This NoC router architecture mainly consists of three parts:

3.1 Virtual Channel

When a physical channel is divided into a multiple number of logic channels, these logic channels are called as virtual channels. A virtual channel has its own queue, but it shares the bandwidth of the physical channel in a time multiplexed fashion. Virtual channels offer flexibility, better channel utilization and improve network throughput and reduce the effect of blocking.

3.2 Arbiter

An arbiter is required to determine how the physical channel can be shared amongst many requestors. Here fixed priority arbiter is used. In fixed priority arbiter, each input port has its own fixed priority level. Depending on this priority level, an arbiter grants an active request signal with the highest priority.

3.3 Crossbar Switch

The crossbar module in the design is responsible for physically connecting an input port to its destined output port, based on the grant issued by the arbiter.

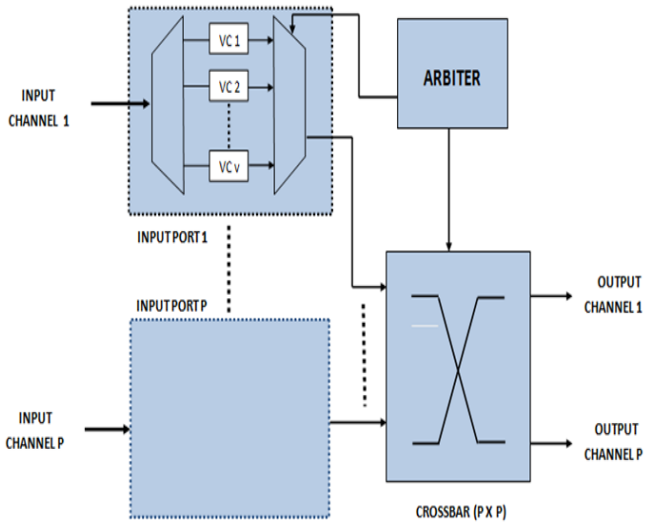

Fig 2: NoC Router Architecture.

4. IMPLEMENTATION AND RESULTS

The router architecture has five input ports, five output ports and each input port has four virtual channels with each VC having four flit buffers. The data coming to each input port is stored in virtual channels temporarily. Each input port sends a request to the arbiter to grant access to the crossbar. So, based on the priority level of each input port, arbiter grants access to the crossbar. Then the data traverse through the crossbar and reached to the destination port.

The design is implemented in VHDL on structural Register Transfer Level (RTL) and it is synthesized and simulated using Xilinx ISE Design Suite 13.1. The router was prototyped in Spartan3 xc3s500e. Here fig. 3 shows the RTL view of NoC router, fig. 4 shows internal blocks of implemented design and fig. 5 shows virtual channel buffer architecture for input port. The simulation result for NoC router is shown in fig. 6 and fig. 7. Here table I shows the comparison of proposed router with other routers [15, 16, 17]. The operating frequency of this router is 210.631MHz. Minimum input arrival time before clock and Maximum output required time after clock is estimated as 3.491ns and 7.225ns respectively. The minimum clock period required is 4.748ns.

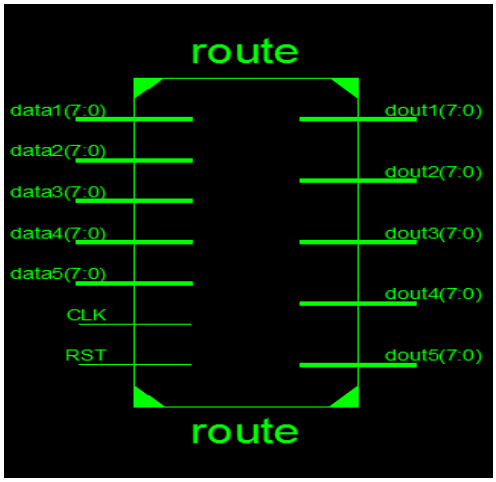

Fig 3: RTL view of NoC Router.

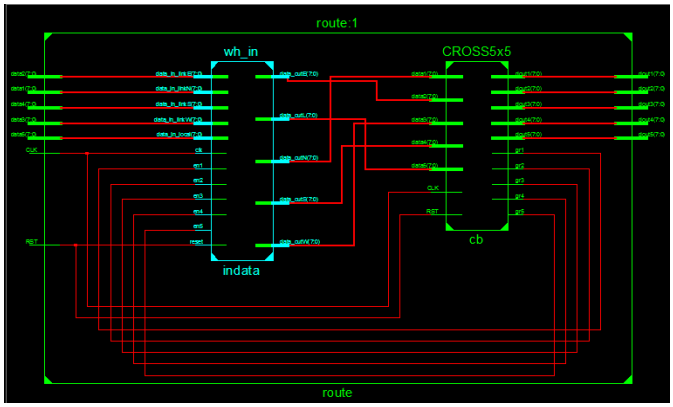

Fig 4: RTL view of NoC Router (Internal block).

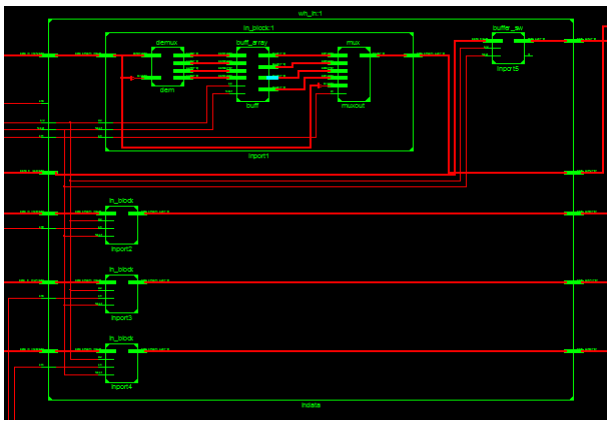

Fig 5: Virtual Channel buffer architecture for input port.

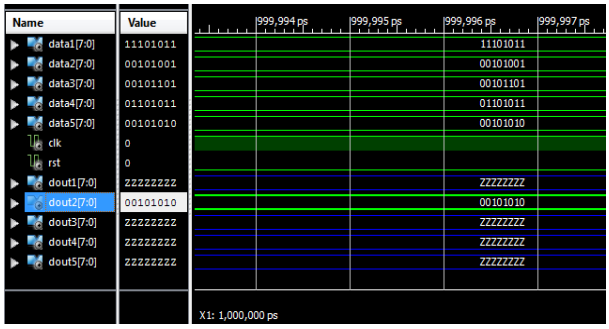

Fig 6: NoC Router Simulation.

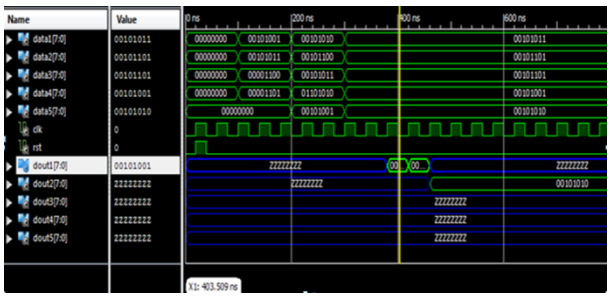

Fig 7: NoC Router Simulation.

Table 1. Comparison between proposed router with other routers.

Resources	5 port router			
	RC [15]	**VC [16]**	**[17]**	**Proposed router**
Target Device	Virtex II XC2VP 30	Virtex II XC2VP 30	3S500E FG320-4	Spartan 3 xc3s500e
Number of Slices	758	861	1464	342
Flip-Flops	398	455	1897	498
LUTS	1515	1722	1901	435
Frequency	----	----	144.196 MHz.	210.631MHz

5. CONCLUSION

A five port NoC router using fixed priority arbiter is proposed in this paper. The synthesis and the simulation of the router is done using Xilinx ISE design suite 13.1 tool. The simulation shows the functionality of NoC router. It is hard to do the comparison directly with other works, so the router area and the frequency of the proposed router are considered for comparison with the other works [15, 16, and 17]. Everton Carara et al. [15], Moraes et al. [16] presented the replicated channel router and virtual channel router which uses switch control for arbitration and Swapna S et al. [17] presented the router with FIFO registers and scheduler which uses round robin algorithm. The virtual channel buffers used in this router provides better channel utilization as well as this router has low latency and requires less area as compare to other routers. As fixed priority arbiter can be used for few requesters and there is no limit to how long a lower priority request should wait until it receives a grant so this can affect the network performance. This router can be modified by using a strong fairness arbiter such as round robin arbiter.

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