Relative Performance Analysis of Different CMOS Full Adder Circuits

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ABSTRACT
Different adder circuits are elementary blocks in many contemporary integrated circuits, which are not only employed to perform addition operations, but also other arithmetic operations such as subtraction, multiplication and division. Full adder is the basic building block of any adder circuit. Area, speed and power are the three main design metrics for any VLSI circuit. In this work, eight different full adders' circuits based on standard (std.) CMOS, CPL, 16-Transistor, DCVSL, PTL, TGA, 14-Transistor and 8-Transistor have been designed and implemented using Tanner EDA simulation tool. In this paper, authors have compared the propagation delay, power consumption and power delay product (PDP) of different full adder circuits by varying supply voltage (V_{dd}).

Keywords
CMOS full adder, Propagation delay, PDP, DCVS, PTL, Tanner EDA tool.

1. INTRODUCTION
In the past, the parameters like high speed, small area and low cost were the major areas of concerned, whereas power dissipation is now gaining the interest of VLSI designers. The growing market demand for low-power VLSI can be addressed at various design levels, such as architecture, logic, circuit and physical design [1]. In circuit level, significant amount of power saving can be obtained by selecting proper logic style for implementing combinational circuits. In recent years, the growth of personal computing devices and wireless communication systems has made power dissipation a most serious design parameter [2]. In the absence of low-power design techniques such applications usually suffer from very small battery life time, while the cost for packaging and cooling increases. Addition is one of the vital and frequently used arithmetic operations in many signal processing and other applications. Bridge transistors design style offers more regularity and higher density than conventional CMOS design style [4]. Adder is one of the most valuable components of a processor which determines its throughput, as it is used in the ALU, and for address generation in case of cache memory [5]. Misra et al. introduced a new transistor resizing approach for 1bit full adder (FA) cells to determine the optimal sleep transistor size which reduce the leakage power and area to minimize leakage current [8]. In [9], two high-speed and low-power full-adder cells have been designed with an unconventional internal logic structure and pass-transistor logic styles which lead to reduce power-delay product. Samanta et al. derives analytical expression for the delay model of a CMOS inverter including all sorts of secondary effects which may occur in the Ultra Deep Submicron MOS devices [6]. The performance of 1-bit FA has compared using different CMOS logic design styles in [12-14]. The functionality and performance analysis of different 8-bit adder topologies are described in [15]. The 1 bit-full adder is designed using adiabatic logic for low power application in [16].

In this work, 8 different FAs are compared in terms of propagation delay, average power consumption and power delay product (PDP). Performances of different adders are measured by varying the constant supply voltage. The rest of the paper is organized as follows. In Section 2, 8 different FA circuits are discussed in brief. Simulation results are given in Section 3. In Section 4, analysis of result has been carried out. The paper is concluded in Section 5.

2. DESIGN OF DIFFERENT FA
In this Section, brief description of 8 different circuits of 1-bit FA is discussed. In FA, two input bits along with the previous carry are added to produce sum and carry output. The output expression of sum (S) and final carry (C_0) are as follows.

$$S = A \oplus B \oplus C_i \quad \&$$
$$C_0 = AB + (A+B)C_i$$

Where A, B are data input and C_i is the previous input carry. Design of different FA circuits are explained in the following subsection.

2.1 Standard CMOS FA
In Figure 1, the CMOS FA is implemented by using standard CMOS logic [2]. Total 28 numbers of transistors are needed for this configuration. The sum expression is given as follows.

$$S = ABC_i + C'_0 (A+B+C_i)$$

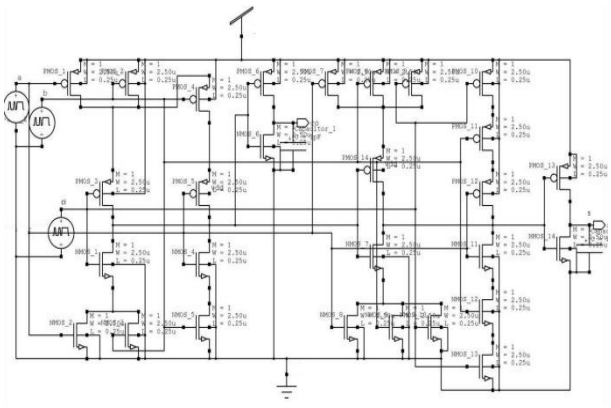

Fig 1: Schematic view of the Standard CMOS FA

2.2 Complementary pass transistor logic FA

The complementary pass transistor logic (CPL) FA shown in Fig. 2 is made up of NMOS pass-transistors which have differential inputs and outputs. CPL circuits consume less power than usual static logic circuits due to the logic output voltage swing of the pass transistor is less than the supply voltage level [10].

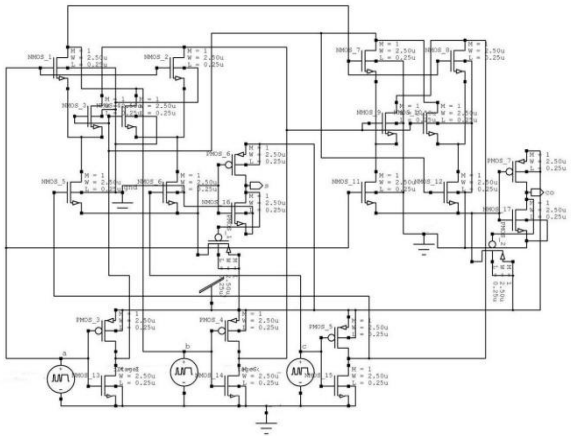

Fig 2: Schematic view of the CPL FA

2.3 16-Transistor FA

The 16-transisitor FA shown in Fig. 3 is based on the 4-transistor design of the XOR and XNOR functions. The cell delay decreases in any design by using pass transistor and transmission gates of the cell. This adder does not employ any inverters or standard CMOS style. This reduces the short-circuit power component within the cell. The incomplete voltage swing for some input combinations (say, a = b = 0, a = b = 1) minimizes the power consumed in these [11].

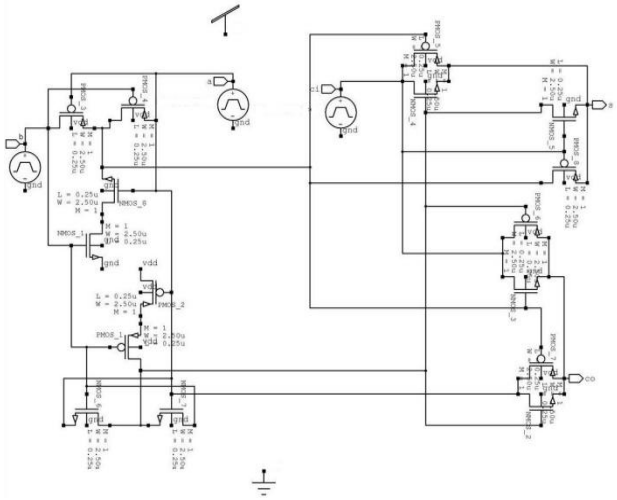

Fig 3: Schematic view of 16-Transistor FA

2.4 DCVSL FA

Differential Cascode Voltage Switch Logic (DCVSL) FA is shown in Fig 4, It diminished the transistor counts over NAND/NOR implementations. DCVSL has got enhanced performance of about 4 times as compared to the CMOS/NMOS NAND/NOR circuits and retaining the low power circuitry [10].

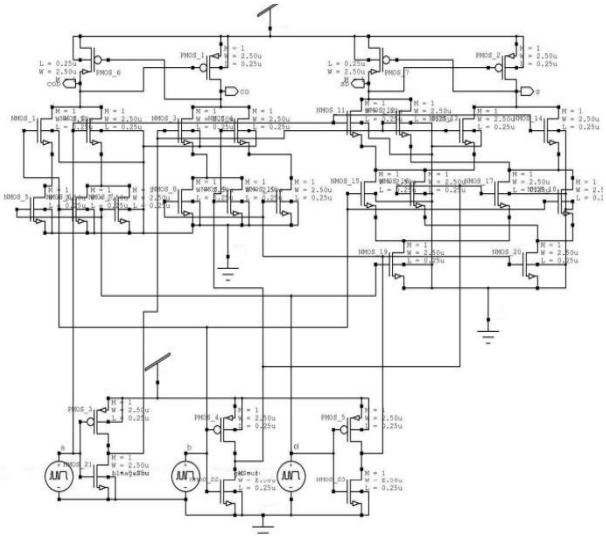

Fig 4: Schematic view of the DVCVSL FA

2.5 Pass Transistor Logic FA

Pass transistor logic (PTL) FA is shown in Fig. 5. The main advantage of using the CMOS-based PTL circuits is that the number of transistors can be reduced acutely compared to those based on conventional CMOS. Say, only two transistors are needed for both the OR and AND gates, whereas a total of six transistors are used in the corresponding standard CMOS circuit. For XOR gate using PTL logic only 2 transistors are needed.

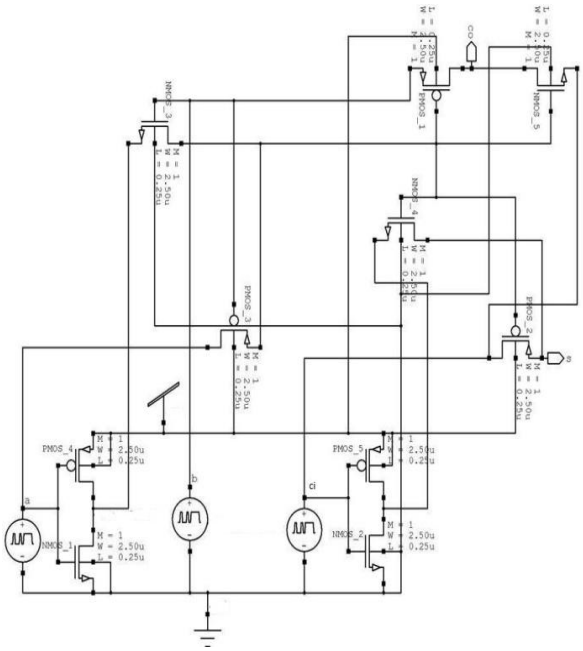

Fig 5: Schematic view of PTL FA

2.6 TG-Based FA

Transmission Gate based adder (TGA) is shown in Fig. 6, It is widely used CMOS design style to implement many digital system. TG based design is similar to pass transistor with the difference that transmission gate logic uses nMOS and pMOS transistors where as pass transistor logic uses either nMOS or pMOS [5].

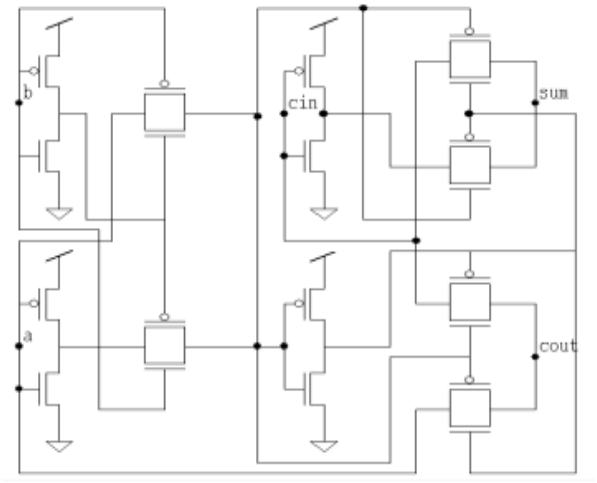

Fig 6: Schematic view of TGA FA

2.7 14-Transistor FA

The 14-transistor (14T) adder uses only one inverter, but it still has the similar drawback of glitches in the outputs. Also, it has some limitations of introducing a static power component at the inverter output. Due to the incomplete voltage swing of the XOR gate when a = b = 0, both the N and P transistors will be ON, which will direct to draw current from the power supply although the circuit is in balanced state. This shortcoming increases the power consumed by this cell, but still it remains a good candidate for low power applications [3].

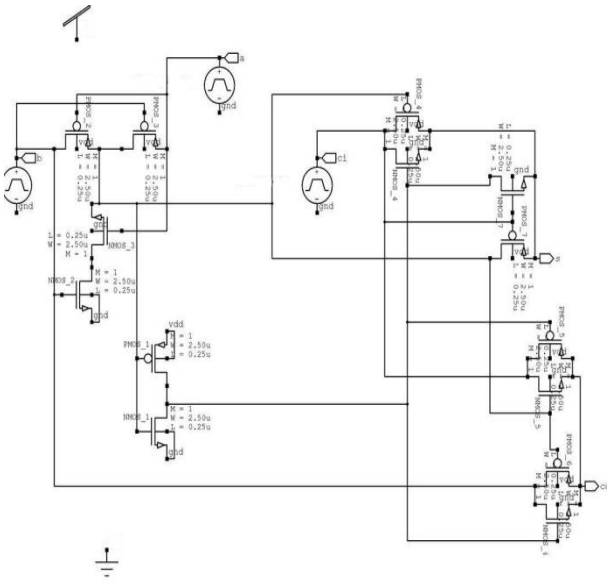

Fig 7: Schematic view of 8-Transistor FA

2.8 8-Transistor FA

8-Transistor (8T) FA is shown in Fig. 9. The design of the FA is based on the design of the XOR gate. The design of 8-T FA uses three transistor XOR gates [7] which is shown in Fig. 8. The design is based on a customized version of a CMOS inverter and a PMOS pass transistor. The function of left inverter is similar to a normal CMOS inverter when the input b is at logic high.

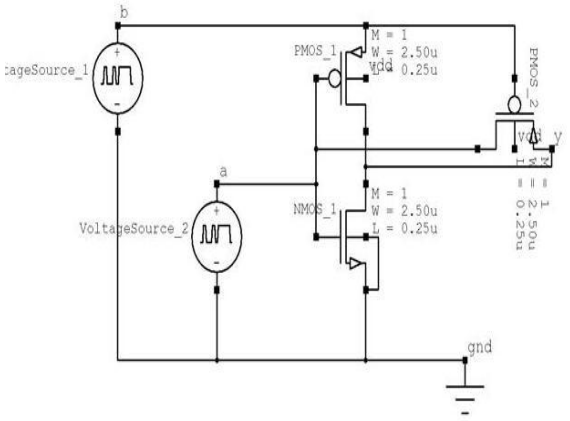

Fig 8: Design of 3-Transistor XOR gate

Therefore, the output y is the complement of input a. When the input b is at logic low, the CMOS inverter output is at high impedance. The operation of whole circuit is thus like a 2 input XOR gate. However, when a=1 and b=0, voltage degradation due to threshold drop falls across transistor PMOS2 and consequently the output y is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably reduced by enhancing the W/L ratio of transistor of second PMOS. This design of proposed FA is based on three transistor XOR gate. It acquires least silicon area. The design of 8T FA is shown in Fig.9. The heart of the implementation is based on a modified version of a CMOS inverter and a PMOS pass transistor.

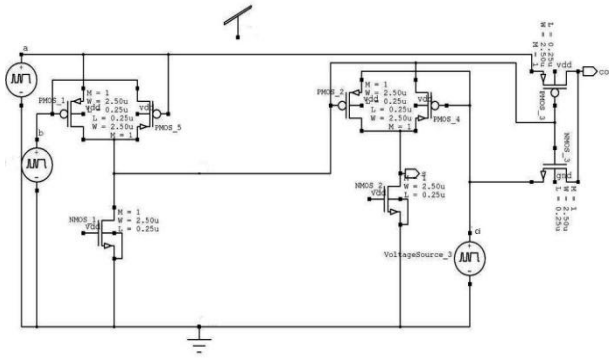

Fig 9: Schematic view of 8-Transistor FA

3. SIMULATION RESULTS

In this section, simulation results have been elaborated. To compare FA performance, we have evaluated delay and power dissipation by performing simulation runs on a Tanner14.1 Spice simulation environment using a 250nm CMOS technology. The simulations have been performed for different constant power supply voltages. Each one-bit FA has been analyzed in terms of propagation delay, minimum, maximum and average power dissipation and PDP. The propagation delay has been measured as the time interval between the time the input signal takes to reach 50% of its logic swing and the time the output takes to reach the same value. The input and output waveforms of sum and carry bit of CMOS FA is taken from Tanner simulation tool, which is shown in Fig. 10.

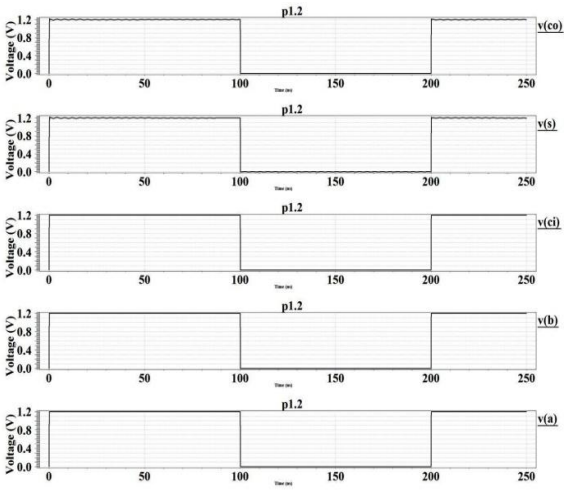

Fig 10: Input & Output waveforms of FA

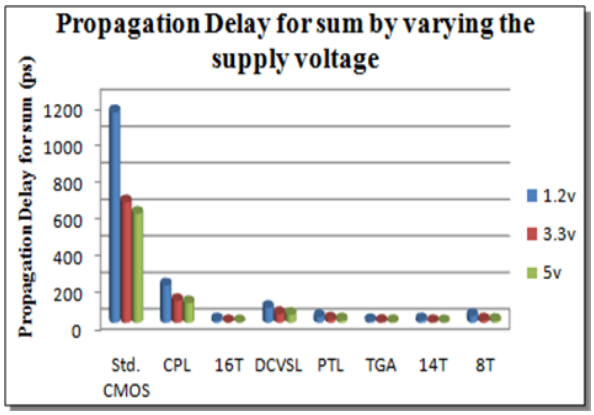

Fig 11: Propagation delay of sum for different adder by varying V_{dd}

In Figure 11, shows the propagation delay of sum bit for different adder circuit by varying V_{dd} (1.2V, 3.3V and 5.0V).

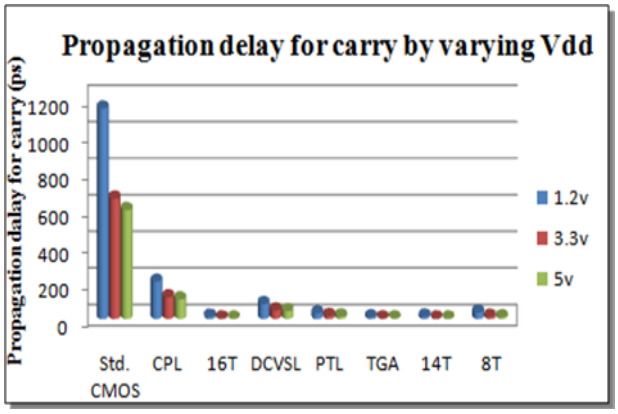

Fig 12: Propagation delay of carry for different adder by varying supply voltage

In Figure 12, shows the propagation delay of carry bit for different adder circuit for the three different values of supply voltages.

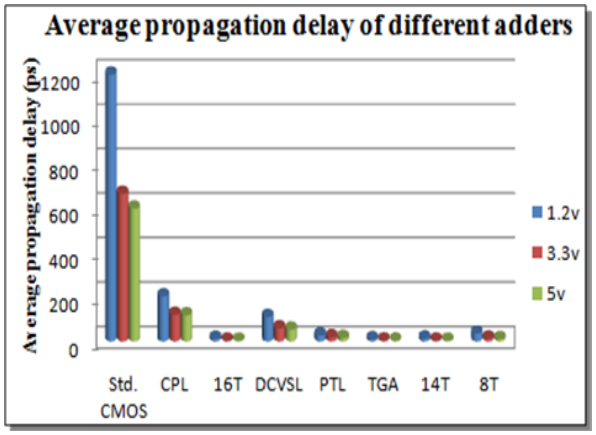

Fig 13: Avg. Propagation delay for different adder by varying V_{dd}

In Figure 13, propagation delay for different adder circuit are compared varying the supply voltages (V_{dd}=1.2V, 3.3V & 5.0V).

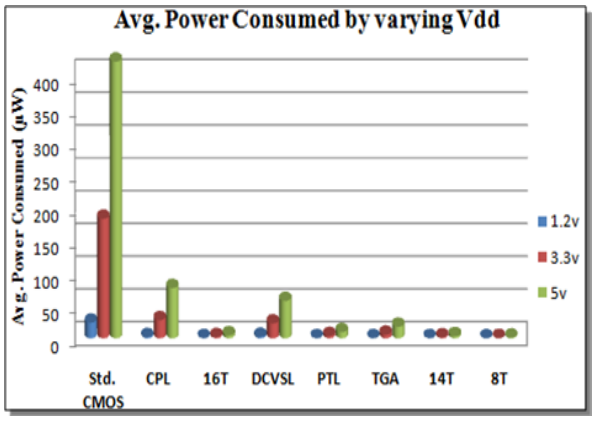

Fig 14: Avg. Power consumed for different adder by varying V_{dd}

In Figure 14, avg. power consumption for different FA is shown for different supply voltages.

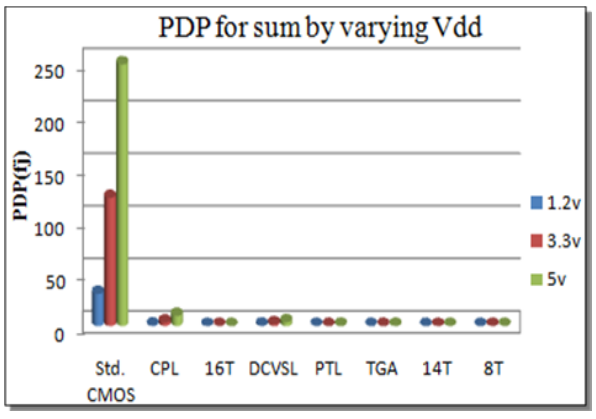

Fig 15: PDP of sum for different adder by varying V_{dd}

In Figure 15, power delay product of sum bit for different adder for different supply voltages.

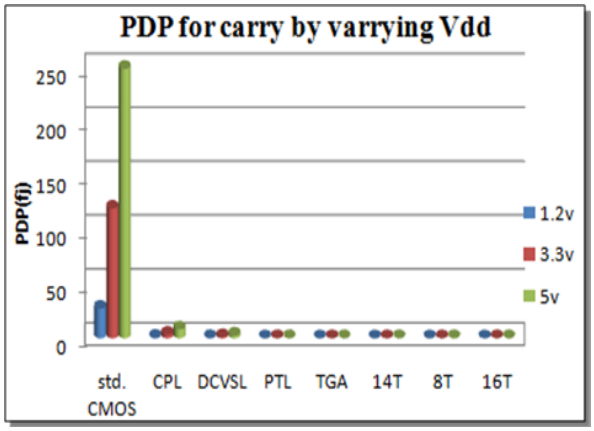

Fig 16: PDP of carry by varying V_{dd}

In Figure 16, shows the variation of PDP of carry bit for different adder with different supply voltages.

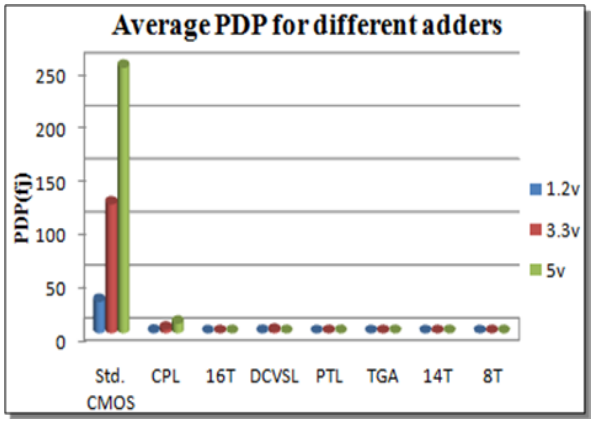

Fig 17: Avg. PDP of carry by varying V_{dd}

It is observed from Fig. 17 that the average PDP of different adder is varying with different supply voltages.

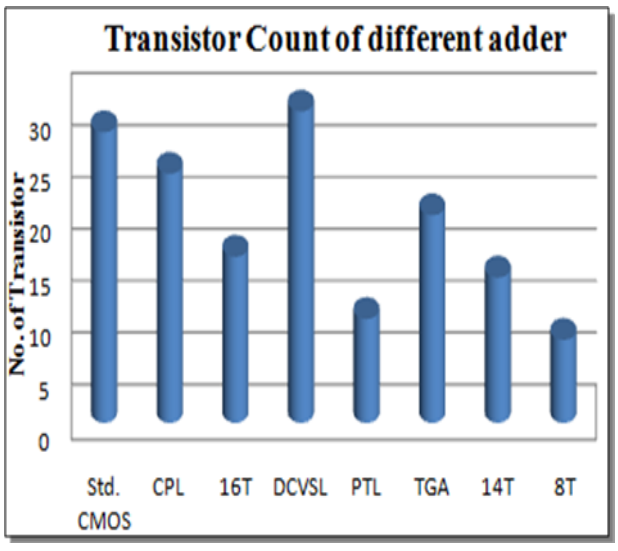

Fig 18: Number of transistor required for different adders

Figure 18, shows the number of transistors required to implement the different adder. The least number of transistors are required in 8T FA and highest numbers of transistors are required in CPL FA. In the following section result has been analyzed.

4. RESULT ANALYSIS

The 8 FA circuits like Std. CMOS, CPL, 16-Transistor, DCVSL, PTL, TGA, 14-Transistor and 8-Transistor FAs are compared in terms of propagation delay, Avg. power consumption, Power delay product (PDP) and transistor complexity. The details results are obtained by employing Tanner14.1 EDA simulation tool which is shown in Table 1. The bold data are showing the minimum value of the different performance parameters. From Table 2 it is noted that summery of all results are given. In the next subsection, comparative study analysis has been done.

From Table 2, it is observed that the smallest propagation delay is found in 16T FA for medium and high supply voltage and in TG FA for lower supply voltage. Maximum propagation delay is found in std. CMOS FA for any supply voltage.

It is also noted that the smallest & highest power consumed in Std. CMOS & 8T FA for any supply voltage.

It is also noted that the smallest power delay product is obtained in 14T FA for lower and medium supply voltage and in TG FA for lower supply. Maximum PDP is found in std. CMOS FA for all supply voltages.

Table 2. Performance summery of different FA

Measuring Parameter	V_{dd}=1.2V		V_{dd}=3.3V		V_{dd}=5.0V	
	Max	**Min**	**Max**	**Min**	**Max**	**Min**
avg. propagation delay	std. CMOS	TGA	std. CMOS	16T	std. CMOS	16T
avg. power consumed	std. CMOS	8T	std. CMOS	8T	std. CMOS	8T
avg. PDP	std. CMOS	TGA	std. CMOS	14T	std. CMOS	14T

5. CONCLUSION

In this paper, 8 different FA circuits like standard CMOS, CPL, 16-Transistor, DCVSL, PTL, TG, 14-Transistor and 8-Transistor are designed and implanted using Tanner EDA simulation tool for 250nm technology. Delay, power consumption and power delay product of different FA have been computed and compared. It is observed that delay decreases and power dissipation increases with the increase of $V_{dd.}$ It is noted that all three parameters have maximum value for std. CMOS FA and average power dissipation is minimum for 8T based FA. VLSI designer can easily design adder circuits employing these results. Employing these optimized full adder circuits, multi bits adder with different architectures can be designed.

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Table 1. Performance of different CMOS FA circuits for different Supply Voltages

Sl. No.	Different FA	Variation of Supply Voltage	Propagation Delay for sum (ps)	Propagation Delay for carry (ps)	Avg. Power Consumed (µW)	PDP for Sum (fJ)	PDP for Carry (fJ)	Transistor Count (Normalized)
1	Std. CMOS FA	1.2	1286.60	1152.50	23.86	30.67	27.50	28(3.5)
		3.3	667.98	659.44	182.39	121.83	120.28	
		5.0	598.80	596.60	422.06	248.93	251.80	
2	CPL FA	1.2	201.19	204.13	1.93	0.39	0.39	24(3)
		3.3	120.48	118.55	27.66	3.33	3.28	
		5.0	126.35	107.99	76.69	9.69	8.28	
3	16-T FA	1.2	11.56	12.91	0.25	0.0029	0.0032	16(2)
		3.3	**3.02**	**3.39**	2.00	0.006	0.0068	
		5.0	**2.35**	**2.66**	4.55	0.0107	0.0121	
4	DCVSL FA	1.2	137.86	81.64	2.30	0.31	0.19	30(3.75)
		3.3	70.65	47.35	22.68	1.60	1.07	
		5.0	62.74	43.22	57.11	3.58	2.47	
5	PTL FA	1.2	23.67	30.21	0.17	0.004	0.005	10(1.25)
		3.3	18.91	17.19	3.40	0.064	0.058	
		5.0	17.15	13.69	9.50	0.163	0.13	
6	TGA FA	1.2	**9.34**	**9.33**	0.24	**0.002**	**0.002**	20(2.5)
		3.3	4.05	4.04	5.66	0.023	0.023	

		5.0	3.45	3.41	17.53	0.06	0.059	
7	14-T FA	1.2	12.19	13.70	0.20	0.002	0.003	14(1.75)
		3.3	3.07	3.46	1.46	**0.0045**	**0.005**	
		5.0	2.40	2.73	3.25	**0.0078**	**0.0089**	
8	8-T FA	1.2	33.98	35.96	**0.09**	0.003	0.0032	**8(1)**
		3.3	12.32	12.53	**0.45**	0.0055	0.0056	
		5.0	10.56	10.45	**1.15**	0.0121	0.012	