A Novel Design of SET-CMOS Half Subtractor and Full Subtractor

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ABSTRACT
Single Electron transistor have high integration density, ultra-low power dissipation, ultra-small size, unique coulomb blockade oscillation characteristics which makes an attractive technology for future low power VLSI/ULSI systems. The Single Electron Transistor have extremely poor driving capabilities so that direct application to practical circuits is a yet almost impossible, to overcome this problem and to investigate the robustness and fastness of the novel design, the hybrid circuits of SET and CMOS are builded. In this work, novel design of SET-CMOS of Half Subtractor and Full Subtractor circuits are designed.

Keywords
SET-CMOS, hybrid CMOS-SET circuits, SET modeling and simulation.

1. INTRODUCTION
The electronic devices are used to increase the operational speed and reduction in power. Researchers in single electron devices are mostly accepted to replace the present CMOS technology [1,2]Single Electron transistors are often discussed as element of nanometer scale electronic circuit because they can be made very small and they can detect the motion of individual electrons. The real problems preventing the use of SETs in most applications are their low current drivability, small voltage gain, high output impedance, high sensitivity to background charges [3,4]. Since CMOS device have advantages that can compensate for the drawbacks of SETs, hybrid CMOS-SET circuits that combine both SET and CMOS device is one of the possible solutions to the problems of Single electron transistor.

The SET made Single electron device(SED) attracted lot of attention for future large scale integration because of its low power nature, small size and allowance of manipulation of individual electrons. Single electrons make use of the available possibility and control the movement and position of a single electron or a small number of electrons. The elementary principle of single electronics is the coulomb blockade, first observed and studied by Gorter [5]. The SEDs make use of the Coulomb blockade(CB), which occurs in tiny structures made from conductive material due to the electrostatic interactions of confined electrons. The development of coulomb blockade, single electron tunneling and related phenomena from the physical point of view have been observed in semiconductor SET, metallic nanostructure device, low dimensional organic nanostructure, etc. Thus, the Single Electron Transistor Circuit has advantages of reducing the power consumption as a single electron is sufficient to store information, which is not in the case of CMOS circuits.

The instability and reliability problem is controlled by extremely low power operation. Also the speed power produce is predicted to lie close to the quantum limit set by the Heisenberg's Uncertainty principle. The SEDs are confined in a small space so that the integration density is higher than the CMOS based VLSI/ULSI level. The feature of SET is the generality and robustness of the effect and the relative simplicity of the device structures, it makes the single electronics the most likely candidate for future ultra-dense digital circuits. Furthermore, the noise during operation is ultra-low for single electron devices [6].

The SETs are made by placing two tunnel junctions in series. The two tunnel junctions craft the "Coulomb Island" where electrons can only enter by tunneling through one of the insulators. The device consists of three terminals very much similar to CMOS transistors; the outside terminal of each tunnel junction, and a gate terminal which is capacitively coupled to the node amid the two tunnel junctions. The capacitor acts as third tunnel junctions, however it is much thicker than the others so that no electrons can tunnel through it. The capacitor here resembles a way of setting the electric charge on the coulomb island [7]. The prior conditions for successful tunneling are that when the gate voltage is et tom Zero, very little tunneling occurs in the course of the two tunnel junction fig 1(a). and the fig. 1(b) shows the basic Structure of SET.

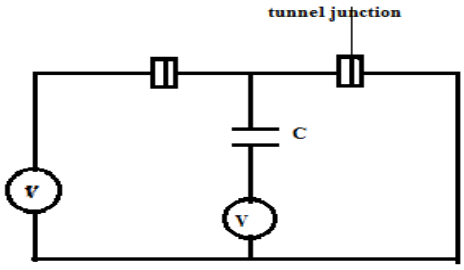


Fig 1(a) is a view of two tunnel junction in series of SET

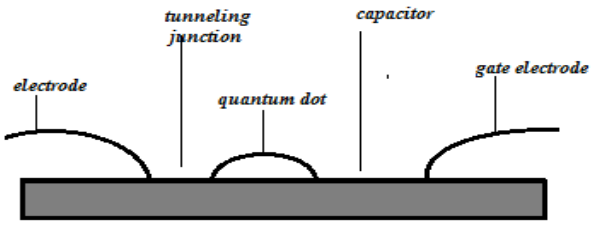
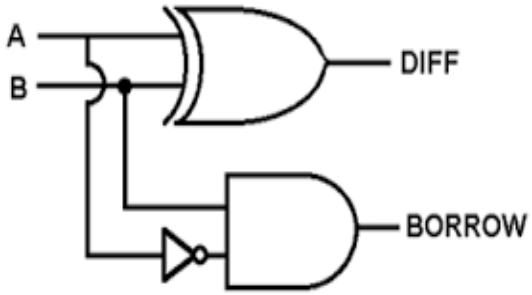


Fig 1(b) shows the basic structure of |SET

This Phenomenon of opposition of tunneling is called the Coulomb blockade. Considerably if the gate voltage is raised to e/2C it corresponds to half of the charge of an electron on the plates of the gate capacitor; next the tunneling current rises dramatically. The SETs will harvest the new seeds of next generation consumer electronics in digital electronics industries. Therefore, it is high time for the researchers to ponder over new direction of fast switching, low power and less space consuming logic circuits, vice conventional circuits to meet the growing demands of industries.

Thus researchers whenever intend to scale down computer chips even smaller, the idea of incorporating SETs has become increasingly appealing. Like several other electronic devices, they uphold the potential to reach the molecular scale and would confine itself in far less space as compared to their conventional counter parts. The small size, fast in action, and low power dissipation of SET circuits make them potentially useful and best competent for next generation logic and memory circuits [8].

2. HALF AND FULL SUBTRACTOR

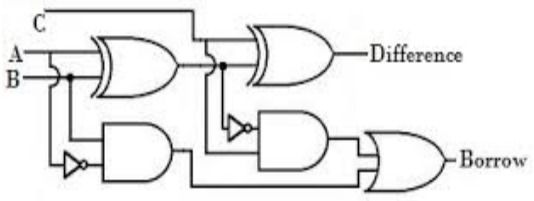


TRUTH TABLE:

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Fig 2 shows the logic circuit and truth table of half subtractor

The Half Subtractor and Full Subtractor is a combinational circuit which is used to perform subtraction of 2 bits and 3 bits. It has 2 inputs and 2 outputs for half subtractor, 3 inputs and 2 outputs for full subtractor. The logic circuit and truth table of half and full subtractor are shown in the fig. 2,3.



TRUTH TABLE

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Fig 3 shows the logic circuit and truth table of full subtractor

The circuit of a hybrid SET-CMOS Inverter proposed which is formed by a PMOS transistor as the load resistance of an SET. Although it resembles a CMOS inverter, there are two difference in the pull down transistor is a SET and the VDD is defined by the SET device parameters.

Since the MIB model is valid for |VDD| ≤3e / Cε [9] for single / multiple gate (s) and symmetric (or) asymmetric SET devices, the bias Voltage is taken as 800mv. The values of the tunnel junction capacitors are CTD and CTS have be designed to prevent tunneling due to thermal energy. Based on the idea that serial connection is AND and Parallel connection is OR, the circuit of 2 input NAND, 2 input NOR and 2 input XOR are realized using the hybrid CMOS-SET inverter. The circuits of 2 input NAND, 2 input NOR, and inverter are shown in Fig 4(a),4(b), 4(c), 4(d).Using the structure of CMOS counterparts, the Circuits of half subtractor and full subtractor are designed and implemented using the hybrid logic gates are shown in fig 5,6. The simulation results are shown in fig.7(a), 7(b).

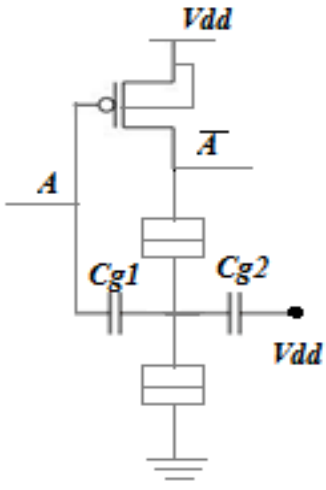


Fig 4(a) shows the SET-CMOS Inverter Circuit

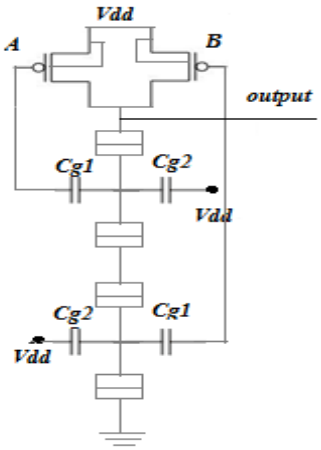


Fig 4(b) shows the 2 Input of SET-CMOS NAND gates

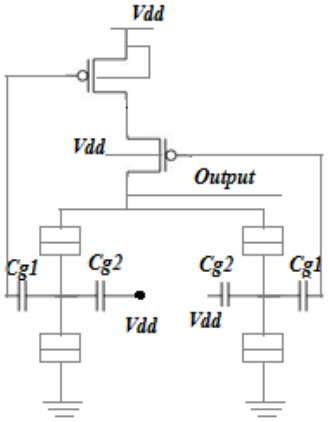


Fig 4(c) shows the 2Input of SET CMOS circuit of NOR gate

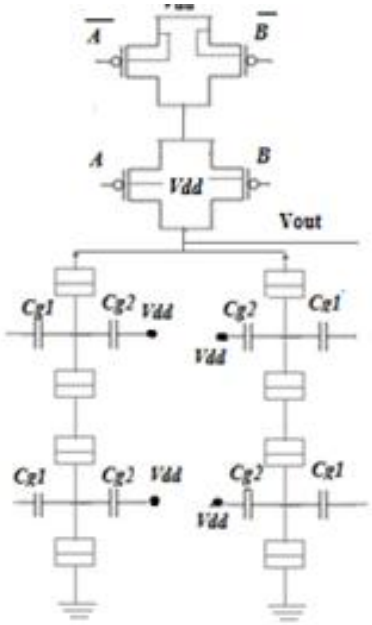


Fig 4d shows the 2 input of SET-CMOS XOR gate

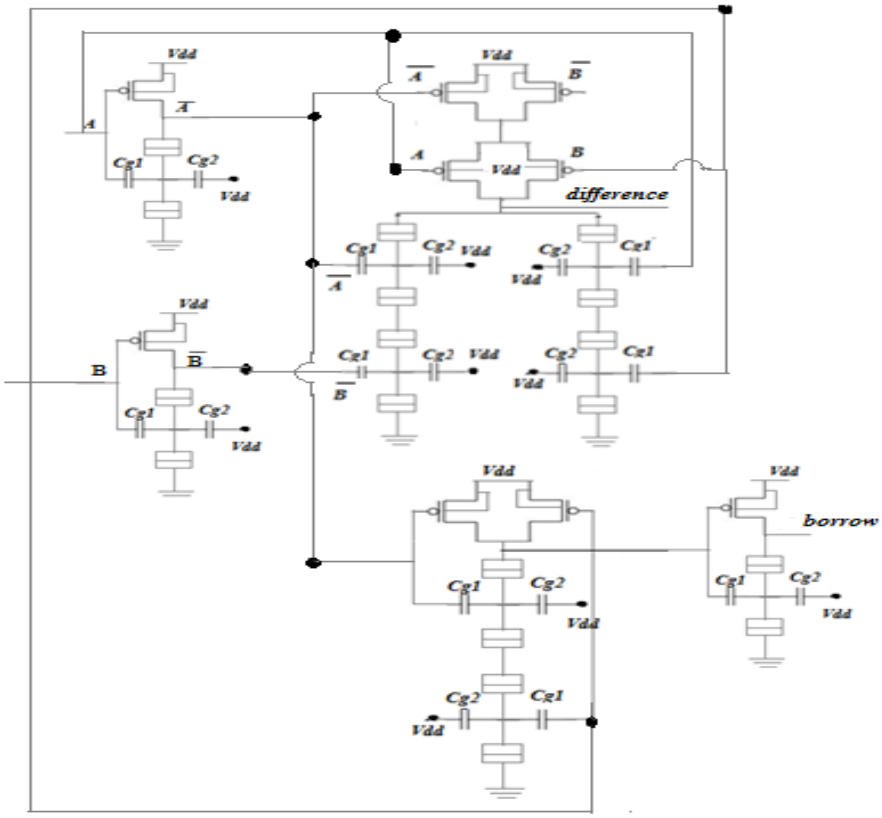


Fig 5 shows the CMOS-SET circuit of Half Subtractor

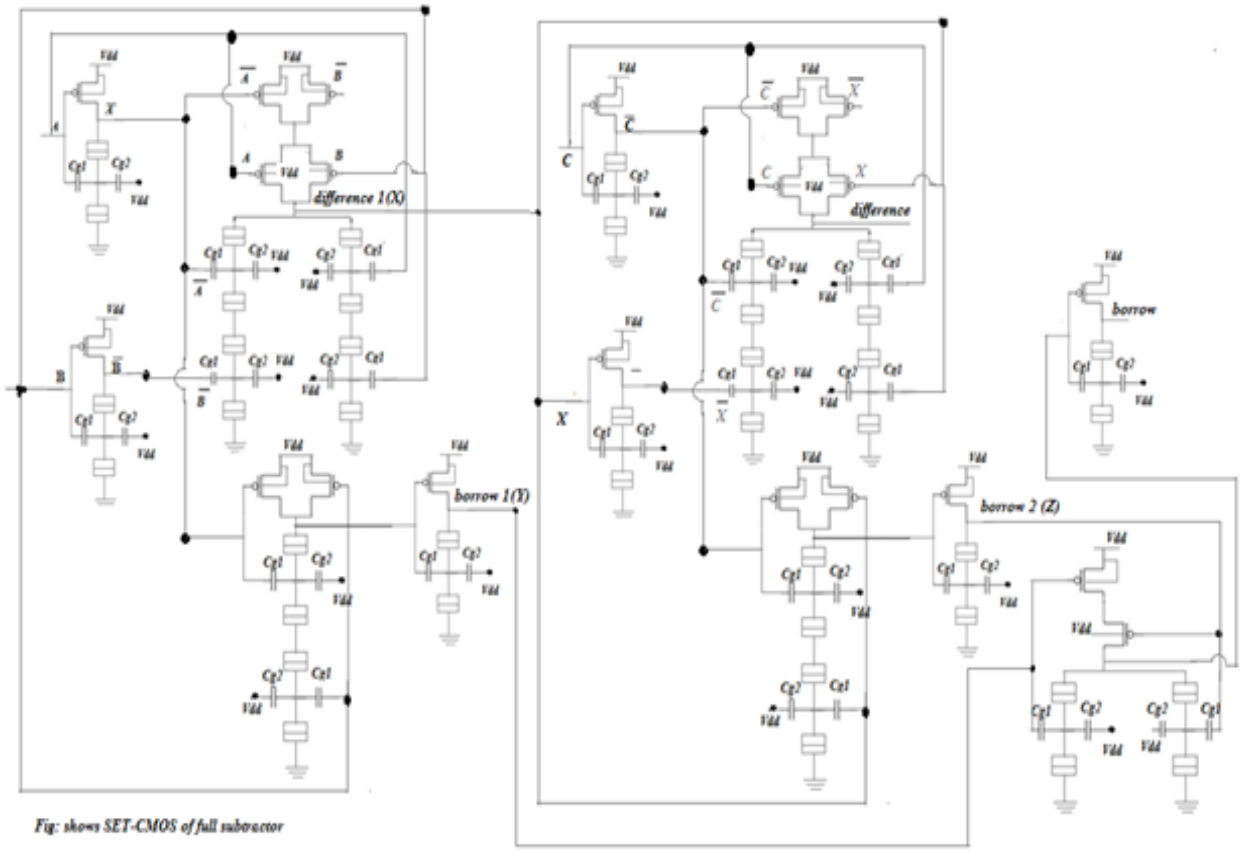


Fig: shows SET-CMOS of full subtractor

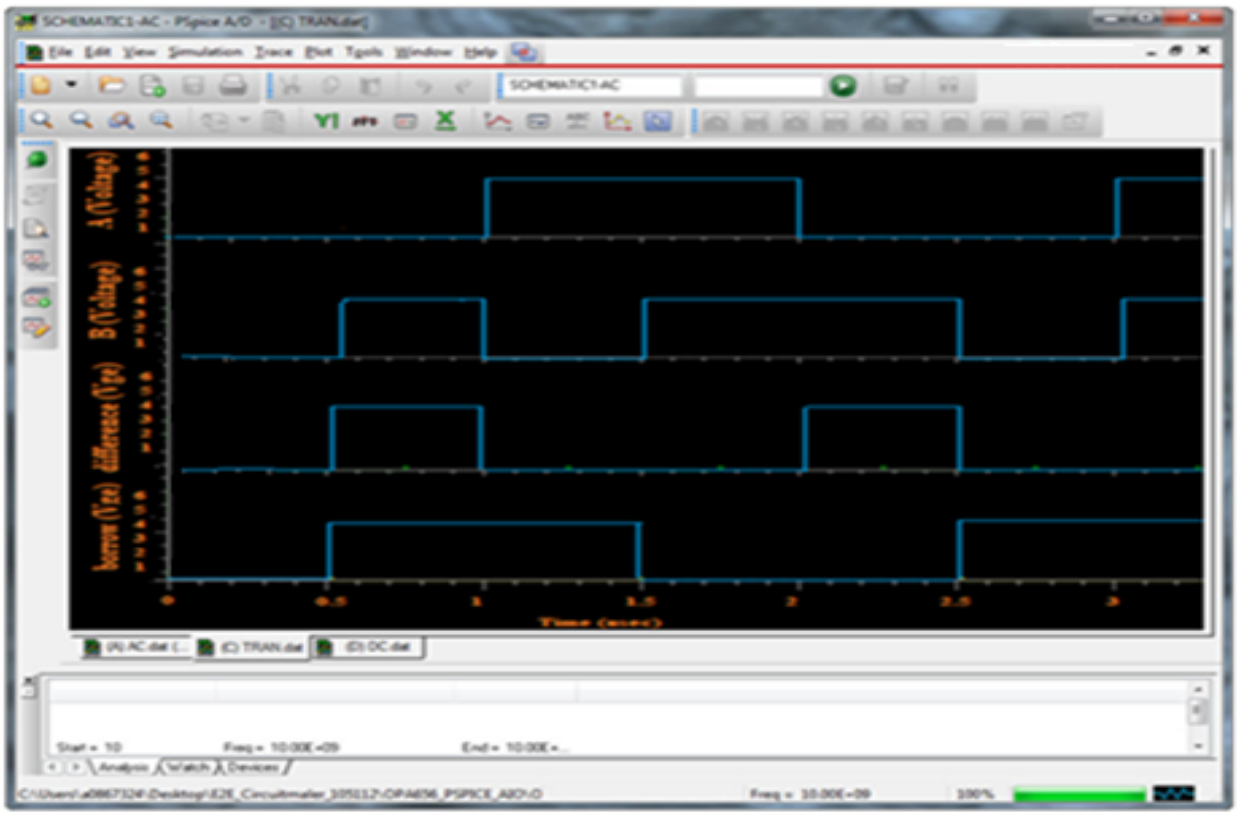


Fig: 7(a) output of half subtractor

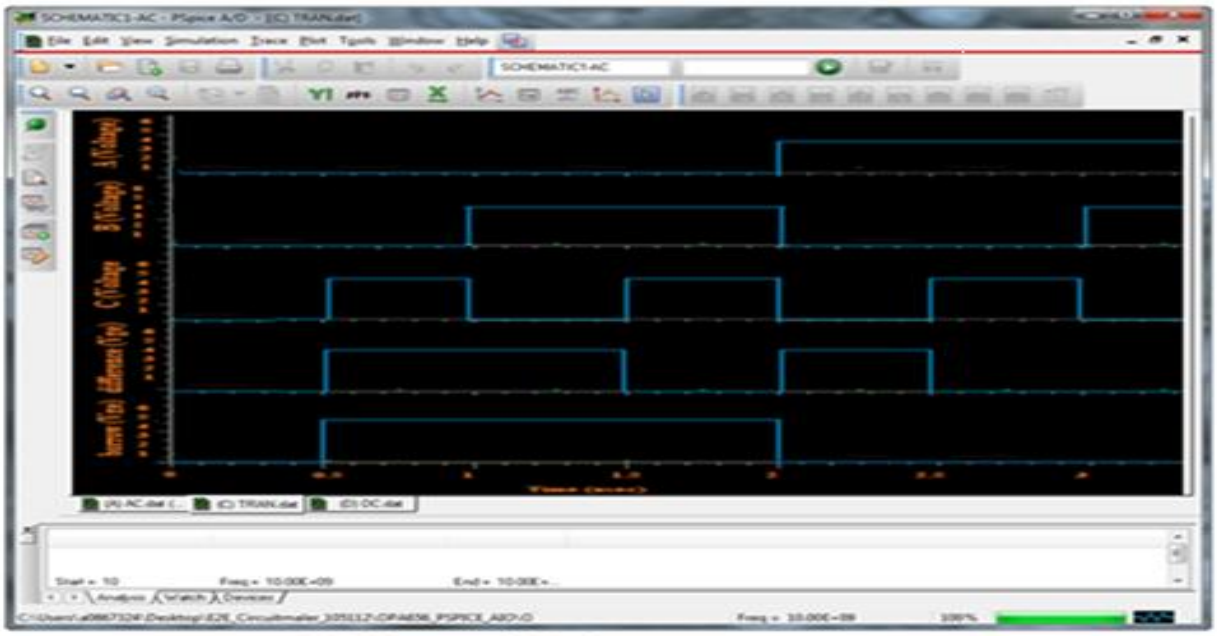


Fig: 7(b) output of full subtractor

3. RESULT AND DISCUSSION

Many simulators and modeling methods have been made for SET devices and circuits. SIMON, MOSES, SECS are popular SET simulation tools based on Monte Carlo method. SIMON and MOSES are not SPICE compatible. The SPICE macro model can be used to describe the behavior of SET transistors used to describe the behavior of SET transistors as independent elements with CMOS transistors in are of interconnection capacitance node between SET and CMOS devices is large enough. The proposed circuits are simulated using the MIB compact model. The island, gate and tunnel capacitors of SET designed for room temperature operation and the supply voltage Vdd is taken to 08V [10,11].

Design parameters of the SET transistor are CTD = CTS = 0.15aF, Cg1 = Cg2 = 0.2aF and RTD = RTS = 1MΩ. The BSIM4.6.1 predictive model is examined the behavior of CMOS transistor through SPICE simulations. Design parameters of CMOS transistor are W/L = 64/54nm, Vth = -0.3V for PMOS and Vth = 0.47V for NMOS

4. CONCLUSION

Our designed room temperature operable hybrid SET-CMOS based half subtractor and full subtractor. This papers presents successful attempt in making feasibility of using the proposed hybrid circuits in future low power ultra-dense VLSI/ULSI circuits.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

[1] Lageweg. C.et al. Single electron encoded latches and flip flops, IEEE Trans. Nanotechnology 3(2, 237-248 (2004)

[2] Wu, G., Cai, L., Kang: A 8 bit parity code generator based on multigate SET, IEEE, NEMS, 183-186 (2008)

[3] Santanu Mahapatra, Adrian Mihai Ionescu, Hybrid CMOS SET device and circuit design-Artech House, Inc 2006

[4] Inokawa, Takahash, A multiple valued logic and memory with combined Single electron and metal oxide semiconductor transistors, IEEE trans. Electron devices50(2), 462-470(2003)

[5] Gorter C.J., A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strengths. Physics 17(8), 777-780(1951)

[6] Mizugaki Y. Blocking Charge Oscillation in a series array of two tiny tunnel junctions with resistive ground path from its island. (2012), 194-192 IEEE Trans.

[7] Shin, S.J., Jung, Park, Yoon, Silicon based ultra small multi switching SET operating at room temperature Appl. Physics., 97(10), (2010)

[8] Uchida, et. Al. Programmable SET logic for future low power intelligent LSI: proposal and room temperature operation, IEEE, Electron Devices 50(7), 1623-1630,(2003)

[9] Ionecu, S. Pott, Mahapatra, Hybrid SETMOS architecture with Coulomb blockade oscillations and high current drive, IEEE Electron devices Lett. 25(6), 411-413 (2004)

[10] Zhang, T. Kasai, Novel hybrid voltage controlled ring oscillators using SET and MOS transistor, IEEE, Nanotechnology 6(2), 170-175, 2007

[11] Shin, Yang, S. R. Takahashi, Room temperature charge stability modulated by quantum effects in a Nano scale silicon island, Nano letter 11(4), 1591-197(2011)