FPGA Implementation of OFDM Transceiver using Verilog - Hardware Description Language

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ABSTRACT
Orthogonal Frequency Division Multiplexing (OFDM) is a Frequency Division Multiplexing (FDM) technique used as a digital multi-carrier modulation method. A large number of closely spaced sub carriers which are orthogonal are used to carry data on several parallel data streams. OFDM uses the spectrum efficiently compared to Frequency Division Multiple Access (FDMA) by spacing the channels much closer and creating all the carriers orthogonal to one another. Orthogonality of the carriers prevents interference between the closely spaced carriers and provides high bandwidth efficiency. This work focuses on design and implementation of OFDM transmitter and receiver. Corresponding blocks of OFDM transmitter and receiver includes Quadrature Amplitude Modulation (QAM), Symbol Generator (SG), Zero Padding, Inverse Fast Fourier Transform (IFFT), Cyclic Prefix, Output Module, Inverse Cyclic Prefix, Fast Fourier Transform (FFT), Inverse Zero Padding, Inverse Symbol Generator and De-mapping block. 8-Point IFFT and 8-Point FFT with radix-2 algorithm is used for IFFT and FFT blocks. The design has been coded in VERILOG. To synthesize and simulate, Xilinx 12.2 tool with Modelsim6.3f simulator is used. The design of OFDM transceiver is implemented on Vertex 4 FPGA.

Keywords
Orthogonal Frequency Division Multiplexing (OFDM), Quadrature Amplitude Modulation (QAM), Inverse Fast Fourier Transform (IFFT),Fast Fourier Transform (FFT)

1. INTRODUCTION
Due to rapid growth of wireless and multimedia communication, there is a tremendous need for high-speed data transmission. Telecommunication industry provides variety of services ranging from voice to multimedia data transmissions, in which speed ranges several Kbps to Mbps. Existing system, may fail to support high speed efficient data transmission. To improve the speed and maximum amount of data transmission Orthogonal Frequency Division Multiplexing (OFDM) system may be used [1].

Orthogonal Frequency Division Multiplexing (OFDM) was first developed in the 1950's [2]. OFDM is a method of encoding digital data on to a numerous carrier frequencies. It has developed into a very popular scheme for wideband digital communication systems. Many researchers shown OFDM can be used in applications such as audio broadcasting [3], digital television [4], power line networks [5], wireless networks and 4G mobile communications [6].

In OFDM a large number of thoroughly spaced sub carriers are used to convey data on to several parallel data streams. Each sub carrier is modulated with modulation techniques such as Quadrature Amplitude Modulation (QAM), Quadrature Phase Shift Keying (QPSK) or Binary Phase Shift Keying (BPSK) at a lesser symbol rate.

In this paper implementation of OFDM transmitter and receiver on Vertex 4 FPGA is discussed. This work involves designing of 8-point IFFT and 8-point FFT blocks using radix-2 algorithm. Using these IFFT and FFT blocks, OFDM transmitter and receiver blocks are constructed.

Rest of the paper is organized as follows. In section 2 related work is discussed. In section 3 overview of OFDM is discussed. OFDM transmitter and OFDM receiver details are given in section 4 and 5 respectively. Implementation and simulation results are discussed in section 6. Conclusion and future work is mentioned in section 7.

2. RELATED WORK
Many researchers were contributed their work towards FPGA implementation of Orthogonal Frequency Division Multiplexing (OFDM) transceiver. In [1] designing of OFDM system was performed using VHDL. They used radix-2 8-Point Decimation In Frequency (DIF) IFFT/FFT blocks. In [2] various design parameters of OFDM system was performed using Matlab. They implemented OFDM transceiver on Spartan 3A kit using VHDL programming language. In [8]designing of OFDM Transmitter and Receiver was performed using Quartus II tool. Altera Modelsim was used for simulation and every component of OFDM Transceiver was designed using Verilog. In [12] designing of OFDM system was performed using Verilog with radix-2 8-Point Decimation In Frequency (DIF) FFT and IFFT. In [13] designing of OFDM system was performed using VHDL and Xilinx's Chip scope tool was used for validating results on Spartan 3E kit. In [14] OFDM system was implemented on Virtex-2using Xilinx ISE 10.1.In [15]designing of OFDM system was performed using VHDL and Xilinx's Chip scope tool is used for verifying the results on Spartan 3E kit. In [17] designing of OFDM system was implemented using Xilinx on Spartan-3 FPGA. In this work FFT/IFFT module was implemented using CORDIC algorithms as an alternate for multipliers. In [18] 16 bit Quadrature Amplitude Modulation (QAM)was simulated using simulink and VHDL code was generated using system generator tool.

This work focused on designing core processing blocks of OFDM transmitter and receiver. Design has been coded in VERILOG. Timing simulation is analyzed using Xilinx ISE

12.2 and modelsim 6.3f. Design of OFDM transceiver is synthesized and it is implemented on Vertex 4 FPGA.

3. OVERVIEW OF OFDM

Orthogonal Frequency Division Multiplexing (OFDM) is a modulation scheme having multicarrier transmission technique [7]. In OFDM, spectrum is divided into abundant carriers each one being modulated at lower data rates. Fig.1 shows spectrum of Frequency Division Multiplexing (FDM). In FDM subcarriers are non-overlapping, hence requires more bandwidth. Fig.2 shows spectrum of OFDM overlapping subcarriers. Saving of bandwidth in OFDM is shown in Fig.2. OFDM is analogous to FDM but much more spectrally effective by positioning the sub-channels much closer together. This is done by selecting the frequencies that are orthogonal and by letting the spectrum of each sub channel to overlay another without interfering with it. Fig.3 shows spectrum overlap in OFDM. It is observed from Fig.3 that, at any instance only main lobe of one signal is high and all lobes of other signals are zero. Hence necessary band width is significantly reduced by removing guard bands and this allows signals to overlap [7].

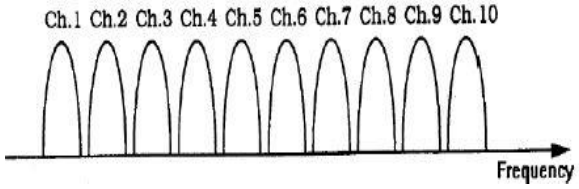

Fig.1 Spectrum of FDM non-overlapping subcarriers [7]

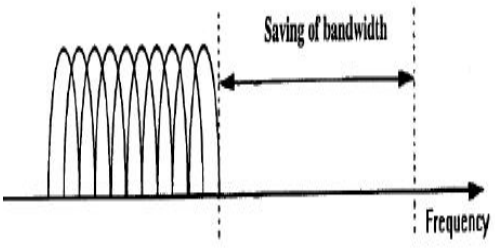

Fig.2 Spectrum of OFDM overlapping subcarriers [7]

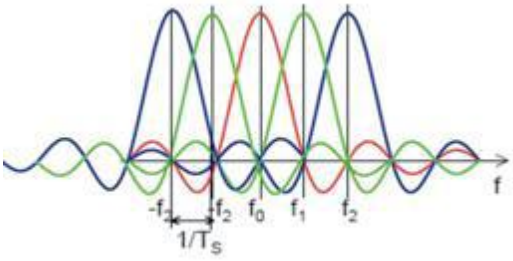

Fig.3 Spectrum overlap in OFDM [7]

4. OFDM TRANSMITTER

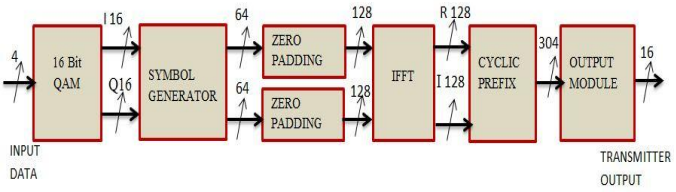

Fig.4 Block diagram of OFDM transmitter

Fig. 4 shows the block diagram of OFDM transmitter. OFDM transmitter generates a modulated data. It consists of blocks such as, 16 bit QAM, symbol generator, zero padding, IFFT, cyclic prefix and output module blocks. Input to the QAM is 4 bit binary data. The output of QAM consists of 16 bit In-phase and quadrature components. Output of QAM is given to the symbol generator. Symbol generator gives a 64 bit output by concatenating each component of QAM output by four times. The output of symbol generator is given to zero padding block. At zero padding block 32 bits of zeros are added at the beginning and at the end of the symbol generator output, which gives 128 bit output. Inverse Fast Fourier Transform [IIFT] converts a spectrum consisting of both amplitude and phase of each component in frequency domain to a time domain signal. 8-point 16 bit radix 2 IFFT is used. In this work two IFFT modules, one for the real component and the other for the imaginary component is used. The output of IFFT is given to cyclic prefix block. The word cyclic prefix refers to the preceding of symbol with a replication of the end. It serves as a guard interval, which eliminates inter-symbol interference from previous symbol. Cyclic prefix is frequently used in coincidence with modulation in order to recollect sinusoid properties in multipath channels. The output of cyclic prefix block is given to output module block. The purpose of output module block is to have a 16 bit data as the OFDM transmitter output. Individual blocks of OFDM transmitter are discussed below.

4.1 Quadrature Amplitude Modulation (QAM)

Quadrature Amplitude Modulation can be used as both an analog and digital modulation technique. It is a mixture of Amplitude Shift Keying (ASK) and Phase Shift Keying (PSK).

In this work 16-bit QAM is used as digital modulation technique. The block diagram of 16-bit QAM is given in Fig.5

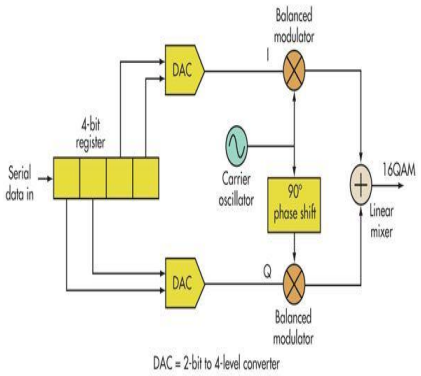

Fig.5 Block diagram of 16-bit QAM [9]

The block diagram of 16-bit QAM consists of 4 bit register, Digital to Analog converter (DAC), phase shifter with an angle 90̊, carrier oscillator, balanced modulator and linear mixer. Input to the 16-bit QAM is four bit binary data, which is stored in 4 bit register. Out of 4 bits of data 2 bits are given DAC and other 2 bits to another DAC block. The DAC block converts binary input data into analog signal. The analog output of two DAC's is given to two balanced modulators.

Carrier oscillator generates a signal that is given to top balanced modulator. The same signal is 90̊ phase shifted and is given to bottom balanced modulator. Output of top and bottom balanced modulator is added at the Linear Mixer. The equation of 16 bit QAM carrier wave is given in equation (1)

$$S(t)=x(t).\cos(2\pi ft) - y(t).\sin(2\pi ft) \quad (1)$$

Where x(t) and y(t) represent the In-phase (I) and Quadrature (Q) axis respectively. This clearly shows that the amplitude of the signal varies with time as bits are modulated onto it. It is also apparent that the phase also changes with time.

4.2 Constellation of 16 bit Quadrature Amplitude Modulation (QAM)

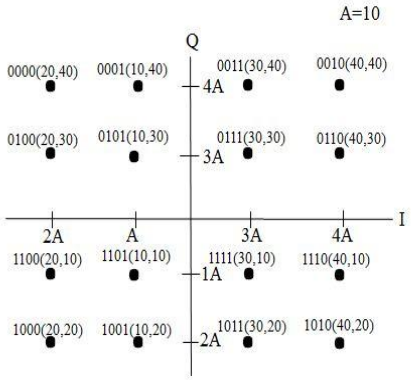

Fig.6 Constellation diagram of 16-bit QAM

16 bit QAM has 16 possible states. It gets 16 states by using 12 different phases and 3 different amplitudes of modulation. Constellation diagram of 16-bit QAM is shown in Fig.6. This diagram has 4 levels per dimension. This means that there are 4 Imaginary and 4 Quadrature values. Since 2^4= 16, there are 4 bits to represent each state. So bit rate is 4 bits per cycle. 16 QAM is also represented as 4 baud. In Table.1 various input combinations and their corresponding output combinations are listed.

4.3 Symbol generator

It is used to concatenate 16 bits of data 4 times to make 64 bit data. In this 8-point IFFT, every point consists of 16 bit data is used. Hence the output of QAM is concatenate 4 times.

4.4 Zero padding

It is used to make 64 bit data to 128 bit. Since 8-point IFFT, every point consists of 16 bit data is used. A total of 128 bit is required as input to IFFT block. Hence 32 bit of zero's are added at the beginning and at the end of 64 bit symbol generator output. Zero padding doesn't change the Fourier transform it only changes the density of the samples of DFT. It increases density of the samples. Fast calculations are the main reason for zero padding.

4.5 Inverse Fast Fourier Transform [IIFT]

It transforms a spectrum of both amplitude and phase of each component in frequency domain to a time domain signal. In this work 8-point 16 bit IFFT is used. Fig. 7 shows butterfly diagram of 8-point IFFT using radix-2 algorithm. In this work two IFFT modules are used for transforming frequency domain constrains to time domain constrains.

The basic equation of IFFT is given in equation (2)

$$x(n) = \frac{1}{N}\sum_{n=0}^{N-1} X(K)e^{-\frac{j2\pi n}{N}} \quad (2)$$

Where $n = 0, 1, 2, \dots, N-1$

The inherent properties of FFT/IFFT in an OFDM system make the symbol orthogonal. In OFDM transmitter the input symbols (N symbols) are considered to be in frequency domain and IFFT is applied on N symbols.

Table.1 16 bit QAM output combinations

Sl. No	Combinations	Output (In phase, Quadrature)
1	0000	(20,40)
2	0001	(10,40)
3	0010	(40,40)
4	0011	(30,40)
5	0100	(20,30)
6	0101	(10,30)
7	0110	(40,30)
8	0111	(30,30)
9	1000	(20,20)
10	1001	(10,20)
11	1010	(40,20)
12	1011	(30,20)
13	1100	(20,10)
14	1101	(10,10)
15	1110	(40,10)
16	1111	(30,10)

4.6 Cyclic prefix

The word cyclic prefix refers to the preceding of a symbol with a replication at the end. It serves as a guard interval which eliminates inter-symbol interference from previous symbol. Cyclic prefix is frequently used in coincidence with modulation in order to recollect sinusoid properties in multipath channels.

5. OFDM RECEIVER

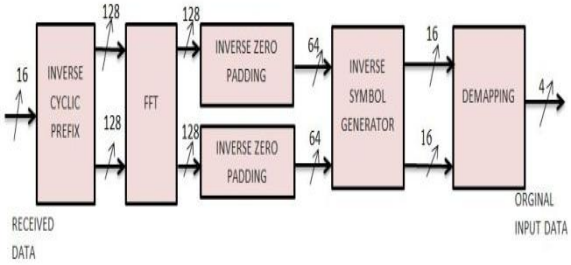

Fig.7 Block diagram of OFDM receiver

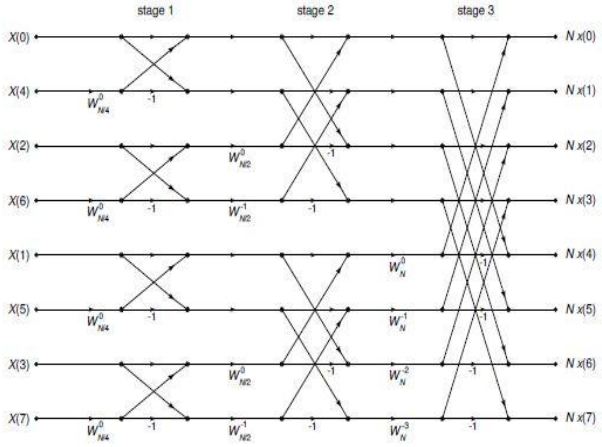

Fig.8 8-point IFFT [10]

Fig. 8 shows block diagram of OFDM receiver. OFDM receiver regenerates original input data from modulated output of OFDM transmitter. OFDM receiver includes Inverse Cyclic Prefix, Fast Fourier Transform (FFT), Inverse Zero Padding, Inverse Symbol Generator and De mapping block. Individual blocks of OFDM receiver are discussed below.

5.1 Inverse cyclic prefix

This block is used to remove prefixed data bits that are used at the transmitter. In this block 48 bits are removed which were appended during transmission.

5.2 Fast Fourier Transform [FFT]

It converts time domain constraints to frequency domain constraints. Here 8-point radix 2 FFT is used. Each path consists of 16 bit data and a total of 128 bits are given as input to FFT block.

The basic equation for FFT is given in equation (3)

$$X(K) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi kn}{N}} \qquad (3)$$

Where $k = 0, 1, 2, \ldots, N-1$

The butterfly diagram of 8 point FFT is shown in Fig. 9

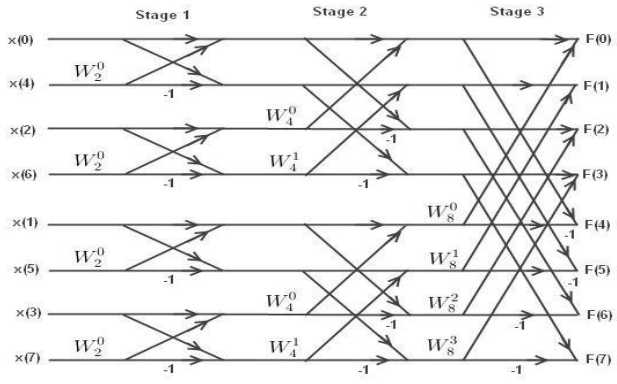

Fig.9 Butterfly diagram of 8-Point FFT [2]

5.3 Inverse Zero Padding

32 bits of Zeros are added at the beginning and at the end of each component of symbol generator output at the transmitter. In this block a total of 64 bits are removed which were used during transmission.

5.4 Inverse Symbol Generator

It converts 64 bit data to a 16 bit data.16 bits output of QAM is concatenated 4 times in order to make 64 bits at symbol generator of OFDM transmitter. In this block 48 bits are removed which were used during transmission.

5.5 De-mapping

It is used to regenerate original 4 bit input data signal from 16 bit data. In this 16 bit QAM demodulator is used.4 bits of original input data is regenerated from 16 bit output of Inverse symbol generator block.

6. IMPLEMENTATION RESULTS

In this work OFDM transmitter and receiver is simulated and implemented on Vertex 4 (xc4vlx15) device. To synthesize and simulate Xilinx 12.2 software with Modelsim 6.3f simulator is used. To analyze the modules, different inputs are considered.

6.1 OFDM transmitter

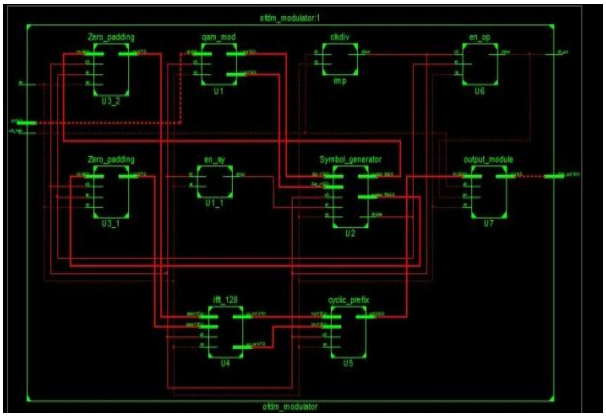

Fig.10 RTL schematic view of OFDM transmitter

Fig. 10 shows RTL schematic of OFDM transmitter. It is observed in the figure that RTL schematic includes various blocks. All these blocks are connected as follows. 4 bit binary input is given to Quadrature Amplitude Modulation (QAM)

block. Real and Imaginary components of QAM is given to Symbol generator block. Output of Symbol generator is given to two Zero padding blocks, one for real and other for imaginary. Output of Zero padding blocks is given to two Inverse Fast Fourier Transform (IFFT) blocks. Output of IFFT is given to cyclic prefix block. Output of Cyclic prefix is given to output module. Output of output module is a 16 bit binary data and it is transmitter output.

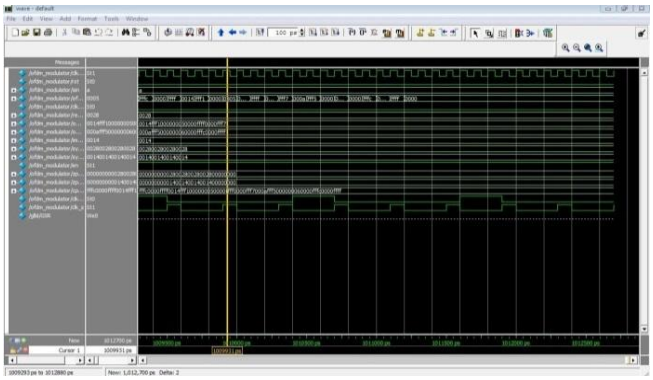

Fig.11 Simulation result of OFDM transmitter

Fig. 11 shows output of OFDM transmitter. If clock=0, reset=0 or 1, output of various blocks of OFDM transmitter will be zero. Various blocks of OFDM transmitter produces a value only when clock is high and reset is 0. 4 bit binary input is given to QAM. Input value considered here is 1010 (Hexadecimal a). The output of QAM consists of 16 bit In-phase and Quadrature components. Output of QAM is given to the Symbol generator. Symbol generator gives a 64 bit output by copying each component of QAM output by four times. The output of symbol generator is given to Zero Padding block. At zero padding block 32 bits of Zeros are added at the beginning and at the end of the Symbol generator output, which gives 128 bit output. Output of Zero padding is given to I IIFT block. Output of IFFT is 128 bits of real and imaginary components and it is given to Cyclic Prefix block. Output of cyclic prefix block is of 304 bits and it is given to Output module block. The purpose of output module block is to have a 16 bit data as the OFDM transmitter output.

6.2 OFDM receiver

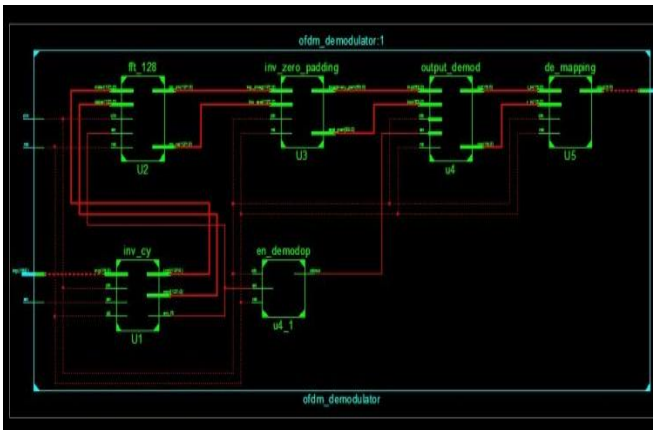

Fig.12 RTL schematic view of OFDM receiver

Fig. 12 shows RTL schematic of OFDM Receiver. It is observed in the figure that RTL schematic includes various blocks. All these blocks are connected as follows. OFDM Transmitter output is given to Inverse Cyclic prefix block. Output of Inverse Cyclic prefix block is given to Fast Fourier Transform (FFT) block. Output of FFT is given to Inverse Zero padding blocks. Output of Inverse Zero padding blocks is given to Inverse Symbol generator. Output of Inverse Symbol generator is given to De mapping block. Original input data is recovered at De mapping block.

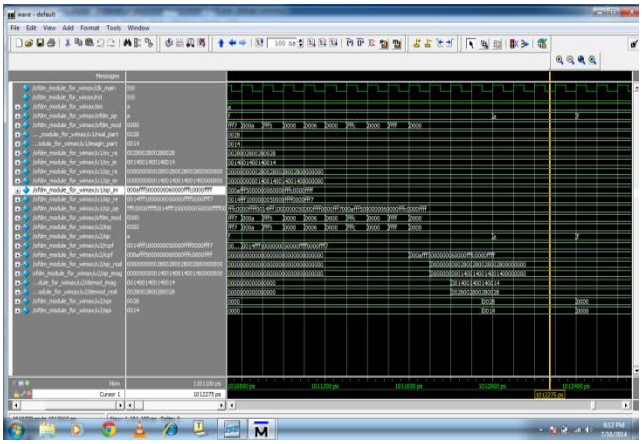

Fig.13 Simulation result of OFDM receiver

Fig. 13 shows output of OFDM Receiver. If clock=0, reset=0 or 1, output of various blocks of OFDM receiver will be zero. Various blocks of OFDM receiver produces a value only when clock is high and reset is 0. OFDM Transmitter output is given to Inverse Cyclic prefix block. At Inverse Cyclic prefix block, those bits which are added at the transmitter are removed. Output of Inverse Cyclic prefix block consists of 128 bits of data. These 128 bits are given to FFT block. It converts time domain constraints to frequency domain constraints. Output of FFT is given to Inverse Zero padding block. This block is used to remove zero's that are added at the transmitter and it consists of 64 bits of data. These 64 bits are given to Inverse Symbol Generator. It converts 64 bit data to a 16 bit data. Extra 48 bits are removed at this stage. 16 bit data is given to De mapping block. At this block original input data is recovered. Input 1010 is given at transmitter and it is recovered at receiver as shown in Fig. 13.

Table 2 Device utilization of Vertex 4 FPGA

Logic Utilization	Used	Available	Utilization
Number of slices	1428	3584	39%
Number of slice flip flops	1149	7168	16%
Number of 4 input LUTs	2259	7168	31%
Number of bonded IOBs	23	141	16%
Number of MULT 18×18s	8	16	50%
Number of GCLKs	3	8	37%

In table 2 various logic block utilization of Vertex 4 FPGA kit are shown. It is observed that design consumes very low devices.

7. CONCLUSION

In this work OFDM system is designed and implemented on Vertex 4 FPGA using Verilog. 8 point radix 2 IFFT and FFT are designed and used at transmitter and receiver respectively. Maximum frequency of the designed system is 494.841MHz.Maximum frequency of OFDM system can be increased by using radix-4 algorithm for IFFT and FFT. Further OFDM transceiver can be implemented using ASIC methodology.

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