Review of Mesh Topology of NoC Architecture using Source Routing Algorithms

Vaishali V. Ingle
PG. Student, MTech (ELECTRONICS)
B.D.C.O.E, Sevagram,
India.

Mahendra A.Gaikwad, Ph.D.
Prof. &Head, Dept.of EXTC
B.D.C.O.E, Sevagram,
India

ABSTRACT

NoC is efficient on-chip communication architecture for SoC architectures. It enables integration of a large number of computational and storage blocks on a single chip. NoCs have tackled the SoCs many disadvantages and are structured, reusable, scalable, and have high performance. Lots of topologies have been proposed for NoCs. Among these topologies, mesh topology has gained more consideration by designers due to its simplicity. A 2D-mesh topology is one of the most frequently mentioned topologies for an NoC design due to its natural layout mapping onto an SoC. Thus, the 2D mesh network on chip (NoC) is a popular NoC topology because of network scalability and the use of a simple routing algorithm. In this paper, we compare popular mesh with the other NoC topologies in terms of different performance metrics such as, latency, power consumption, and power/throughput ratio under different routing algorithms.

Keywords

Noc, mesh topology, routing algorithm, latency, throughput.

I. INTRODUCTION

A variety of interconnection schemes are currently in use, including crossbar buses and NOCs. Of these, later two are dominant in research community. However buses suffer from poor scalability because as the number of processing elements increases, performance degrades dramatically. Hence they are not considered where processing elements are more. To overcome this limitation attention has shifted to packet-based on-chip communication networks, known as Network-On-Chip (NOC). NoC improves the scalability of SoCs (System-on-Chip), and the power efficiency of complex SoCs compared to other designs. Network-on-Chip (NoC) is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. In a NoC system, modules such as processor cores, memories and specialized IP blocks exchange data using a network.

The Network-on-Chip (NoC) concept has been proposed to replace conventional bus-based system architectures to create scalable and flexible future SoC designs. NoC is a regular and predictable infrastructure having well defined interfaces.NOC is having a layered structure, where packet based communication using router is done. Topology and routing algorithm are two important features which distinguish various NoC platforms.

II. NETWORK TOPOLOGY

The topology of a NoC specifies the physical organization of the interconnection network. It defines how nodes, switches and links are connected to each other. Topology for NoCs can be classified into two broad categories: 1) direct network topologies, in which each node (switch) is connected to at least one core (IP), and 2) indirect network topologies, in which we have a subset of switches (nodes) not connected to any core (IP) and performing only network operation. 2D mesh is most popular topology in which all links have the same length it eases physical design and area grows linearly with the number of nodes. It must be designed in such a way as to avoid traffic accumulating in the center of the mesh. The size of topology can be specified in terms of number of rows and columns.

The Network Topology refers to the static arrangement of channels and nodes in the network. It is good if it allows to satisfy the requirements of the traffic at reasonable costs. In NoCs there are many types of proposed topologies, so far, such as Mesh, Torus, Star, Octagon, and SPIN. In this paper, we are comparing the most commonly used Mesh Topology under Source Routing.
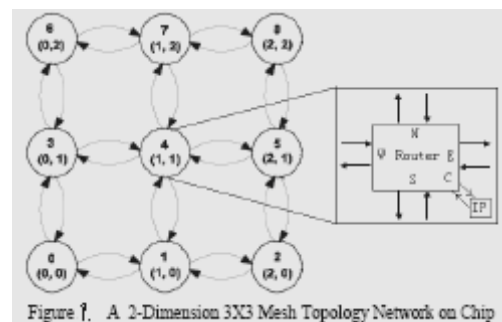

Figure 1. A 2-Dimension 3X3 Mesh Topology Network on Chip

In the Fig. 1, each circle represents a tile in the network. Each tile consists of an IP core connected to a router by a bidirectional core channel (C). A tile is connected to neighbor tiles by four bidirectional channels (N, E, S and W). Each tile is identified by a unique integer ID. Also, each tile can be identified by a pair x-coordinate and y-coordinate. Our 2-Dimesion 3X3 mesh topology NoC is designed using wormhole switching mechanism, in which packets are divided into flits. A packet consists of 3 types of flits, which are head flit, data flit and tail flit. All the three routing algorithms, XY routing algorithm, OE routing algorithm and DyAD routing algorithms are based on these characteristics.

III. ROUTING ALGORITHM

Routing algorithms significantly affect the performance of a NoC. Most of the existing NoC architectural proposals advocate distributed routing algorithms for building NoC platforms. Although source routing offers many advantages, researchers avoided it due to its apparent disadvantage of larger header size requirement that results in lower bandwidth utilization. In this paper we make a strong case for the use of source routing for NoCs, especially for platforms with small sizes and regular topologies like Mesh.

Communication performance of a NoC depends heavily on the routing algorithm used. According to where routing decisions are taken, it is possible to classify the routing as source and distributed routing [10].

Routing algorithm can be classified on the basis of adaptivity such as deterministic or adaptive. In deterministic routing, the path from the source to the destination is pre-computed and provided in the packet header. In distributed routing, the header contains destination address only and the path is computed dynamically by participation of routers on the way to the destination. [7].In this paper, advantages of source routing for mesh topology is applied as in path information can be efficiently encoded with small number of bits. It can be easily shown that two bits are sufficient to encode every hop in the path. Since the packet entering a router contains the pre-computed decision about the output port, the router design is significantly simplified. Since only a few bits of the header are used in every router, its design is not only simple but is also independent of the network size. It seems that the advantages more than compensate its disadvantages.

A. *XY Routing Algorithm*

The XY routing algorithm is one kind of distributed deterministic routing algorithms. For a 2-Dimesion mesh topology NoC, each router can be identified by its coordinate (x, y) (Fig. 1). The XY routing algorithm compares the current router address (C_x, C_y) to the destination router address (D_x, D_y) of the packet, stored in the header flit. Flits must be routed to the core port of the router when the (C_x, C_y) address of the current router is equal to the (D_x, D_y) address. If this is not the case, the D_x address is firstly compared to the C_x (horizontal) address. Flits will be routed to the East port when $C_x<D_x$, to West when $C_x>D_x$ and if $C_x=D_x$ the header flit is already horizontally aligned. If this last condition is true, the D_y (vertical) address is compared to the C_y address. Flits will be routed to South when $C_Y<D_y$, to North when $C_y>D_y$. If the chosen port is busy, the header flit as well as all subsequent flits of this packet will be blocked. The routing request for this packet will remain active until a connection is established in some future execution of the procedure in this router.

The implementing of XY routing algorithm is simple.

However, it is deterministic routing algorithm, which means that, this routing algorithm only provides a routing

path for a pair of source and destination. Moreover, XY routing algorithm cannot avoid from deadlock appearance.

B. *OE Routing Algorithm*

OE routing algorithm is a distributed adaptive routing algorithm which is based on odd-even turn model. It exerts some restrictions, for avoiding and preventing from deadlock appearance. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels. Explaining some definitions are necessary in order to represent this algorithm. In a two-dimension mesh with dimensions X*Y each node is identified by its coordinate (x, y). In this model, a column is called even if its x dimension element is even numerical column. Also, a column is called odd if its x dimension element is an odd number. A turn involves a 90-degree change of traveling direction. A turn is a 90-degree turn in the following description. There are eight types of turns, according to the traveling directions of the associated channels. A turn is called an ES turn if it involves a change of direction from East to South. Similarly, we can define the other seven types of turns, namely EN, WS, WN, SE, SW, NE, and NW turns, where E, W, S, and N indicate

East, West, South, and North, respectively. As a whole, there are two main theorems in odd-even algorithm:

Theorem1: NO packet is permitted to do EN turn in each node which is located on an even column. Also, No packet is permitted to do NW turn in each node that is located on an odd column.

Theorem 2: NO packet is permitted to do ES turn in each node that is in an even column. Also, no packet is permitted to do SW turn in each node this is in an odd column.

OE routing algorithm is more complex than XY routing algorithm. However, it is one kind of adaptive routing algorithm. For a pair of source and destination, it can provide a group of routing paths and it can prevent from dead lock appearance [15].

IV. LITERATURE REVIEW

Wang Zhang et.al. In this paper, it has been demonstrated that the two routing algorithms in details at first. XY routing algorithm and OE routing algorithm which are then simulated and compared based on a 3X3 mesh topology NoC with NIRGAM simulator. The simulation results show that OE routing algorithm, whose P parameter equals to 1.09, increases P parameter greatly as compared to XY routing algorithm, whose P parameter equals to 0.86, in a 2-dimension 3X3 mesh topology NoC, with Constant Bit Rate (CBR) traffic condition of each tail In the above context *P* parameter refers to an average performance parameter to evaluate the average performance of different routing algorithm: i.e.

P= Average Throughput of Network/ Average Latency per packet of Network. If value of parameter P is larger, the performance will be better. Thus, it has been observed that OE routing algorithm fits with their NoC better than XY routing algorithm with CBR traffic condition. The Authors, on the basis of their analysis shows that the latency of OE routing algorithm is shorter than that of XY routing algorithm. Meanwhile, the throughput of OE routing algorithm is larger than that of XY routing algorithm. But their conclusions are just fit for a 2-Dimension 3X3 mesh topology NoC. For other topologies, additional researchers are needed to do in the future [2].

Saad Mubeen, et.al. In this paper, source routing has been used for NoCs, especially for platforms with small sizes and regular topologies, Mesh. Because of the small and fixed size of practical NoCs, the overhead of source routing is negligible and it is easily compensated by a large number of its advantages, including lower router cost and higher communication speed of the router. It has been demonstrated through simulation based evaluation that source routing has a

potential of achieving higher latency and throughput performance, for example up to 28% lower latency even at medium load , as compared to distributed routing[13].

Krishan Kumar Paliwal, et.al.In this paper, a novel scheme is presented which compares and evaluates the performance of guaranteed throughput and best effort traffic in Network on-Chip under different synthetic traffic generators and highlights its dependence in terms of latency on the type of traffic patterns and on the topology selection (mesh and torus) of Network on Chip. It also explores the effect of various routing function on latency of GT and BE traffic for mesh topology. This paper presented a comparison of QoS for both GT and BE for mesh and torus topologies under different traffic scenarios and showed that there is a significant improvement in average latency for both types of traffic classes in torus topology over mesh topology. It is also concluded that transpose traffic in mesh topology the

valiant routing function is one which has least average latency for both GT as well as BE traffic [14].

Mikael Milberg, et.al. In this paper, Forced Requeue is to prematurely lift out low priority packets from the network and requeue them outside using priority queues. In this paper it studies the Forced Requeuing on a mesh with varying burst sizes and traffic scenarios, Priority Based Forced Requeue (PBFR) have been introduced to decrease worst-case latencies in NoCs offering best effort services. In this paper, deflective routing based on NoC Nostrum has been discussed. On the basis of simulation data it claims that there are no performance degrading penalties related to the use of PBFR.But, it causes an extra cost in hardware and an implementation based on shift registers is proposed. From the simulation observation; using the PBFR approach reduces the worst-case latencies by 50% while still when the same numbers of buffers are used. This has been demonstrated both for a uniform traffic pattern as well as for a traffic pattern constructed to create hot-spots in the centre of the NoC[1].

Pan Hao, et.al. In this paper, some research has been done on XY and OE routing algorithms based on mesh topology by using NIRGAM emulator. The result shows that the ratio of throughput rate and package time delay is 2.5358 in OE routing algorithm, which seems to be larger than 2.1126 in XY routing algorithm and it proves that the OE routing algorithm is better to Mesh topology than XY routing algorithm. The ratio of average throughput and average packet delay is used to show whether the algorithm is good or bad. The larger the ratio, the better the performance [19].

Lalit Kishore Arora, et.al. In this paper, a simulation framework for mesh interconnection network has been designed. To evaluate the interconnection topology, data loss has been the measure performance parameter. The packet loss was analyzed during the fault in mesh interconnection network topology with source routing using network simulator NS2. The designed framework has considered two parameters packet size and packet generation interval and also used both with and without acknowledgement transmission evaluating the performance of mesh interconnection topology. It is found that when the above mentioned two parameters are changing the ratio of packet loss is constant in cases where traffic generator has used acknowledgement mechanism.

But when acknowledgement mechanism is added it has been found that there was no packet loss in the both cases. Therefore it claims that the mesh network with the traffic agent which uses acknowledgement mechanism is more reliable; except that the delay of transmission due to the link down occurs [10].

Another paper, about the performance evaluation on the basis of packet loss in Mesh interconnection with source routing using different traffic generation mechanisms for parallel transmissions with handshaking concept. On the experimental basis 2D Mesh of size 4x4 was evaluated, and compared the performance of FTP mechanism with the constant bit rate mechanism for parallel transmission. It was found that the FTP mechanism has not lost any packet while constant bit rate mechanism had lost few packets in parallel transmission. Also it adds, if the time of the simulation window was increased from 5 seconds to 6 seconds, in the constant bit rate mechanism, no loss would be found but delay occurs. Therefore, it suggests, FTP mechanism as most secure and reliable when parallel transmission is considered with handshaking concept in the Mesh interconnection networks [17].

Parag Parandkar, et.al. In this paper, based on a 2-Dimension 3x3 mesh topology NoC, three different routing algorithms, XY routing algorithm, OE routing algorithm and DyAD routing algorithm are simulated on NIRGAM simulator platform and impact of Percentage Load variation is compared with four different parameters namely overall average latency per channel per packet, overall average latency per channel per flit, overall average latency per flit and overall network power respectively. Communication performance of a NOC heavily depends on routing algorithm. XY routing algorithm is distributed deterministic routing algorithm. Odd-Even (OE) routing algorithm is distributed adaptive routing algorithm with deadlock-free ability. DyAD combines the advantages of both deterministic and adaptive routing schemes. Key metrics which determines best performance for routing algorithms for Network-on-Chip architectures are Minimum Latency, Minimum Power and Maximum Throughput. We demonstrated the impact of traffic load variations on average latency and total network power for three routing algorithms XY, OE and DyAD on a 3x3 2-dimensional mesh topology. It has been found on the basis of the simulation results reveals that the DyAD dominates the XY and OE algorithms as it has depicted the minimum values of overall average latency per channel (in clock cycles per flit) as 1.58871, overall average latency per channel (in clock cycles per packet) as 9.53226, overall average latency (in clock cycles per flit) as 26.105, and total network power as 0.1771 milliwatts, achieved for DyAD routing algorithm [20].

Mubeen .S, et.al. In this paper, source routing for NoCs has been especially used for regular topologies like mesh. A method to compute paths for various communications has been proposed in such a way that traffic congestion can be avoided while ensuring deadlock free routing. The path which was computed may not be the best in terms of link load distribution; therefore an iterative algorithm to improve the computed path for application specific source routing has been proposed.. After analysis and selection of routing algorithm, initial paths are computed for all communications. But in second step when link load variance was estimated, two possibilities arised- first if the load distributed was small then the paths which was computed in the first step are used for source routing. Otherwise, secondly,if link load distribution was not acceptable then the most congested link was identified. One communication using this link was rerouted on an alternative path using the adaptivity of the routing algorithm. The above process was iteratively repeated until link load distribution became acceptable or it doesn't not shows any further improvement[21] .

M. Mirza-Aghatabar, et.al. In this paper, two popular NoC topologies, i.e., mesh and torus, in terms of different figures of merit e.g., latency, power consumption, and power/throughput ratio under different routing algorithms and two common traffic models, uniform and hotspot are compared. The main problem with the mesh topology is its long diameter that has negative effect on communication latency. Torus topology was proposed to reduce the latency of mesh and keep its simplicity .The only difference between torus and mesh topology is that the switches on the edges are connected to the switches on the opposite edges through wrap-around channels. Although the torus architecture reduces the network diameter, the long wrap-around connections may result in excessive delay which can be avoided by folding the torus. Due to importance of these two topologies, i.e., mesh and torus, we compare the performance and power consumption of these NoC

topologies under different routing algorithms. So, XY routing as an example of deterministic, Odd-Even and Negative First Turn models as examples of partially adaptive and Duato as an example of fully adaptive routing algorithms are used. These examples were chosen because they are all deadlock-free and incur minimal hardware cost. PP, P/T and S factors are used as three different functions to select the best routing algorithm for each topology under uniform and hotspot 14% traffic models with the least number of virtual channels to be deadlock-free. In all, it was found that when latency is a constraining criterion, it is better to use the torus topology and when power consumption is a constraining criterion, it is better to use the mesh topology. Thus from the above data it shows torus always has better latency than mesh. However the cost to pay for this improvement is higher power consumption.[22]

V. OBSERVATION

Reviewing the Literature, we identified that a large number of Routing Algorithm have been proposed in literature. Source Routing has not been so far considered for NoCs, due to its apparent large overhead. Therefore, we observed the performance and simulation of Source Routing algorithm for 2D mesh topology of Network-on-chip architecture. Performance is to be measured in terms of Latency and Throughput. In short, we found the overall data that we got from the above references and we summarized it as follows

Table 1. Comparative Study Summary

Data	[1]	[2]	[19]	[20]
Simulator	Nostrum	NIRGAM	NIRGAM	NIRGAM
Findings	Using PBFR reduces worst-case latencies by 50%	P for OE=1.09 And XY=0.86 With CBR traffic	Ratio of Throughput rate and package time delay for OE=2.5358 And XY=2.1126	Overall average Latency OE=1.89 XY=1.90 Dy AD= 1.58

P= Average Throughput of Network/ Average Latency per packet of Network.

VI. CONCLUSION

In this paper we studied the different Research papers in context with the Performance of Mesh Topology of NoC Architecture using Source Routing Algorithm. It has been observed that Topology and routing algorithm are two important features which distinguish various NoC platforms. A 2D-mesh topology is one of the most frequently mentioned topologies for an NoC design due to its natural layout mapping onto an SoC. Thus, the 2D mesh network on chip (NoC) is a popular NoC topology because of network Scalability and the use of a simple routing algorithm. In this paper, we compare popular mesh with the other NoC topologies in terms of different Performance metrics.

REFERENCES

[1] Mikael Milberg et.al.,"Priority Based Forced Requeue to Reduce Worst-Case Latencies for Bursty Traffic" Proceedings of the Conference on Design, Automation and Test in Europe 2009 Pages 1070-1075

[2] Wang Zhang et.al.,"Comparison Research between XY and Odd-Even Routing Algorithm of a 2-Dimension 3x3 mesh Topology Network –on –Chip" 2009 IEEE computer society

[3] Naveen Choudhary,"*Bursty Communication Performance Analysis of Network-on-Chip with Diverse Traffic Permutations*" International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-6, January 2012

[4] Jan Ho Bahn et.al.,"On Design and Analysis of a Feasible Network-on -Chip(NoC) Architecture"2007 International Conference on Digital Object Identifier

[5] Chuggani R et.al."Traffic Model for Concurrent Core Task in Network on Chip" IEEE 2011.pages:205-210

[6] NIRGAM Manual: A Simulator for NoC Interconnect Routing and application Modeling Version 1.1

[7] Saad Mubeen, "Evaluation of source routing for mesh topology network on chip platforms", Master of Science Thesis, 2009.

[8] Dally W.J et.al. "Route packets, not wires: on-chip interconnection networks", in Design Automation Conference, Las Vegas, Nevada, USA, 2001, pp. 684-689.

[9] Dally W.J. and Towles B., "Principles and Practices of Interconnection Networks", Morgan Kaufmann Publishers an Imprint of Elsevier Inc, 2004.

[10] [Lalit Kishore Arora, et.al. *"Simulation and Analysis of Packet loss in Mesh Interconnection Networks"*, IJARCSSE Proceedings on (DRISTI 2012), DRISTI (1):35 - 38, April 2012. ISB

[11] Axel Jantsch et.al. *"Networks on Chip", Kluwer Academic Publishers*. 2003.

[12] Kavaldjiev N et. al. *"Routing of guaranteed throughput traffic in a network-on-chip"*. Available at: http://doc.utwente.nl/54538/.

[13] Mubeen,S.,et.al," Designing Efficient Source Routing for Mesh Topology Network on Chip Platforms" IEEE 2010Page(s): 181 - 188

[14] Paliwal, K.K.; et.al."Performance Analysis of Guaranteed Throughput and Best Effort Traffic in

Network-on-Chip under Different Traffic Scenario."IEEE 2009, Page(s): 74 - 78

[15] Wang Zhang "The Buffer Depth Analysis of 2-Dimension Mesh Topology Network-on-Chip with Odd-Even Routing Algorithm." IEEE 2009 Page(s): 1 - 4

[16] A.Hemani, et.al, "Network on a chip: an architecture for billion transistor era,"Proc. IEEE NorChip, 2000.

[17] Lalit Kishore Arora, et.al." *Performance Evaluation of mesh with source routing for Packet Loss.*" IJ ARCSSET Volume-1, Issue-5, August 2012

[18] Benini L., Micheli G.D., "Networks on chips: a new SoC paradigm".IEEE Computer Society, 2002.

[19] Pan Hao, et.al."Comparison of 2D MESH Routing Algorithm in NoC." IEEE 2011

[20] Parag Parandkar, et.al." *Performance Comparison of XY, OE and DY Ad Routing Algorithm by Load Variation Analysis of 2-Dimensional Mesh Topology Based Network-on-Chip."*BVICAM's International Journal of Information Technology,@Jan2012

[21] Saad Mubeen, et.al. "*On Source Routing for Mesh Topology Network on Chip."* 9th Swedish SoC Conference, Swedish Chapter of IEEE SSCS

[22] Mirza-Aghatabar, et.al. "An Empirical Investigation of Mesh and Torus NoC Topologies Under Different Routing Algorithms and Traffic Models ." IEEE 2007,Pages: 19-26.