A Comparative Study of Different Topologies for Network-On-Chip Architecture

Sonal S. Bhople
M-tech(II year) Electronics
B.D.C.E. Sewargram, Wardha(M.S.)

M. A. Gaikwad, Ph.D
Department Of Electronics
B.D.C.E. Sewagram, Wardha (M.S.)

ABSTRACT

Network on Chip (NoC) is one solution for designing communication among components in the SoC circuits with several billion transistors that will reach the market in approximately 5-10 years from now. Different topologies having various advantages according to their applications. This paper present brief idea about topologies depending on parameter.

Keywords

System on Chip, Network on Chip, Different Topologies and topology parameter.

I. INTRODUCTION

System on chips are not containing IP cores only and traditional methods for communication such as bus are not suitable solution for future System on chips. That is impossible to send signals from one end to another end within a clock cycle. Problems such as global wire delay and global synchronization will limit us. In order to overcome these problems, designer use models, techniques, and tools from network design field and apply them to System on chips design that leads to new paradigm called Network on chip. Network on chip is solution for communication architecture of future System on chips that are composed of switches and IP cores where communicate among each other through switches. Between IP cores data move in the form of packet. Network on chip is an emerging approach for the implementation of on chip communication architecture.

The Network-on-Chip(NoC) is a communication centric interconnection approach which provides a scalable infrastructure to interconnect different IPs and sub-systems in a SoC [5, 7, 17]. Moreover, NoCs can make SoCs more structured, and reusable, and can also improve their performance [5, 8]. However, solutions to overcome performance limitations in NoCs are yet to be presented. Many topologies with different capabilities have been proposed for NoCs including Mesh [8], Torus [7], Octagon [9], SPIN [4], and BFT [11]. In such cases, one of the main goals is to improve network performance by providing better static topological characteristics such as diameter and average inter-node distance [8]. However, when designing communication architecture, it is vital to consider the effect of physical design constraints such as wire routing, wiring density, and power consumption. The authors of [13] showed that in contrast to normal beliefs, on chip interconnections suffer from certain physical limitations which lead to great performance reduction.

This paper organised as follows, Section II deals with different NoC Topologies, Section III deals with literature review, Section IV explain the comparison between various topologies, Section V deals with proposed work, Section VI presents Conclusion and Finally Section VII parents references.

II. NoC TOPOLOGIES

Network topology refers to the shape of the network. How the different nodes in a network are connected to each other and how they communicate are determined by the network's topology.

Mesh topology comes in two types. They are full mesh and partial mesh. Full mesh means that a node is connected to every other node in the network; this is a very costly method and mostly used to connect busses. Partial mesh means that a node doesn't have to be directly connected to all other nodes. This type of mesh is not as costly as full mesh, but the disadvantage is less redundancy.

2D-array is a type of mesh in which nodes form a two dimensional grid where each node is connected to the four adjacent routers. The routers at the edges have only two or three connections since they don't have more adjacent routers. The number of nodes will then become CxR where C is the number of columns and R is the number of rows.
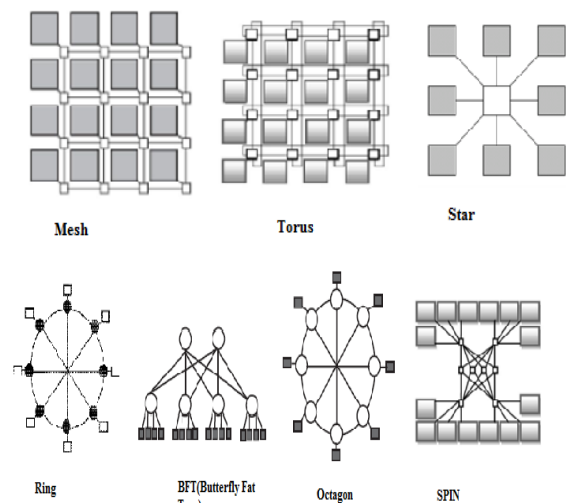
FIG 1 . NOC TOPOLOGIES

Torus is a topology, which is similar to the 2D-array in which nodes form a regular cyclic 2- dimensional grid. Here all routers have four connections since a torus basically is a mesh with wrap-around on the edges.

Star topology uses a central hub to which all recourses are connected. All communication between resources is then passed through the central hub. Ring topology when the resources are connected to each other in a ring. Every resource is then connected to its two neighbours communication with other resources then has to pass through the neighbours. Bus topology means that several resources use the same communication channel. Octagon Topology is one of the type of ring topology. It consists of several eight paths so it is called as octagon. Binary Tree Topology(BFT) has a central

root node that is connected to one or more nodes of a lower hierarchy. In a symmetrical hierarchy, each node in the network has a specific fixed number of nodes connected to those at a lower level. Scalable, Programmable, Integrated Network (SPIN) architecture. This architecture implements the topology similar to Butterfly Fat Tree Topology with some changes. In this topology router in each level consists of same number of parent ports and child ports. This type of topological structure provides higher throughput compared with Butterfly Fat Tree Topology.

In an ordinary local area network this can results in collisions, caused by two resources sending a packet at the same time. If you want to avoid collisions it is a possible to let the resources send their packet in a time slot, which is unique for each resource.

III. LITERATURE REVIEW

Haytham Elmiligi, Ahmed A. Morgan, M. Watheq El-Kharashi, Fayez Gebali, [1]. In this paper the impact of network the network topology on NoC system delay using graph-theoretic concept. In this paper model which was based on topology was developed to calculate average NOC delay which is caused by the links and routers. A case study of MPEG4 video application is presented to explain how the proposed model could be used to minimize the network delay by selecting the best topology. Experimental result show that the average network delay could have been increased if a wrong topology was chosen.

M. Mirza-Aghatabar, S.Koohi, S. Hessabi, M. Pedram. [2] proposed compare two popular NoC topologies, i.e., mesh and torus, in terms of different figures of merit e.g. latency, power consumption, and power/throughput ratio under different routing algorithms and two common traffic models, uniform and hotspot. To the best of our knowledge, this is the first effort in comparing mesh and torus topologies under different routing algorithms and traffic models with respect to their performance and power consumption. Torus always has better latency than mesh topology.

M. Nickray, M.Dehyadgari, and A. Afzali-kusha, "Power and Delay optimization for network on chip,[7]. This paper, they were introduced an algorithm based on genetic algorithm for optimizing power consumption and delay of applications which are mapped on fat tree topology. In this paper developed a NOC communication power model to estimate the power consumption in communication. Algorithm consists of Vertex mapping to PEs, Node mapping and Delay optimization. These steps map task graphs into a fat-tree NOC how had been minimum power consumption. Algorithm was proposed in this paper could be applied to various derivatives of fat-tree topology. Our work could be extended with achieving to more accurate model for power.

Victor Dumitriu and Gul N. Khan, "Throughput-Oriented NoC Topology Generation and Analysis for High Performance SoCs",[17]. In this paper presents a new approach to the design and analysis of NoC topologies which is based on the transaction-oriented communication methods of on-chip components. They propose two algorithms that attempt to meet the communication requirement of an on-chip application using a minimum number of network resources for the task, by generating application-specific topologies. And they are also design process of complex systems, the design method incorporates a form of predictive analysis which can estimate the degree of contention in a given system without performing detailed simulation. This predictive analysis method is used to determine the minimum frequency of operation for generated topologies, and is incorporated into the topology generation process. The proposed design method was tested using real-word applications, including an MPEG4 decoder and a Multi-Window Display application. The generated topologies were found to offer similar or better performance when compared with regular topologies. However, the topologies generated by our method were more economical, using, on average, half the network resources of regular topologies. As well, a method for the estimation of dynamic effects in the system is proposed which does not require extensive simulation at the design stage. This predictive analysis method is incorporated into the topology generation process and allows the automatic generation of topologies based on potential contention in the system. The proposed methods are tested using a simulation environment dedicated specifically to on-chip communications, implemented using SystemC. The simulation models accurately reproduce on-chip communication behavior, including signal level

interfacing between components. The proposed topologies offer similar performance when compared with regular topologies while using less than half the required number of network resources, on average. As well, the prediction algorithm is found to be accurate to within 27% in worst case situations, despite the reduced complexity of the analysis method employed.

Mahmoud Moadeli1, Ali Shahrabi2, Wim Vander bauwhede1, Mohamed Ould-Khaoua[18]. In this paper the spidergon topology emerged to realize cost effective MPSoC development using a fixed and optimized NoC architecture. In this paper they have analyzed the traffic in the architecture and presented a model to compute the mean message latency in the spidergon architecture employing wormhole switching. Extensive simulation experiments have shown the analytical model predicts the message latency with a good degree of accuracy in a wide range of traffic rates. In particular the model well predicts the saturation points in the networks with different configurations. Their next objective is to investigate the impact of employing more virtual channels and adopting adaptive routing on the latency in the spidergon scheme. Developing a cost model to study the effect of the channel length on evaluations as the size of the network grows is their another goal we. They are going to analytically compare the spidergon NoC with other topologies in the domain including mesh and torus.

IV. COMPARATIVE STUDY

Comparative study different topologies on the basis of delay parameter is as shown in the following table.

Topology	Average network delay
Mesh	29
Torus	25
Folded Torus	26
Ring	32
Octagon	21
Spider	24
BT	59
BFT	40
SPIN	40

V. PROPOSED WORK

In the previous work they were using various topologies such as mesh, torus, octagon, SPIN, BFT etc. and compare with different parameters such as power, delay, area, throughput. In the previous work they were compare different topologies such as mesh, torus, folded torus, SPIN, BF, BFT etc with delay parameter. In the next paper they were compare mesh and torus topology in terms of different figures of merits for

example latency, power consumption and power/throughput ratio. In the next paper they were introduced an algorithm based on genetic algorithm for optimizing power consumption and delay of applications which are mapped on fat tree topology. In the next paper they were presents a new approach to the design and analysis of NoC topologies which is based on the transaction-oriented communication methods of on-chip components. They propose two algorithms that attempt to meet the communication requirement of an on-chip application using a minimum number of network resources for the task, by generating application-specific topologies. In the next paper they have analyzed the traffic in the architecture and presented a model to compute the mean message latency in the spiderg on architecture employing wormhole switching. Our proposed work is to comparative study of various topologies in terms of average network delay. And comparing all the topologies according to the delay parameter.

VI. CONCLUSION

In the previous work they were using various topologies such as mesh, torus, octagon , SPIN, BFT etc. and compare with different parameters such as power, delay, area, throughput. In the previous work they were compare different topologies such as mesh, torus, folded torus, SPIN, BF, BFT etc with delay parameter. In the next paper they were compare mesh and torus topology in terms of different figures of merits for example latency, power consumption and power/throughput ratio. In the next paper they were introduced an algorithm based on genetic algorithm for optimizing power consumption and delay of applications which are mapped on fat tree topology. In the next paper they were presents a new approach to the design and analysis of NoC topologies which is based on the transaction-oriented communication methods of on-chip components. They propose two algorithms that attempt to meet the communication requirement of an on-chip application using a minimum number of network resources for the task, by generating application-specific topologies. In the next paper they have analyzed the traffic in the architecture and presented a model to compute the mean message latency in the spidergon architecture employing wormhole switching. This paper explains different topologies according to various parameters and it gives comparatively study of delay parameter. So our proposed work is to compare different topologies using delay parameter.

VII.REFERENCES

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