Review of Quaternary Adders in Voltage Mode Multi-Valued Logic

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ABSTRACT
The Binary logic circuits design is limited by the requirement of number of interconnections which increases the chip area with increase in logic. Multi valued logic designs are gaining importance form that perspective. Adders are one of the important part of the processing element and hence it has a focus of research. Therefore design of adders using multi valued logic can prove to be very useful. Thus there is a need to design a optimal adder. In this paper we review Quaternary Adders circuit. The proposed adders are to be design in Multi-Valued Voltage Mode Logic and investigate the effect of one parameter on another. Optimized adders will be designed, analyzed and proposed for multi-valued logic arithmetic unit design which will achieve the practical ranges of parameters of circuit.

Keywords
Voltage Mode Multiple-Valued Logic, Quaternary Logic.

1. INTRODUCTION
Computers have become very complex machines, running on processors with millions and millions of circuits and running at clock speeds of 4GHz and higher. The programs running on these machines are even more complex, involving millions of instructions. Despite all this complexity, the stunning fact is that the basic component of all this machinery is the very basic binary switch, which switches between two states. Some people have tried to explain all this complexity from a perspective of "symbol processing." Other has tried to connect our thinking with binary logic, which is the 'language' of binary switching. No matter how it is all explained, the fact remains, that for over 70 years, computing devices as we know them have been based on the simplest of simple switching states: "on" and "off"'. Binary technology appears to be a given, a fundamental approach to allow a machine to perform instructions. It also appears to be limiting. Just two states? To automate all our thought processes? What would one be able to do with a machine that performs non-binary switching? What would it require? What would it look like? How does one apply it?

The answer to this is Multi-valued logic. "Elean Dubrova" basically defines Multi-valued logic is like painting a picture having all possible colours available [1]. Multi-value logic is defined as a non-binary logic and involves the switching between more than two states. Multi-valued logic means instead of assuming one of the two states as per in binary logic , signal may assume one of more than two states , for instant 4 states. Binary values take only values {0,1}.Multi-valued synthesis take multivalued variables Xi can take values Pi={0,…pi-1}.

Multi-valued logic offers important advantage like more information can be processed over a given set of lines to reduce the burden of interconnections and thereby switching[2]. The advantage of Multi-valued logic are the use of fewer operations potentially fewer gates and reduction in number of interconnections and switching. The reduction of dynamic power dissipation is VLSI applications is the major challenge for today's engineers as major portion of the power is consumed by interconnect and switching [3].

Adders form the basic part of processing element. An adder is basically a circuit which is used in variety of applications. So, if we create an optimized adder simultaneously the processing elements will be improved. This will fasten the calculation of arithmetic Logic Unit which further improves and fasten the performance of the unit. Using an optimized adder using Multi-Valued logic will lessen the space required. Optimized adders will prove to be useful in other Digital Signal Processing as adders are the basic part of Digital Signal Processing.

Increased data density, reduced dynamic power dissipation, and increased computational ability are among some of the key benefits of Multiple Valued Logic (MVL). Several Implementation methods have been proposed in the recent papers to realize the Multi-valued logic circuits.[4,5].They can be fundamentally categorized as current –Mode, voltage mode and mixed mode circuits. Several prototype chips of current-mode CMOS circuits have been fabricated, showing somewhat better performances compared to the corresponding binary circuit[6-9]. Even though current-mode circuits have been popular and offer several CMOS binary logic circuits from the perspective of dynamic switching activity. Several approaches for quaternary circuit design have been proposed [7-12], in voltage mode technique. benefits, the power consumption is high due to their inherent nature of constant current flow during the operation. Alternatively, voltage-mode circuits consume a large majority of power only during the logic level switching.

Hence, voltage-mode circuits do offer lesser power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity. Several approaches for quaternary circuit design have been proposed [7-12], in voltage mode technique. In current mode circuits the power dissipation is high due to their inherent nature of constant current flow during the operation. Alternatively, volatage mode circuits consume a large majority of power only during the logic level switching. Hence, voltage –mode circuits offers lesser power consumption which is the key benefit. Quaternary logic (radix-4-valued) is chosen as the base radix. Using a quaternary radix offers all the benefits of MVL with the important advantage of being able to easily interface with traditional binary logic circuits.

2. Review of MVL Adders
Novel quaternary half adder, full adder, and a carry-look ahead adder were introduced by M Thoidis [13]. In his paper, the proposed circuits were static and operate in voltage mode.

They reported no static power dissipation as the circuits were static in nature.

Ricardo designed a new truly full adder quaternary circuit using 3 power supply lines and multi-Vt transistors. He has designed quaternary multiplexer (MUX) 4:1 with 4 quaternary inputs and one quaternary output and used this MUX as a building block to construct full adder. The proposed multiplexer circuit is based on voltage-mode quaternary logic CMOS circuits. These circuits use several different transistors with different threshold voltages and operate with four voltage levels, corresponding to 0V common terminal and three power supply lines of 1V, 2V and 3V. The quaternary MUX is designed using Down Literal Circuits (DLCs), binary inverters and pass transistor gates. Down Literal Circuits performs the functions shown in table I. There are 3 possible Down Literal Circuits in quaternary logic, named DLC1, DLC2 and DLC3.

IN	Down Literal Circuit Output		
	DLC1	DLC2	DLC3
0	3	3	3
1	0	3	3
2	0	0	3
3	0	0	0

Table I . Down Literal Circuit Truth Table

The Down Literal Circuits are designed in CMOS technology with 3 different threshold voltages for PMOS transistors and 3 different threshold voltages for NMOS transistors. Table II shows Vt values relative to the transistors source-bulk voltages.

	T1	T2	T3	T4	T5	T6
Vt	-2.2	2.2	-1.2	0.2	-0.2	1.2
Type	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS

Table II Transistor Vt values related to Vs

The quaternary multiplexer 4:1 is designed using the 3 DLCs, 3 binary inverters and 6 pairs of pass transistor gates and its schematic is presented in figure 1.

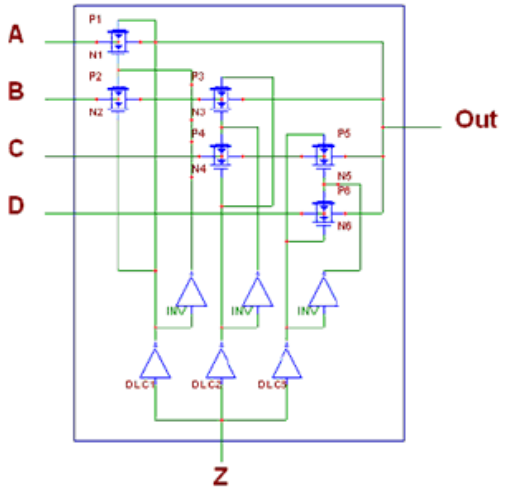

Figure 1 : Quaternary MUX 4:1 schematic circuit

This circuit has 4 quaternary inputs (A, B, C and D), one quaternary output (Out) and 1 quaternary control signal (Z) that sets the output to one of the 4 inputs.

Proposed technique benefits large scale circuits since the much power dissipation with increased speed can lead to the development of extremely low energy circuits while sustaining the high performance required for many applications [14].

Quaternary full adders based on output generator sharing are proposed by Hirokatsu . Full adder are proposed for a high-performance multi-processor which consists of many processing elements (PEs). Arbitrary quaternary functions are represented by the combination of input-value conversion and several quaternary output generations. The use of appropriate input-value conversion makes it possible to reduce the number of output generators, which improves the performance of the resulting Quaternary full adders. In this paper the Quaternary full adder is constructed using the above method and their efficiencies are demonstrated in terms of delay and power dissipation in comparison with those of a corresponding binary CMOS implementation. Table III shows truth tables of quaternary to binary conversion.

IN	G0.5	G1.5	G2.5
0	0	0	0
1	1	1	0
2	1	1	0
3	1	1	1

a)

IN	GA	GB
0	0	0
1	1	0
2	1	1
3	0	1

b)

Table III Truth tables of quaternary to binary conversion represented by
a) Three kinds of binary signals b) two kinds of binary signals

In a basic quaternary circuit, each comparator has one logical threshold T(T={0.5,1.5,2.5} and each quaternary input signal is converted into three binary signalsG0.5,G1.5 and G2.5, given in Eqs.(1)-(3) as

$$G0.5 = \begin{cases} 0 & \text{if } IN < 0.5, \\ 1 & \text{if } IN > 0.5 \end{cases} \quad (1)$$

$$G1.5 = \begin{cases} 0 & \text{if } IN < 1.5, \\ 1 & \text{if } IN > 1.5 \end{cases} \quad (2)$$

$$G2.5 = \begin{cases} 0 & \text{if } IN < 2.5, \\ 1 & \text{if } IN > 2.5 \end{cases} \quad (3)$$

By allowing a comparator to have two logical thresholds, these signals can be represented in two signals GA and GB given in Eqs.(4)-(5) as

$$GA = \begin{cases} 0 & \text{if } IN < 0.5 \text{ or } 2.5 < IN \\ 1 & \text{if } 0.5 < IN < 2.5 \end{cases} \quad (4)$$

$$GB = \begin{cases} 0 & \text{if } IN < 1.5, \\ 1 & \text{if } IN > 1.5 \end{cases} \quad (5)$$

This representation enables to reduce comparators, which results in the reduction of storage elements in quaternary sequential circuits. Table 4 shows truth tables of quaternary full addition.

Table IV Truth tables of quaternary Full addition.
Sum Block:

S0		X			
		0	1	2	3
Y	0	0	1	2	3
	1	1	2	3	0
	2	2	3	0	1
	3	3	0	1	2

S1		X			
		0	1	2	3
Y	0	1	2	3	0
	1	2	3	0	1
	2	3	0	1	2
	3	0	1	2	3

Carry block:

X and Y are the adder inputs,S0 and CO0 are the sum and carry outputs when the carry input is "0", and S1 and CO1 are the sum and carry outputs is "1".The expressions for S0, S1, CO0 and CO1 are given in Eqs.(6)-(9) as

S0 = X+Y if X+Y < 4
X+Y-4 if X+Y>=4 **(6)**

S1 = X+Y+1 if X+Y+1 < 4
(X+Y+1)-4 if X+Y+1 >=4 **(7)**

CO0 = 0 if X+Y<4
1 if X+Y>=4 **(8)**

CO1 = 0 if X+Y+1<4
1 if X+Y+1>=4 **(9)**

If Y'is defined as the sum of Y and CI,S0 and S1(CO0 and CO1)are naturally summarized in S(CO0) for which expressions correspond to those of quaternary half addition, given in Eqs. (10) and (11) as

S = X+Y' if X+Y' < 4 **(10)**
X+Y'-4 if X+Y'>=4

CO = 0 if X+Y'<4
1 if X+Y'>=4 (11)

This means that quaternary full addition can be decomposed into carry pre-addition and quaternary half addition. The algorithm of decomposed quaternary full addition is summarized as

Step 1 : Y' = Y+C1 if Y+C1 <4
Y+C1-4 if Y+C1=4,
Step 2(a) : S = X+Y' if X+Y'<4
X+Y'-4 if X+Y'>=4
Step2(b) : CO = 0 if X+Y'<4
1 if X+Y'>=4
OR Y+C1=4

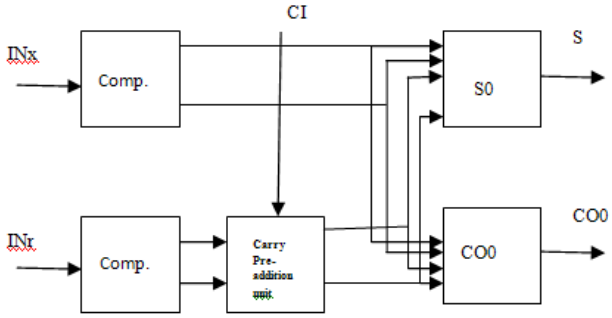

Figure 2 : Proposed quaternary full adder

C00		X			
		0	1	2	3
Y	0	0	0	0	0
	1	0	0	0	1
	2	0	0	1	1
	3	0	1	1	1

CO1		X			
		0	1	2	3
Y	0	0	0	0	0
	1	0	0	1	1
	2	0	1	1	1
	3	1	1	1	1

Figure 2 shows a block diagram of the proposed quaternary full adder. The decomposition of the quaternary full addition into carry pre-addition and quaternary half addition enables to share the S0 generator and S1 generator (the C0 generator and C1 generator) Since the output generators have large input capacitances, the sharing results in high-speed operation.

Logic value	0	1	2	3
Voltages[V]	0	0.4	0.9	1.2

Figure 3 : Relation between MV Logic values and voltage values in voltage mode implementation.

Figure 3 indicates logical values and threshold values, and their corresponding voltage values, respectively. The proposed adders are designed with reduction in delay and power[15].

The implementation of Quaternary Signed Digit addition was presented in paper [16]. The test confirms the superior performance of the QSD adder implementation over other adders due to the carry - free addition scheme. The complexity of the QSD adder was linearly proportional to the number of digits, which are of the same order as the simplest adder, the ripple carry adder. This QSD adder can be used as a building block for other arithmetic operations such as multiplication, division, square root, etc. With the QSD addition scheme, some well-known arithmetic algorithms can be directly implemented [16].

Supplementary Symmetrical Logic Circuit (referred as SUSLOC) was presented in [17]. This work illustrates how quaternary gates can be implemented using the SUSLOC circuit structure. These gates were then used to build three different addition circuit architectures: carry-ripple, carry-look ahead, and carry-select. These three quaternary addition circuits are then modeled using the System Verilog language. The three different adder architectures are designed and compared for area and estimated performance with their binary circuit counterparts

[17].
Full adder circuit proposed by Vasundara Patel K.S., K.S. Gurumurthy is based on Encoder, code generator, sum block and carry block. Encoder is required for the conversion shown in table 4, consists of DLC1 and DLC3 (Down literal circuit) [18].
A full adder circuit is designed by converting the quaternary logic in to unique code, which enables to implement circuit with reduced hard ware. Sum and carry are processed in two separate blocks, controlled by code generator unit. Simple pass transistors are used for implementation. The design is targeted for the 0.18 μm CMOS technology. Area of the designed circuits is less than the corresponding binary circuits and quaternary adders because number of transistors used are less. Figure 4 Shows the block diagram of proposed adder.[19]

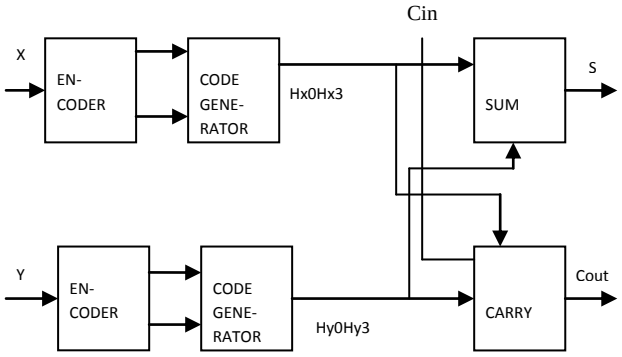

Figure 4 : Proposed quaternary full adder

This proposed adder consists of Encoder block, Code Generator block Sum and Carry blocks.

In the adder proposed by Takahiro Hanyu a high-speed, low-power and compact processing element using quaternary differential logic is proposed for a multi-core single-instruction multiple-data (SIMD) processor. A two-bit addition which is the critical path of the ALU is attributed to a one-digit quaternary addition that is directly performed by using multiple-valued current- mode (MVCM) differential logic circuitry. A one-digit quaternary flip-flop is also simply implemented by using the MVCM differential logic circuitry. [20]

3. PROPOSED ADDERS

Taking in view the investigation which includes three quaternary full adder circuits, proposed by Recardo Cuna et.al [17],Hirokatsu Shirahama et.al [18], Hirokatsu Shirahama et.al
[21] and corresponding binary adder. In paper [17] 180nm technology file and power supply of 3V is used. It is dissipating dynamic power supply of 181 μW at 250 MHz and it shows delay of 2.24ns. It requires 332 transistors. Paper [18] uses 90nm technology files and 1.2V power supply. Propagation delay of 113ps and dynamic power 55 μW at 1 GHz is observed.. In [21] 180nm and 1.8V power supply is used. Propagation delay of 1.4ns and power dissipation of 194 μW is observed at 300MHz. In the adder proposed by Takahiro Hanyu used 180 nm technology, 3 V power supply and 250 M Hz on synopsys Hspice and Cscope for full adder design and 1GHz for half adder design. Logic levels are well defined and independent of fabrication process variations of the component[21]. Power dissipation and delay are observed for sum and carry blocks of both half adder and full adder. Proposed half adder dissipates 112 μW of power at 1 GHz and shows delay of 1.8 ns. Number of transistors required are 76. Proposed full adder dissipates 84 μW of power at 250 MHz and delay of 2.02 ns and number of transistors required are 148. The use of appropriate input value conversion makes it possible to reduce the hardware.
Proposed adders are to be implemented in voltage mode using Quaternary logic. Thus an optimal adder is to be design by investigate the effect of one parameter on another.

4. RESULT AND DISCUSSION

Taking in view the discussion and the design of different quaternary adders an optimal Quaternary adder is to be designed, analyzed and proposed for multi-valued logic arithmetic unit design which will achieve the practical ranges of parameters of circuit. Consequently, this design is appropriate to be applied for high performance which consists of many processing elements.

5. CONCLUSION

Different quaternary adders are designed analyzed and proposed. These quaternary adders are designed using different techniques and different adders are compared on basis of different parameters. Thus we investigate ,analyze different adder on the basis of different parameters. Hence, we can create an optimized adder and can investigate the effect of one parameter on other.

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