Application of Current-Mode Multi-Valued Logic in the Design of Vedic Multiplier

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ABSTRACT
Vedic multiplier is based on ancient Indian Vedic mathematics that offers simpler and hierarchical structure. Multi-valued logic results in the effective utilization of interconnections, which reduces the chip size and delay. This paper proposes that if the potential of multi-valued logic is combined with simplicity of Vedic architecture, it may result in an efficient multiplier design. Since the performance of a digital signal processor depends mainly on the multipliers used, the proposed approach can greatly enhance the performance of a digital signal processor.

Keywords
Current-Mode Multi-Valued Logic, Vedic Multiplier, Arithmetic Circuits, Digital Signal Processing

1. INTRODUCTION
A multiplier is an essential component of a Digital Signal Processor (DSP). Multipliers are essential in implementation of systems realizing many important functions such as fast fourier transforms and multiply accumulate. Performance of DSP depends heavily on its multipliers. Hence, a DSP chip needs compact, fast, reliable and low power consuming multipliers. The delay in an arithmetic unit of DSP is mainly due to its multipliers. Longer word-lengths in binary logic make the multiplier large and complex. In binary logic, the size of the device is reduced by reducing the sizes of the transistors. But it has a limit, since the sizes of transistors cannot be reduced indefinitely. By applying multi-valued logic to the multiplier design, word-lengths and the number of transistors can be reduced. There are various multipliers for binary logic such as array multiplier, Booth multiplier, Wallace tree multiplier and Vedic multiplier. Vedic multiplier has caught the attention of researchers in recent years because of its superiority over other multipliers. If the functional blocks designed in multi-valued logic are used in Vedic multiplier's architecture, it will surely enhance the performance of multipliers and hence the whole DSP chip.

1.1 Vedic Mathematics
The Sanskrit word 'Veda' means 'Knowledge'. Vedic Mathematics is a name which is heard many times with reference to the techniques for solving mathematical problems mentally. Vedic mathematics techniques were rediscovered in the early twentieth century from ancient Indian sculptures by Sri Bharati Krishna Tirthaji Maharaj. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operations without much help of pen and paper. Any ordinary human can perform these mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. Vedic mathematics provides more than one method for basic operations like multiplication and division. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further. These methods can be directly applied to trigonometry, plain and spherical geometry, conics, calculus and applied mathematics of various kinds.

1.2 Multi-Valued Logic (MVL)
It was first proposed by Jan Lukasiewicz, Polish minister of Education in 1919, followed by Emil Post**,** American logician born in Poland. MVL employs more than two discrete levels of a signal, such as ternary, quaternary or even more.
Binary logic dominates the hardware implementation of DSP systems. But it has many drawbacks and limitations. A signal cannot always be just ON or OFF, it can assume another state such as UNKNOWN, DON'T CARE, HIGH IMPEDANCE, etc. Not considering these states can result in inefficient processing of the data. Also, binary logic results in longer word-lengths which increase the number of interconnections and hence the chip size. This hampers the performance of the system.
All these problems in binary logic can be solved by using multi-valued logic that uses more than two logic levels for a signal.

1.3 Operating Modes of MVL
MVL can be employed in either voltage-mode or current-mode. In voltage-mode MVL, operating voltage range is divided into the number of logical values to be represented, e.g. for 5V circuit employing quaternary logic, logic levels 0, 1, 2 and 3 can be assigned to 0V, 1.5V, 3V and 5V respectively. In current-mode MVL, currents are usually defined to have logical levels that are integer multiples of a reference current unit, e.g. logic levels 0, 1, 2 and 3 can be assigned to 0uA, 10uA, 20uA and 30uA respectively.

1.4 Advantages of MVL over Binary Logic
- It reduces the number of interconnections.
- It results in smaller circuitry, less power dissipation, less delay, greater speed and low cross-talk noise.
- It increases the data processing capability per unit chip area.
- Quaternary logic signals easily interface with the binary world; they may be decoded directly into their two-digit binary equivalents.
- It offers the use of signal space that combines some of the efficiency of analog signaling with the noise immunity of digital signaling.

In spite of having so many advantages, there is less research interest in MVL because such circuits are not yet widely used in industrial products. This is because the binary logic is simple and sufficient for present day technologies. But as more complex technologies are being invented, the future will be of MVL and not binary logic. The research in MVL is still in initial stage and the work is more theoretical and fundamental. But if the hardware implementation of MVL circuits is

popularized, MVL will surely dominate the binary logic one day.

2. POPULAR VLSI MULTIPLIERS [2]

There are a number of techniques for performing multiplication in binary logic. In general, the choice is based upon factors such as latency, throughput, area and design complexity. Some most commonly used techniques are briefly discussed below.

2.1 Array Multiplier

In an array multiplier, multiplication of two binary numbers can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. Array Multiplier consumes more power and delay is larger. It also requires larger number of gates because of which area is also increased. Due to this, array multiplier is less economical.

2.2 Wallace Tree Multiplier

A fast process for multiplication of two numbers was developed by Wallace. Using this method, a three step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product. In Wallace tree method, the circuit layout is not easy although the speed of the operation is high since the circuit is quite irregular.

2.3 Booth Multiplier

Another improvement in the multiplier is by reducing the number of partial products generated. The Booth recording multiplier is one such multiplier. It scans three bits at a time to reduce the number of partial products. These three bits are: two bits from the present pair and third bit from the high order bit of an adjacent lower order pair. To speed up the multiplication, Booth encoding performs several steps of multiplication at once. The high performance of Booth multiplier comes with the drawback of power consumption. The reason is large number of adder cells required that consume large power.

The various drawbacks of these three multipliers provide a space for ancient Indian Vedic mathematics that gives efficient formulae for multiplication which increases the speed of multiplier.

3. REVIEW OF VEDIC MULTIPLIERS

Vedic mathematics is based on 16 sutras or formulae written in ancient Indian Vedas. Two of these sutras are useful for multiplication viz. Nikhilam sutra and Urdhva Tiryakbhyam sutra. Nikhilam sutra means "all from 9 and last from 10". It is more efficient when the operands are very large [6] and close to an integer power of 10. Its limitation is that both operands should be either less or greater than the selected power of 10. Urdhva Tiryakbhyam sutra, which means "vertically and crosswise", is more popular than Nikhilam sutra since it is applicable in all cases. Fig.1 shows how the multiplication 96x93 can be done using Nikhilam sutra and Fig.2 illustrates the line diagram for multiplication of two 4-bit numbers using Urdhva Tiryakbhyam sutra [1]-[3]. It can be clearly visualized from these figures that Vedic multiplication is much simpler than conventional multiplication.

In Vedic multiplier, partial product terms are calculated in parallel and hence the delay involved is just the time it takes for the signal to propagate through the gates. Thus, Vedic multipliers are suitable for fast parallel processors [3].

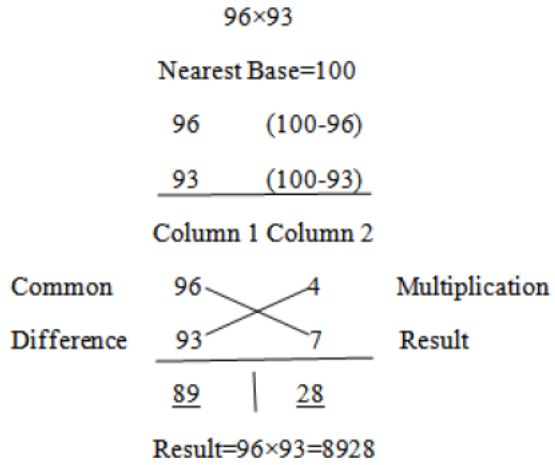

Fig 1: Multiplication of Decimal Numbers Using Nikhilam Sutra

From the perspective of digital hardware, there is no difference in conventional multiplication and Vedic multiplication. Both are combinational multipliers requiring same number of addition and multiplication operations and hence the same amount of hardware [5]. Still, Vedic multiplier has drawn the attention of the researchers because of its simple architecture and hierarchical structure. A 2x2 Vedic multiplier can be used to design 4x4 multiplier, which can be used to design 8x8 multiplier, and so on.

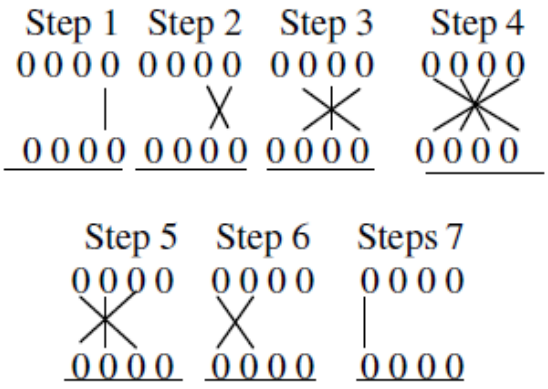

Fig 2: Line Diagram for Multiplication of Two 4-bit Numbers Using Urdhva Tiryakbhyam Sutra

It has been proven in various researches that Vedic multiplier is superior to Array and Booth multipliers in terms of delay, power consumption and size [2]-[4]. Also, Vedic multiplier can be realized using Hardware Description Languages (HDL) like VHDL [5] and Verilog-HDL [3].

If the functional blocks used in Vedic multiplier, such as half adders and full adders are designed efficiently, its performance can be further optimized.

4. REVIEW OF MVL CIRCUITS

MVL is not a new field. But its hardware implementation is not much popular yet. But the researchers, who work in MVL, feel that the binary logic is already doomed. This is just like, if you have colour pencils with you, why to draw a black and

white picture! It is believed that after some years, binary logic will be insufficient for modern technologies and then the whole research done in MVL will be utilized at once. As the amount of information to be processed goes on increasing, binary logic loses its dominance and MVL starts gaining its power. Though it is possible to employ MVL in almost all the areas where binary logic is used, the main potential of MVL is explored in fuzzy applications and arithmetic circuits.

Since both MVL and fuzzy systems use more than two logic levels, fuzzy systems can be made relatively analog by using MVL. Fuzzy inference rules can be used as multi-valued logic functions. V. Varshavsky et al. have done extensive research in this area. First, a functional completeness of summing amplifier with saturation in an arbitrary-valued logic is proven. This summing amplifier is then used as a basic building block for designing a fuzzy controller. Compared with the traditional approach based on explicit fuzzification, fuzzy inference and defuzzification procedures, analog fuzzy implementation has the advantages of higher speed, lower power consumption, smaller die area and more [17]-[18].

5. REVIEW OF ARITHMETIC CIRCUITS BASED ON MVL

The use of MVL allows each input to accept and each output to deliver more information. In other words, the number of logic stages in an MVL circuit is less than that in a corresponding binary logic circuit, which results in the reduction of the delay [9]. Voltage-mode MVL circuits have been achieved in multithreshold CMOS design. A multithreshold CMOS design relies on body effects using different bias voltages to the base or the bulk terminal of the transistors [15]. The voltage-mode MVL is preferred when the prime parameter to deal with is the power dissipation. If we go on increasing the logic levels in the voltage mode, the problem of noise margin will get worse. Hence, for higher radix, current-mode designs are preferred.

The basic current-mode building blocks used to perform most of the arithmetic operations are current sources, current mirrors, current comparators and voltage switched current sources. Using these basic blocks, various functional blocks such as adders, subtractors, etc. can be designed in current mode. A current mirror is used to produce multiple copies of an input current, each multiplied by a constant factor. It can also be used to change the sign of current just by reversing the direction of its copy. Comparators are required so that we can restore a current mode signal to its proper signal level. The comparator is often lumped with switched current sources, but the communication between these two sections is a binary signal, and consequently, this is an ideal place for simple binary logic. Comparators require references to compare against [8],[14]. Reference [9] proposes an appropriate input-value conversion which reduces the number of comparators, which results in reduction of storage elements in quaternary sequential circuits. It is applicable to both voltage-mode and current-mode MVL circuits. A novel design of threshold detector with high driving capability has been presented in [13] to improve the switching speed of current-mode MVL circuits.

The research done in MVL is more focused on designing half adders and full adders so that effective multipliers can be designed. Some new MVL gates like Top Gate, which is a shifter circuit, is presented in [10] that also proposes a switching block to design quaternary X gate equivalent to binary XOR gate. These gates can be used to implement an adder [11].

The main advantage of current-mode is that it reduces the number of active devices and wiring complexity since the frequently used linear sum operation can be performed simply by connecting those wires together by Kirchhoff's current law [13]-[14]. Carry unit is much simpler since carry-out signal will be assigned logic level 1 if the analog addition of inputs goes beyond certain reference current [11]. Also, current mode offers less delay and low transistor count as compared to voltage mode but at the cost of greater power dissipation [9].

MVL is also compatible with binary logic. Hence it can be used at the intermediate stage to modify the binary circuit. This reduces the delay and transistor count, thereby reducing the chip area of such binary circuit [7],[13],[16].

In MVL, most of the circuits designed have radix three or four. Ternary logic is more suitable for signed digit representation, e.g. if {-1,0,1} is used as the set of logic values, it already contains negative value. If unsigned numbers are to be deal with, quaternary logic is preferred since it is compatible and comparable with binary logic. Quaternary to binary or binary to quaternary conversions are also simple.

6. CONCLUSION

Since the research work in MVL is in fundamental stage, there is no standard circuitry established. Different researchers apply different logics. Thus there is a lot of scope to apply our own thinking. The researchers working in MVL are heading towards developing decimal circuits because human beings do the calculations in decimal system. Also, Vedic mathematics methods work as human mind works. So, both MVL and Vedic mathematics serve the same purpose. Combination with Vedic architecture will also popularize the hardware implementation of MVL circuits.

Current-mode MVL provides efficient designs of half adders, full adders and some single digit multipliers, whereas, Vedic multiplier provides simple architecture and it can be optimized by using efficient adders. Thus, if the functional blocks designed in current-mode MVL are used in Vedic architecture, the result will be far better which may change the whole scenario of arithmetic circuits used in DSP.

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