

Implementation of on Chip Data Bus Using Pre Emphasis Signaling

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ABSTRACT

This work describes a differential current-mode bus architecture based on driver pre-emphasis for on-chip global interconnects that achieves high-data rates while reducing bus power dissipation and improving signal delay latency. The 16-b bus core fabricated in 0.25- μ m complementary metal-oxide-semiconductor (CMOS) technology attains an aggregate signaling data rate of 64 Gb/s over 5–10-mm-long lossy interconnects. With a supply of 2.5 V, 25.5–48.7-mW power dissipation.

Keywords

interconnect, power dissipation, delay, crosstalk, noise

1. DRIVER PRE EMPHASIS CIRCUIT

What is pre emphasis?

In processing electronic audio signals, pre-emphasis refers to a system process designed to increase (within a frequency band) the magnitude of some (usually higher) frequencies with respect to the magnitude of other (usually lower) frequencies in order to improve the overall signal-to-noise ratio by minimizing the adverse effects of such phenomena as attenuation distortion or saturation of recording media in subsequent parts of the system. That is the mirror of the de-emphasis. The whole system is called emphasis. The frequency curve is decided by special time constants. The cutoff frequency can be calculated from that value. Pre-emphasis is commonly used in telecommunications, digital audio recording, record cutting, in FM broadcasting transmissions, and in displaying the spectrograms of speech signals. An example of this is the RIAA equalization curve on 33 RPM and 45 RPM vinyl records. In high speed digital transmission, pre-emphasis is used to improve signal quality at the output of a data transmission. In transmitting signals at high data rates, the transmission medium may introduce distortions, so pre-emphasis is used to distort the transmitted signal to correct for this distortion. When done properly this produces a received signal which more closely resembles the original or desired signal, allowing the use of higher frequencies or producing fewer bit errors

2. TRANSMITTER EQUALIZATION (DRIVER PRE-EMPHASIS)

Equalization techniques improve interconnect channel bandwidth and reduce delay latency by compensating for the high-frequency component loss in a low-pass channel. An equalizer compensates the channel high-frequency loss by either emphasizing high-frequency signal components or de-emphasizing low-frequency components to transmit an equalized signal to the receiver (Figure 1). Equalization techniques were traditionally limited in off-chip applications because on-chip signals were more controllable than off-chip signals. Therefore, it was not necessary to consume the extra power and area overhead and extra delay latency associated with equalization for on-chip applications. As technology scaling keeps producing faster logic but slower global interconnects, a high performance VLSI design is reaching the

point where on-chip signal bit error rate (BER) must be considered. Off-chip communication techniques are required for on-chip communication to accommodate this trend. Two main equalization architectures, Feed Forward Equalization (FFE) and Decision Feedback Equalization (DFE). DFE is only used at the receiver side equalization at the driver side is easier to implement for non-variant channels like on-chip interconnects, an FFE driver pre-emphasis architecture shown in Figure 1 is used in this work. It has only one tap on the equalization path to reduce power overhead and its output can be either single-ended or differential.

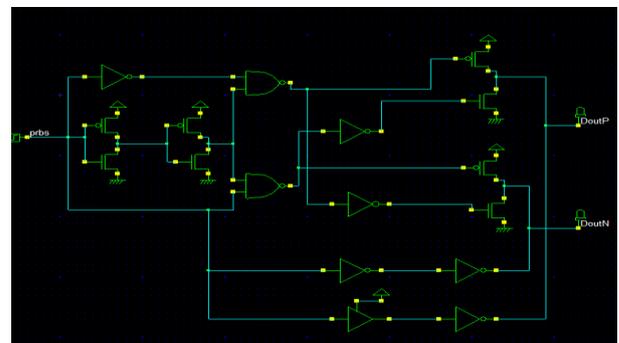


Figure 1. Driver Pre Emphasis Circuit

3. SIMULATION RESULT

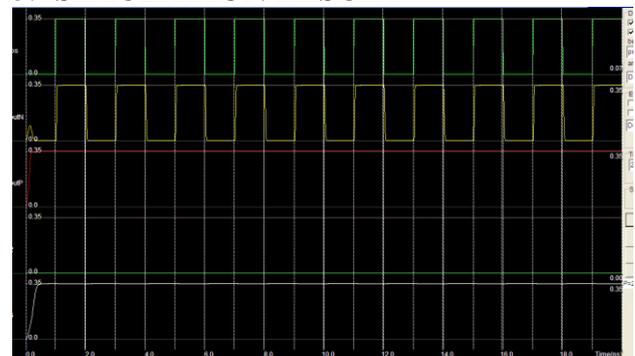


Figure: 2 Voltage Vs Current for Pre Emphasis

Figure 2 shows the simulation results of the waveforms at the driver output and receiver input. An equalized signal is achieved at the receiver input. The illustrative timing diagram is shown in Figure 3. Pre-emphasis is determined by every previous-sent-bit. Data sequence does not need to be pipelined or delayed before appearing at the driver output. Therefore, it does not introduce any extra clock-period of latency into the timing. All consecutive "1"s or "0"s are attenuated by one threshold voltage

TABLE – 1 :IMPLEMANTATION SUMMARY [9].

Parameters	Software Platform Used/Hardware Platform Used	Test Equipment Used	Result Obtained	Chances Improvement/Compromise Done
Prototype Chip	1-On chip PRBS generation & BER analyzer using 8-b data generator 2-BER Test conducted using 1-on chip analyzer 3-Highest 3.6130A error performance analyzer(BERT) 4-On-chip bond technique 5-High-speed signals were directly measured on-chip using high-impedance probes.	on chip high impedance port	1)die microphotograph of the 21.2mm Prototype chip fabricated in 0.25- μ m CMOS technology 2)power supply of 2.5V. 3)16-b, 32-Ch/s, 5-mm-long bus and an 8-b, 16-Ch/s, 10-mm-long bus, both using driver pre-emphasis, and a benchmark 16-b single-ended VM static bus with similar bus routing area for comparison. Of delay, power, and noise performance 4)Minimize the impact of wire bonding inductances	
B Noise and Delay Performance	Single-ended signals at the receiver input were measured and converted to differential signal by the oscilloscope for an active victim pair and a quiet victim pair	oscilloscope	cross-talk between adjacent lines behaves primarily as common-mode noise	
2)-noise swing	differential aggressors	quiet victim pair	cross-talk is 14.4% of the 250-mV signal swing	
3)-delay	eye diagrams at the receiver input when all lanes of the 16-b bus were switching randomly.		The 250-mV differential signal swing produced a 200-mV eye opening. The measured delay from the driver input to the receiver output is 590 ps including 160 ps of	

			driver delay and 210 ps of receiver delay, a 28.3% reduction compared to the reference single-ended repeater bus.	
4)-impact of crosstalk on the low swing bus due to a full-swing aggressor bus.	multilayer bus structure in Fig. 13 was also implemented in the test chip. It consists of a full-swing 8-b VM bus crossing orthogonally beneath the 16-b low-swing bus.		The worst-case crosstalk occurs when all the full-swing signals switch in-phase in the routing region near the receiver side of the low-swing bus.	The measured noise is still primarily common mode and can be ignored due to the small coupling capacitance between different layers.
C. Power Performance	data activity factors		For activity factors above 0.1, the 16-b pre-emphasis bus dissipates 25.5-48.7-mW power, equivalent to 0.00-1.32 pJ/b, a 15.0%-67.5% reduction in comparison to the reference VM repeater bus.	The relative power performance of the proposed pre-emphasis technique is higher only when data activity factors drop below 0.07. In addition, this technique compares favorably against typical CM buses as these require activity factors higher than 0.5 (random data) to achieve better power performance.
Power Performance	This power performance of the proposed pre-emphasis bus was also analyzed based on a time-based Alpha 21264 processor simulator program. Instruction and data (i.e., load/store) streams were modified to extract data activity profiles. A total of 100 million 32-b instructions and another total of 100 million 32-b data were collected for benchmarks from theSPECint2000 test suite. The accumulated data activity profiles from the GNU Compiler Collection (GCC) benchmark (i.e., C programming language compiler) are shown in Fig. 15 for instruction address, instruction, data address, and datapatterns.	1)-time-based Alpha 21264 processor simulator program 2)-SPECint2000 test suite 3)-GNU Compiler Collection (GCC) benchmark	Instruction bus (act=0.352), data address bus (act=0.097), and data bus (act=0.121) exhibit the same uniform activity distributions. Hence, the application of pre-emphasis can save 52.1% of power on the instruction bus, 13.2% on the data address bus, and 20.4% on the data bus	Pre-emphasis only saves 1.4% of power on the instruction address bus, but the instruction address bus exhibits a high correlation of switching activity for the lower order bits, which indicates a higher spatial locality among the address streams since instructions are usually stored in adjacent locations of memory. A bus scheme using pre-emphasis on lower order bits and traditional VM bus on higher order bits could be used to take advantage of this high spatial locality, but the delay latency difference between the two techniques would need to be adjusted if power optimization were the main concern.

(V_{th}) at D_{out} and “0” to “1” or “1” to “0” transition are emphasized. The signal swing attenuation reduces power consumption and the overdrive increases signaling speed by providing a larger signal than required at the receiver input. Both the attenuation and overdrive are the by-products of driver pre-emphasis, which de-emphasizes the low frequency component of signal to reduce inter-symbol interference (ISI) and improve bandwidth.

Table 2. Input For Pre Emphasis Circuit

Input clock	PRBS output 10 ns[*]	PRBS output[2]
Signal swing	75mv	100mv
Targeted data rate	2Gb/s	2Gb/s
Static current	2.00ma	1.6ma

Note: * Indicate results of project work which is simulated & verified in microwind & dsch

4. EYE DIAGRAM

What is an eye diagram?

In telecommunication, an eye pattern, also known as an eye diagram, is an oscilloscope display in which a digital data signal from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails. Several system performance measures can be derived by analyzing the display. If the signals are too long, too short, too noisy, or too slow to change, or have too much undershoot or overshoot, this can be observed from the eye diagram. An open eye pattern corresponds to minimal signal distortion. Distortion of the signal waveform due to inter symbol interference and noise appears as closure of the eye pattern.

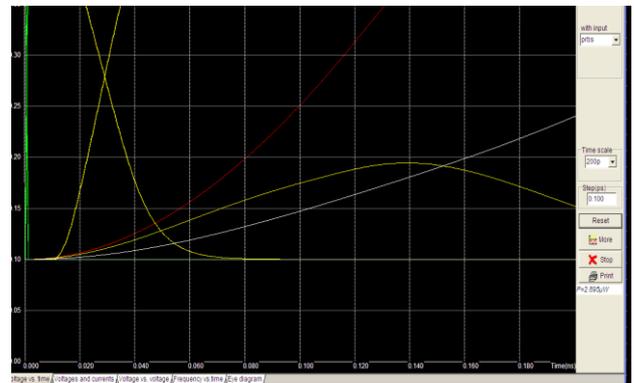


Figure 3 Eye Diagram for Pre Emphasis CircuitPAGE SIZE

5. SENSE AMPLIFIER

A flip flop sense amplifier is used for the receiver. The $V_{dd}/2$ bias helps build a large ($V_{gs}-V_{th}$) value on both inputs of the differential sense amplifier to make it less sensitive to transistor mismatch. Special considerations in layout, large input transistors and dummy cells, are used to compensate input offset. Here guideline from United State Patent (number:7557630,b2,7 July 2009) Name: sense amplifier based flip flop for reducing output delay and method thereof[20].

6. WORKING

The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage as shown in Figure.4. Thus SAFF is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch :or (but not both), depending whether the output is to be set or reset. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the

transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value. Therefore, the whole structure acts as a flip-flop.

6.1 Review of the Pulse-Generating stage Operation

When is low, nodes labeled and are pre charged through small and p MOS transistors, Figure. 4 The lower limit on the size of these transistors is determined by their capability to pre charge the nodes in one half of the cycle. The high state of and keeps and on, charging their sources up to because there is no path to ground due to the off state of the clocked transistor Since either or is on, the common node of and is also pre charged to Therefore, prior to the leading clock edge, all the capacitances in the differential tree are pre charged. The SA stage is triggered on the leading edge of the clock. If is high, node is discharged through the path turning off and on. If is high, node is discharged through the path turning off and on. After this initial change, further changes of data inputs will not affect the state of the and nodes. The inputs are decoupled from the outputs of the SA forming the base for the flip-flop operation of the circuit. The output of the SA, which is forced low at the leading edge of the clock, becomes floating low if the data changes during the high clock pulse. The additional transistor Allows static operation, providing a path to ground even after the data is changed. This prevents the potential charging of the low output of the SA stage, due to the leakage currents. Those currents cannot be neglected in low-power designs where the is lowered. performance affected by the scaling of the supply voltage. However, the additional. Transistor forces the whole differential tree to be pre charged and discharged in every clock cycle, independent of the state of the data after the leading edge of the clock. The additional transistor is minimized, to prevent a significant increase in delay of the SA stage, due to the simultaneous discharging of both the direct path capacitive load and the load of the opposite branch. This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic. It uses single-phase clock, and has small clock load. Its first stage assures accurate timing, due to its SA topology, which is very important at high operating frequencies.

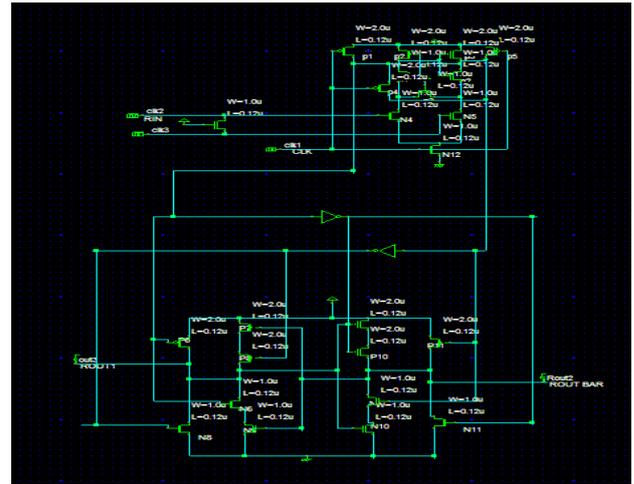


Figure.4 Sense Amplifier

6.2 Symmetric Slave Latch

The SR latch of the SAFF, shown in Figure 4 operates as follows: Input S bar is a set input and R bar is a reset input. The low level at both S bar and R bar node is not permitted and that is guaranteed by the SA stage. The low level at S bar sets the output Q to high, which in turn forces to Q bar low. Conversely, the low level at R bar sets the Q bar high, which in turn forces Q to low. Therefore, one of the output signals will always be delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays. Additionally, the delay of the true Q output, depends on the load on the complementary output Q, and vice versa. This limits the performance of the SAFF.

7. SIMULATION RESULT FOR SENSE AMPLIFIER

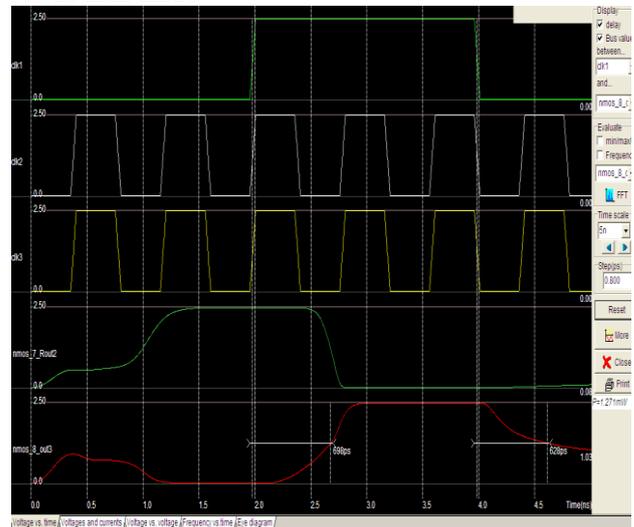


Figure 5 Simulation Result for Sense Amplifier

8. TEST BENCH FOR SENSE AMPLIFIER

By observing the differences in outputs between the pairs of flip-flops, the unknown values of inverter delays and sums of setup time, delays can be measured. At cycle times which are long enough for both flip-flops to successfully capture the data, the output waveforms at two flip-flops following the

chains that differ in one inversion are out of phase as expected from Figure. 6, and shown in Figure..7

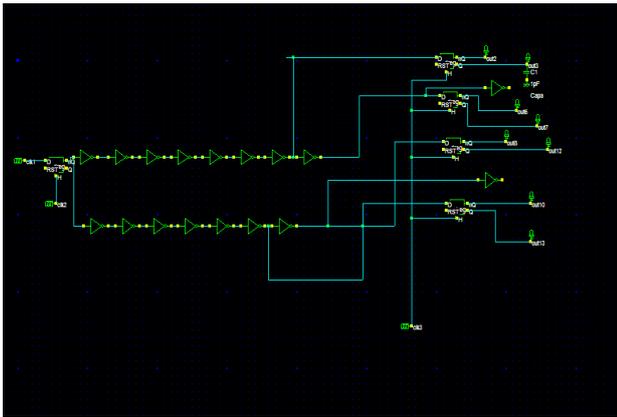


Figure 6. Test Bench For Sense Amplifier

9. SIMULATION RESULT FOR TEST BENCH OF SENSE AMPLIFIER

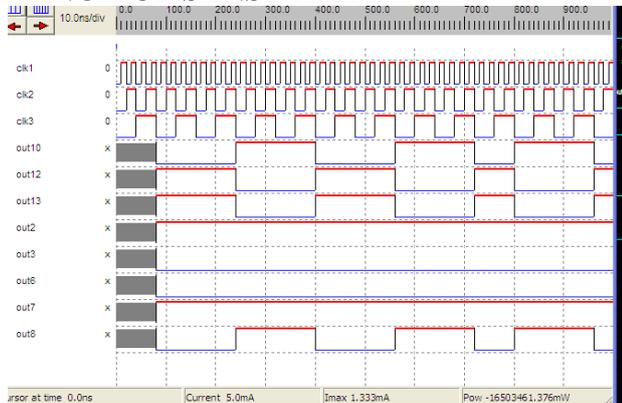


Figure7. Simulation Result for Test Bench

As the clock frequency increases, the flip-flop that follows the longer inverter chain fails to capture the data due to setup violation, as observed in Figure.7. With further shortening of the clock cycle the signal propagating through the longer inverter chain does not arrive in time, however, the flip-flop will at some point start to successfully capture the pervious value of the signal. The capturing of that pervious signal value by the flip-flop will be stabilized only after the signal arrives after the hold-time window of the flip-flop, thus avoiding the hold-time violation. Capturing of the pervious value of the data produces the same waveform as the output of the flip-flop receiving inverter chain path containing one inversion less, as shown in Figure. 7.

10. TEST BENCH FOR SENSE AMPLIFIER WITH LOAD INVERTER & CAPACITOR

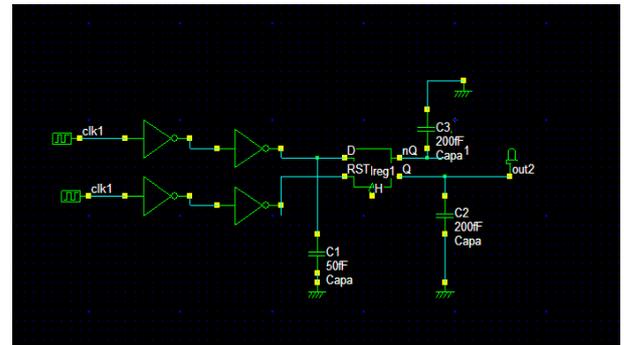


Figure 8: Test Bench for Sense Amplifier With Load Inverter & Capacitor

Simulated and measured data is summarized in Table 3. The measured results show a very good agreement with the simulation, which testifies not only to the accuracy of the post-layout simulation but a validity of described method for measuring flip-flop parameters as well. The accuracy of our measurement lies within 30 ps in both and directions. In order to measure the flip-flop performance, a simple test structure was implemented on the test chip shown in Figure 8. The minimum delay between the latest point of data arrival and output transition is measured indirectly, using the structure from Figure. 6.8. Several chains of inverters as depicted in Figure.8 were implemented. The measurement results were averaged over a set of sample chips obtained from the test run. The test chip contained a time-base generator, which allowed wide variation of clock frequency. The clock frequency was raised until one of the flip-flops receiving signal from a chain of inverters failed. The time period corresponding to the failing clock frequency was calculated and entered into a set of equations describing the timing relationship between the flip-flop parameters and the signal delay

11. SIMULATION RESULT FOR TEST BENCH OF SENSE AMPLIFIER WITH LOAD INVERTOR & CAPACITOR:

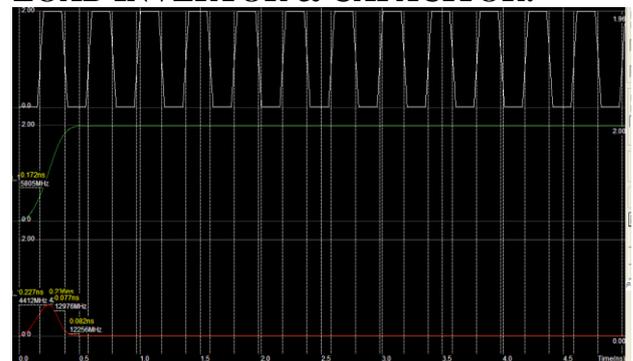


Figure.9. Simulation Result for Test Bench of Sense Amplifier With Load Invertor & Capacitor

12. PRBS

On-chip pseudo-random bit sequence (PRBS) generator implemented based on an 8-bit data generator structure. Semi-dynamic flip-flop (SDFF) is chosen for the data generator to

take advantage of its negative setup time. Pseudo random binary sequence is essentially a random sequence of binary numbers. So PRBS generator is nothing but random binary number generator. It is 'random' in a sense that the value of an element of the sequence is independent of the values of any of the other elements. It is 'pseudo' because it is deterministic and after N elements it starts to repeat itself, unlike real random sequences. The implementation of PRBS generator is based on the linear feedback shift register (LFSR). The PRBS generator produces a predefined sequence of 1's and 0's, with 1 and 0 occurring with the same probability. A sequence of consecutive $n \cdot (2^n - 1)$ bits comprise one data pattern, and this pattern will repeat itself over time. In this project, the entire design of the PRBS generator was implemented using DSCH and the simulation were done and tested on the MICROWIND simulator.

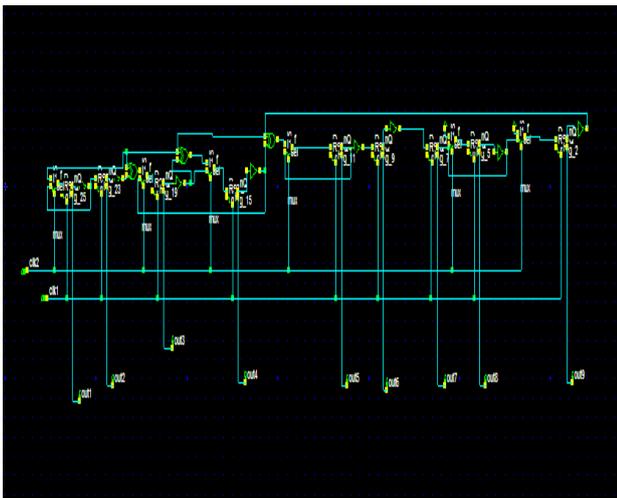


Figure :10 Pseudo Random Bit Sequence Generator



Figure :11: Simulation in DSCH

13. SIMULATION RESULT FOR PRBS

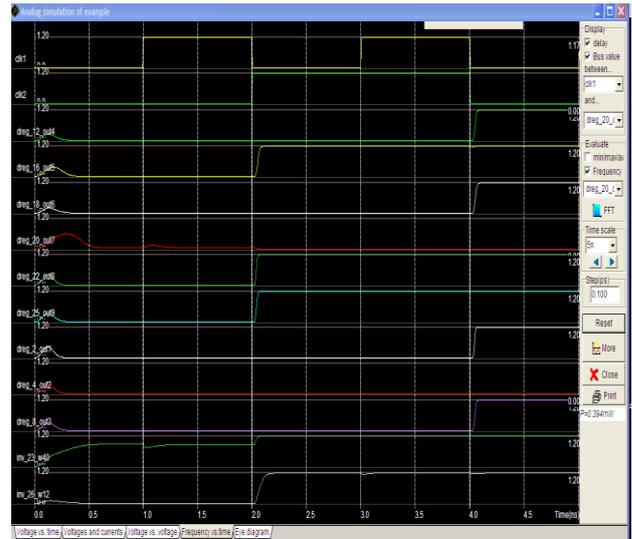


Figure :12 Simulation Result For PRBS

On-chip pseudo-random bit sequence (PRBS) generator implemented based on an 8-bit data generator structure as shown above. Characteristics Of Output Stream: By definition, the period of an LFSR is the length of the output stream before it repeats. Besides being non-repetitive, a period of a maximal length stream has other features that are characteristic of random streams.

13.1 Sums of Ones and Zeroes.

In one period of a maximal length stream, the sum of all ones will be one greater than the sum of all zeroes. In a random stream, the difference between the two sums will tend to grow progressively smaller in proportion to the length of the stream as the stream gets longer. In an infinite random stream, the sums will be equal.

13.2 Runs of Ones and Zeroes.

A run is a pattern of equal values in the bit stream. A bit stream like 10110100 has six runs of the following lengths in order: 1, 1, 2, 1, 1, 2.

One period of an n-bit LFSR with a maximal length tap sequence will have $2(n-1)$ runs (e.g., a 5 bit device yields 16 runs in one period). 1/2 the runs will be one bit long, 1/4 the runs will be 2 bits long, 1/8 the runs will be 3 bits long, etc., up to a single run of zeroes that is n-1 bits long and a single run of ones that is n bits long. A random stream of sufficient length shows similar behavior statistically.

13.3 Shifted Stream.

Take the stream of bits in one period of an LFSR with a maximal length tap sequence and circularly shift it any number of bits less than the total length. Do a bitwise XOR with the original stream.

A random stream also shows this behavior. One characteristic of the LFSR output not shared with a random stream is that the LFSR stream is deterministic. Given knowledge of the present state of the LFSR, the next state can always be predicted

14. PRBS+PREEMPHASISCIRCUIT+SENSE

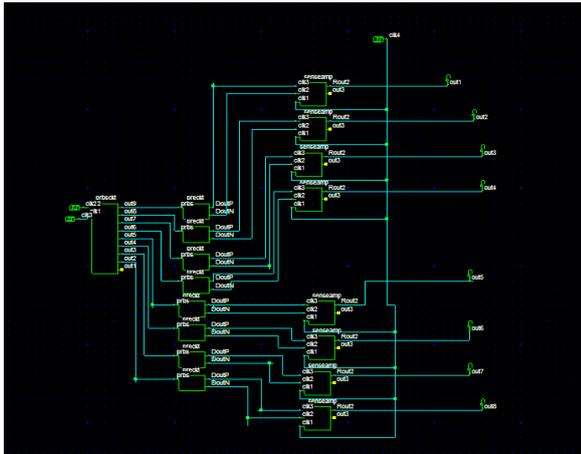


Figure:13:Prbs+Preemphasiscircuit+Sense

The output of the prbs+preemphasis circuit+sense amplifier is shown in above Figure 13.

The clock load of a typical static DFF is already equal to four minimum size inverters and a dynamic flip-flop with more clock load has to be used at the high speed. A 127-bit Pseudo-Random Binary Sequence (PRBS) input. The measurement results at the receiver input are shown in Figure :13, simple interconnect with no repeater (left), interconnect with one repeater (middle), and interconnect with driver pre-emphasis (right). A data pattern is used for the waveform measurement to show inter-symbol interference (ISI) and the PRBS input is used for the eye diagram measurement. At 2Gb/s, the simple interconnect has severe ISI, resulting in eye closure. The interconnect containing repeater reduces ISI by boosting the whole signal, while the interconnect using driver pre-emphasis does this by attenuating the low-frequency signal components. Both approaches increase bandwidth, but driver pre-emphasis saves power. An interconnect delay latency of 720ps is measured and matches the simulation results.

15. SIMULATION RESULT FOR PRBS+PRE+SA

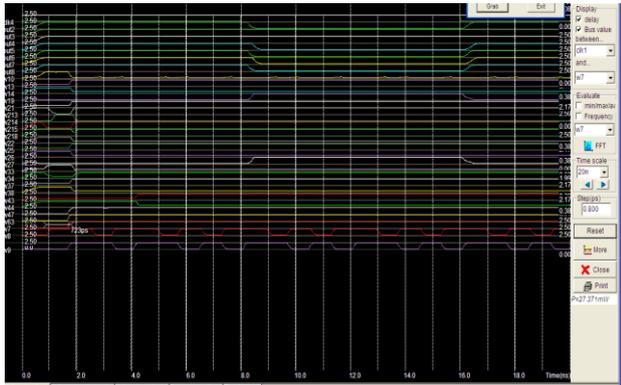


Figure 14 Simulation Result For Prbs+Pre+Sa:

To transmit 2Gb/s signal on the previous analyzed interconnect, a driver pre-emphasis circuit is designed based on the architecture proposed in Figure 14.

16. Pre Emphasis Output (Driver Side)

Driver side output is shown in above Figure 15 Current-mode signaling can be used to provide higher interconnect bandwidth]. For the current-sensing circuit architecture shown in Figure 15 a static current path always exists between the driver and receiver stages even if there is no data activity on the interconnect. To compensate for this static current, we propose to use a pair of differential interconnects with a bridge resistor termination R signaling. The current return path is well-defined in a differential structure and it reduces the impact of inductive effects. Besides, the combination of driver pre-emphasis, current-mode sensing, and differential signaling increase interconnect channel bandwidth and allow for narrow and resistive interconnects. It therefore dominates inductive effects.

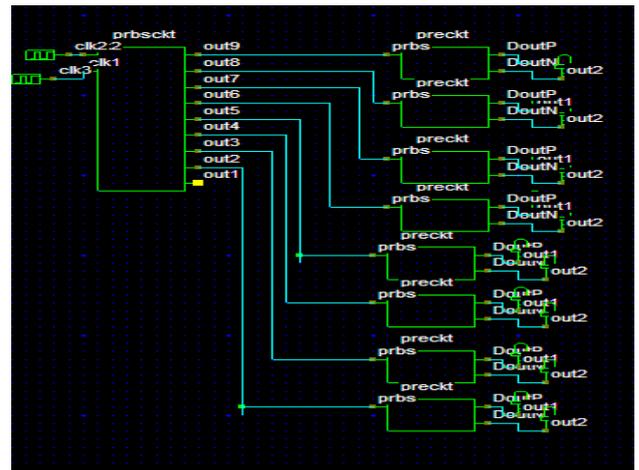


Figure: 15:Pre Emphasis Output(Driver Side)

17. Simulation Result for Driver Side Output

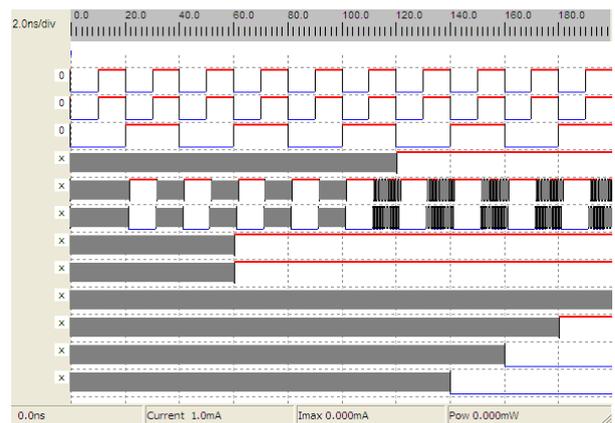


Figure:16 Simulation Result For Driver Side Output:

Both the attenuation and overdrive are the by-products of driver pre-emphasis, which de-emphasizes the low frequency component of signal to reduce inter-symbol interference (ISI) and improve bandwidth.

18. COMPLETE DESIGN OF 32GB/S

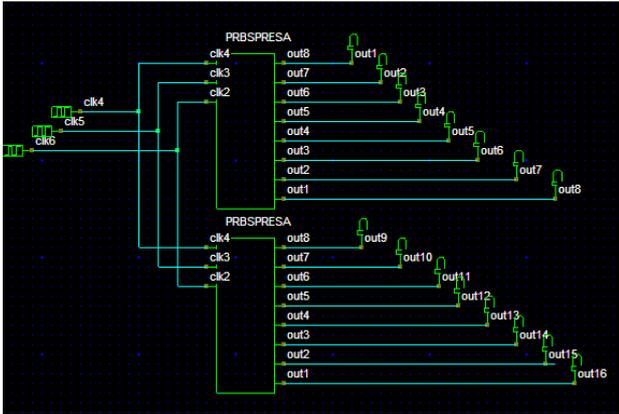


Figure:17 Complete Design Of 64Gb/s(future work)

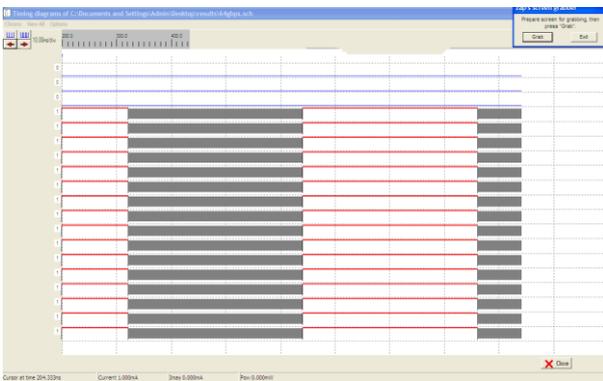


Figure:18 simulation output of the 64gb/s.

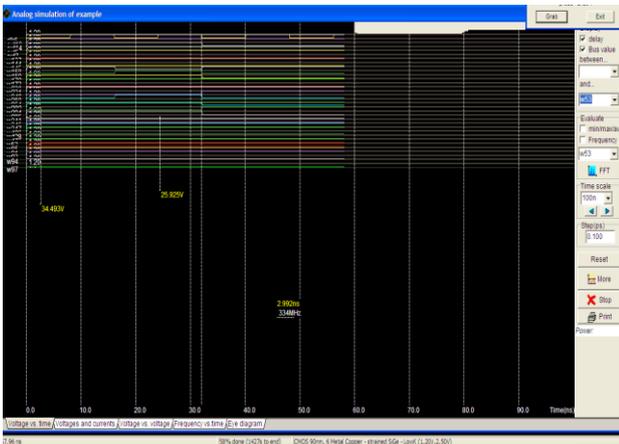


Figure 19: voltage vs time for 64gb/s circuit

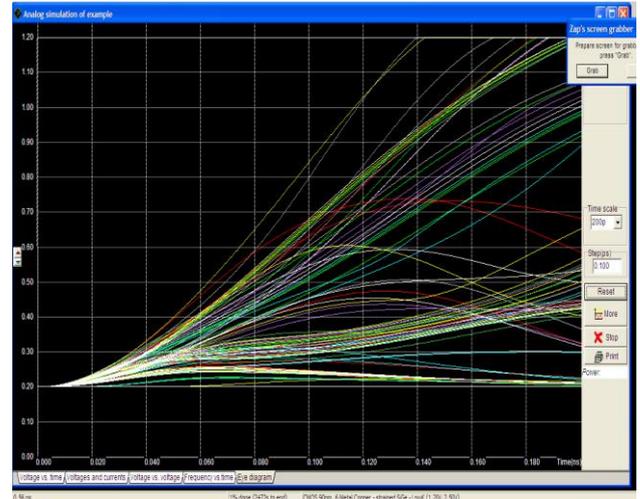


Figure 20:eye diagram.

The signal swing on the bridge resistor is limited by the sensibility of the sense-amplifier receiver. The driver size is decided by the targeted data rate the static current overhead, 2Gb/s and 1.6mA in this case.

19. CONCLUSION

Delay, power, area, and noise are all important performance metrics in on-chip signaling methodologies. This project explored and applied communication and circuit techniques to on-chip signaling while achieving various design tradeoffs. Similar to the optimization of SRAM designs, delay and power performances there were also improved by trading off signal swing and noise margin, while a degradation of these metrics was allowable within a confined domain of global busses where noise levels were tightly controlled by circuit techniques and bus structures.

20. FUTURE SCOPE:

Here we are using the pre emphasis signaling with 2Gb/s signaling capacity. But the actual capacity of pre emphasis signaling is up to 7 Gb/s. By using this parameter we can redesign for the 64 Gb/s bus

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