Design of GDI based 4-Bit Multiplier using Low Power Adder Cells

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ABSTRACT
Gate Diffusion input (GDI) a new technique of designing low-power digital combinational circuit is described. This technique allows reduction in power consumption, transistor count, propagation delay and area of digital circuits. This approach allows implementation of a wide range of complex logic functions using only two transistors. GDI proposes and compared with traditional CMOS. Comparison of GDI transistor count with CMOS is presented. . Simulation result shows that the propose GDI has better performance in terms of power consumption and transistor count in compared to CMOS design. In our paper, we designed the 4*4 array multiplier based on GDI and the simulations are performed by CADENCE VIRTUOSO based on 180nm CMOS technology with the supply voltage of 0.7V.

Keywords
Gate Diffusion Input, CMOS, Full Adder, Low power, Multiplier.

1. INTRODUCTION
With expeditious development of VLSI applications such as DSP, image, video processing and microprocessors extensively use logic gates and arithmetic circuits. Recently, building low power VLSI System has emerged as highly in demand because of the fast growing technology in mobile communication and computation. The demand for increasing speed, compact implementation and low power dissipation triggers numerous research efforts. To improve the performance of logic circuits, once based on traditional CMOS technology, resulted in the development of many logic design techniques during the last two decades. To reduce the power consumption different CMOS logic design techniques like CMOS complementary logic, Pseudo nMOS, Dynamic CMOS, Clocked CMOS logic (CMOS), CMOS Domino logic, Cascade Voltage switch logic (CVSL), Pass Transistor Logic (PTL) have been proposed[1].

One form of logic that is popular for in low-power digital circuits is PTL. The advantages of PTL over standard CMOS design are

i) High speed, due to small node capacitances.
ii) Low power dissipation, as a result of reduced number of transistors.
iii) Lower interconnection effect, due to smaller area.

PTL: In Pass Transistor logic only pull-down network is used. The input signals are applied to both the gate and drain/source terminals. However, most of the PTL implementations have two basic problems. First, the threshold drop across the single-channel pass transistors results in reduced current drive and hence slower operation at reduced supply voltages; this is particularly important for low-power design since it is desirable to operate at the lowest possible voltage level. Second, since the "high" input voltage level at the regenerative inverters is not VDD, the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant.[2]

There are many sorts of PTL techniques that intend to solve the problems mentioned above.

i) Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using a small number of complementary transistors. It solves the problem of low logic level swing by using pMOS as well as nMOS.

ii) Complementary pass-transistor logic (CPL) features complementary inputs/outputs using nMOS pass-transistor logic with CMOS output inverters. CPL's most important feature is the small stack height and the internal node low swing, which contribute to lowering the power consumption. The CPL suffers from static power consumption due to the low swing at the gates of the output inverters. To lower the power consumption of CPL circuits, LCPL and SRPL circuit styles are used. Those styles contain pMOS restoration transistors or cross-coupled inverters (respectively).

iii) Double pass-transistor logic (DPL) uses complementary transistors to keep full swing operation and reduce the dc power consumption. This eliminates the need for restoration circuitry. One disadvantage of DPL is the large area used due to the presence of pMOS transistors.

An additional problem of existing PTL is top-down logic design complexity, which prevents the pass transistors from capturing a major role in real logic LSIs. One of the main reasons for this is that no simple and universal cell library is available for PTL-based design. This paper proposes a new low-power design technique that allows solving most of the problems mentioned above using gate diffusion input (GDI) technique. This method is useful for design of fast, low-power circuits, using a reduced number of transistors.

The Section 2 presents GDI functions and their principle. In Section 3 and 4 describes transient analysis of AND, EXOR gates. Section 5 describes Novel 6T Full Adder. Section 6 describes 4 bit multiplier design. Section 7 describes comparison of GDI with CMOS. Comparisons of some basic logic functions and high-level combinational circuits designed in CMOs and GDI are discussed.

2. GDI FUNCTIONS

The GDI method is based on the use of a simple cell as shown in Fig. 1. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.

1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

It must be remarked that not all the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (**SOI**) technologies.

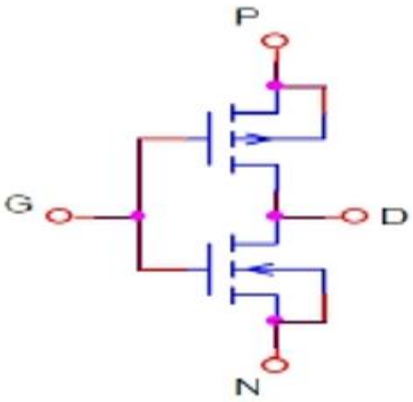

Fig.1 GDI Basic Cell

Table 1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions.

Most of the functions are complex in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method.

Table 1.Various Logic Functions of GDI cell for different input configurations.

N	P	G	D	Function
0	B	A	$\overline{A}$	F1
B	1	A	$\overline{A}$ +B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
0	1	A	$\overline{A}$	NOT

TRANSIENT ANALYSIS OF AND GATE USING GATE DIFFUSION INPUT (GDI)

GDI AND gate requires only two transistors to design the circuits. Here A is taken as input voltage for the terminal G, B is taken as input voltage for the terminal N. The P terminal is kept at logic 0. The output is taken at the terminal D. GDI AND Gate is shown in Fig 2.1. Transient analysis of AND gate is shown in Fig 2.2

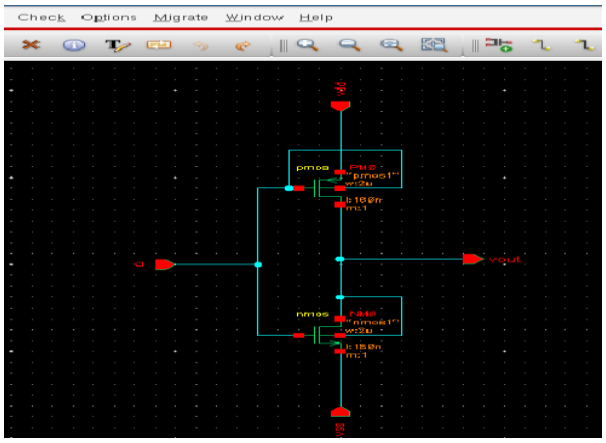

Fig 2.1: GDI AND Gate

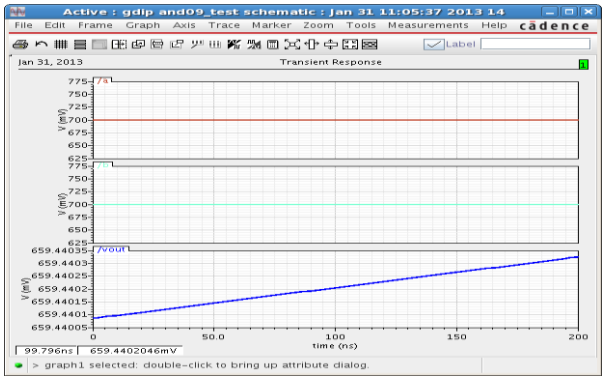

Fig 2.2: Transient analysis of AND Gate

GDI EXOR GATE

EXOR function is the key variable in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. The GDI EXOR gate requires only four transistors. The propose GDI EXOR gate use less transistor when compared with CMOS counterpart. Input voltage is given as 0.7V. GDI EXOR Gate is shown in Fig 3.1 Transient analysis of GDI EXOR Gate is shown in Fig 3.2.

NOVEL 6T GDI FULL ADDER

The transistor level implementation of GDI Full Adder using six transistors is shown in Fig 4. We propose a Novel Full Adder using 6 Transistors. This full adder consists of two modules one XOR gate and a multiplexer. These Full adders use fewer transistors when compared with CMOS counterpart. Due to the advantages of GDI cell, less transistor count this circuit can achieve its benefit of low power consumption. GDI 6T Full Adder is shown in Fig 4.1. The transient analysis of GDI 6T Full Adder is shown in Fig 4.2.

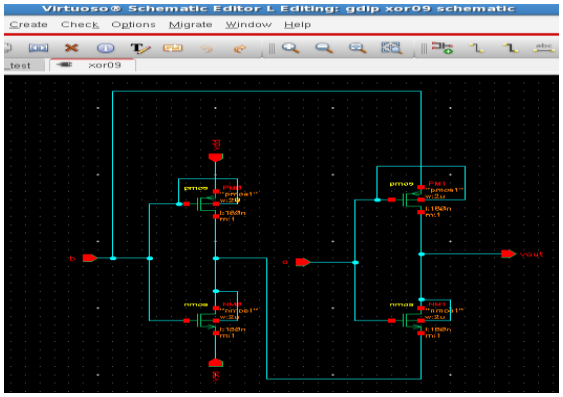

Fig 3.1: GDI EXOR GATE

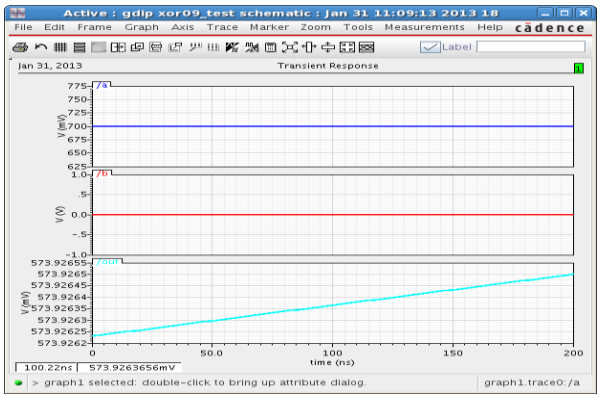

Fig 3.2: Transient Analysis of GDI EXOR Gate

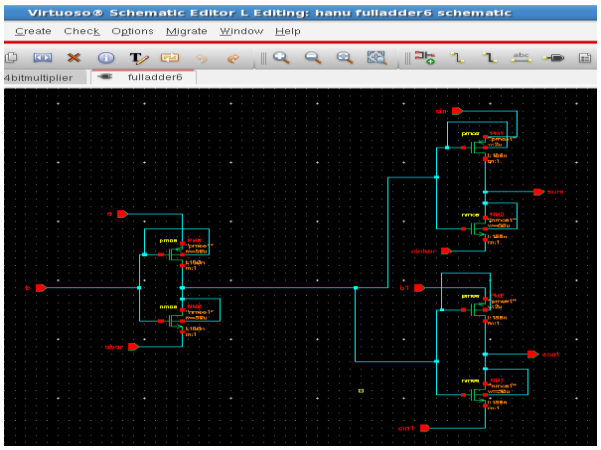

Fig 4.1: GDI 6T Full Adder

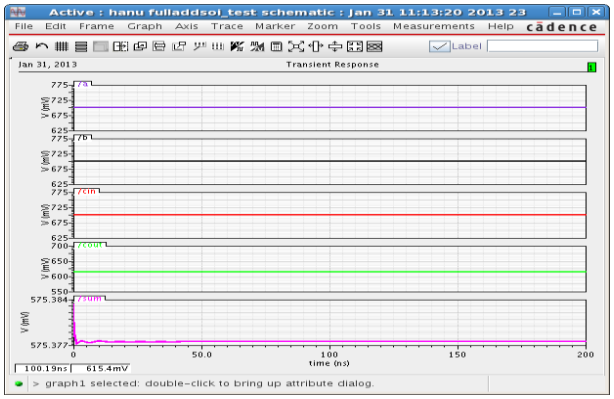

Fig 4.2 Transient Analysis of GDI Full Adder

4 BIT MULTIPLIER DESIGN

Multiplication is one of the basic functions used in various VLSI applications. The multipliers are widely used in Arithmetic and Logic Unit, DSP Processors, FIR filters, Math processors and floating point units. Present processor aim to design a low power multiplier. Different types of multipliers are available in the literature, depending upon the requirements and various companies are using different types of multipliers according to their needs. In this paper we used array multiplier. The notable characteristic about the array multiplier is its regular structure shown in fig 5(a). An n bit Array multiplier has n x n array of AND gates can compute all the aibi terms simultaneously. The terms are summed by an array of "n x (n-2)" full adders and "n" half adders[6].

The Block Diagram of 4*4 bit array multiplier is shown in Fig 5.1. The 2*2schematic are shown in 5.2 and the simulation results are shown in 5.3.The 4*4Schematic are shown in 5.4 and the simulation results are shown in 5.5.1, 5.5.2, 5.5.3.

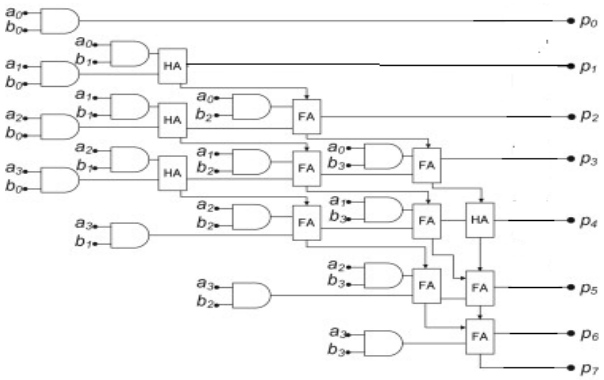

Fig 5.1 Block diagram of 4*4 bit array multiplier

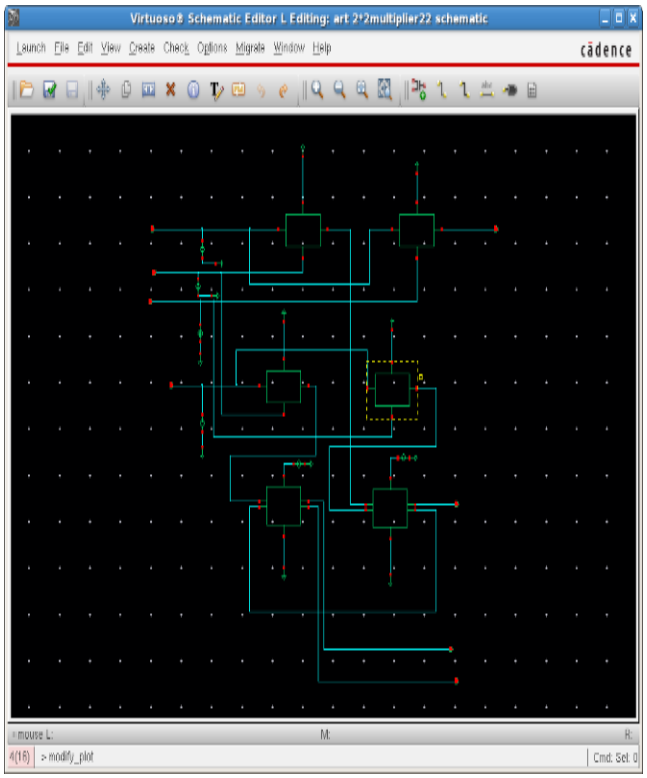

Fig 5.2 2*2 Multiplier Schematic

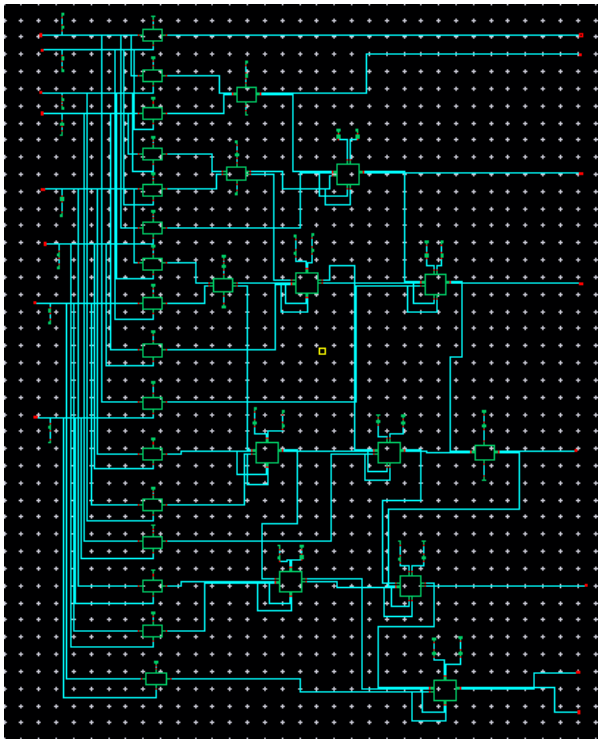

Fig 5.4 4*4 Multiplier Schematic

Fig 5.5.1

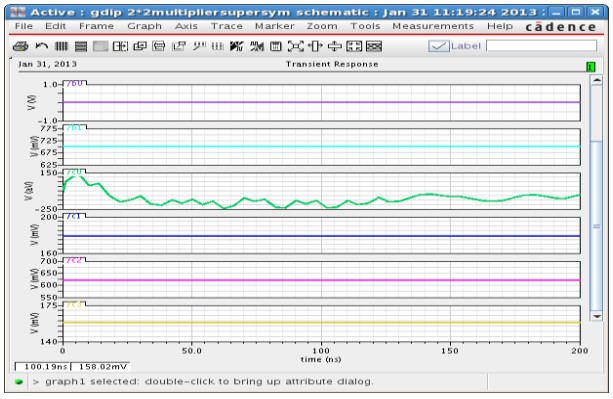

Fig 5.3 2*2 Simulation results

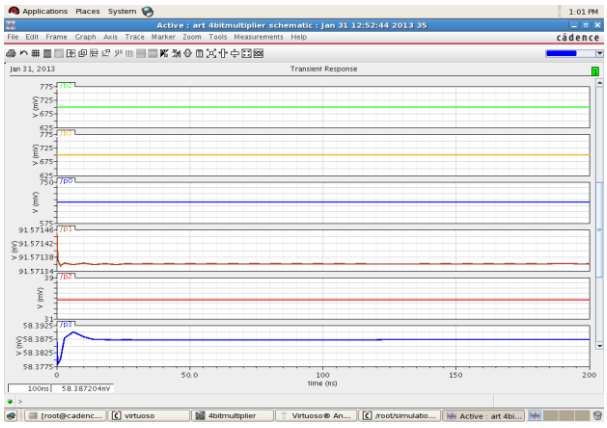

Fig 5.5.2

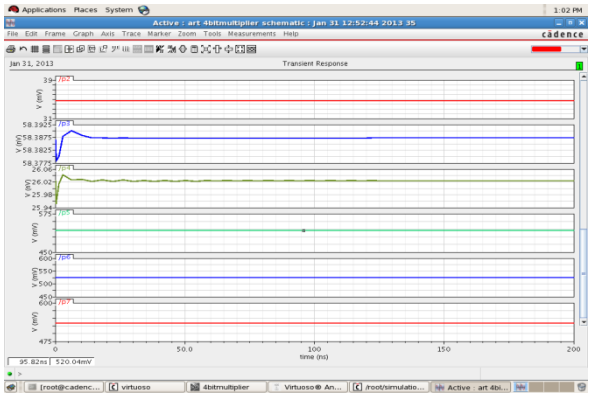

Fig 5.5.3: 4*4 Simulation results

5. COMPARISON OF GDI WITH CMOS

In this work a variety of function have been implemented in 180nm technology, to compare the Gate Diffusion Input (GDI) technique with CMOS. GDI circuits were designed at the transistor level in an 180nm SOI CMOS process technology. The circuits were simulated using Cadence Design Tool. Table 2 is the comparison of transistor count of GDI and CMOS. Fig 6 shows the Schematic comparison of GDI with CMOS.

Table 2. Transistor count of GDI and CMOS

FUNCTION	TRANSISTOR COUNT	
	GDI	CMOS
AND	2	6
XOR	4	12
HALFADDER	6	18
FULLADDER	6	42
2*2	20	60
4*4	104	504

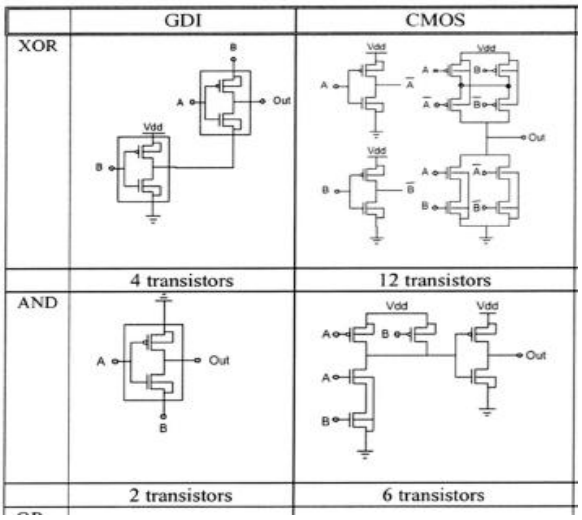

Fig 6 Schematic comparison of GDI and CMOS

6. CONCLUSION

It has been observed that GDI is most effective in terms of transistor count as it requires less no of transistors and has least power consumption. The advantage of GDI technique is two transistor implementation for complex logic function. This together with positive measurement and simulation results, provide evidence that the GDI design might enrich the toolbox of VLSI designers.

7. REFERENCES

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