TFET based Ternary Logic Gates & Arithmetic Circuits

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ABSTRACT
Scaling of conventional CMOS devices has reduced the device dimensions from 10 mm in 1970s to 0.1 µm in a present day. According to ITRS (i.e. International Technology Roadmap for Semiconductors) we are going to face the brick wall in 2015 if we continue in the same development speed. This will not be possible for us to maintain the pace forecasted by Moore.(Moore's law) This is because of the fundamental limitations of device parameter dimensions due to which performance is degrading in several ways.
To overcome this and go ahead in technology , one must look into new devices those can be scaled down to come up with other solutions. Either it should be possible to go ahead by again reducing the device dimensions in some way or we have to reduce the circuit overhead with less complexity. Solution to this might be : MVL i.e. Multivalued Logic & TFET i.e. Tunnel Field Effect Transistor.[1]This report presents a novel design of Ternary Logic Gates & arithmetic circuits using TFET

General Terms

µm (micrometer), mm (millimeter)

Keywords
CMOS, ITRS, TFET, MVL.

1. INTRODUCTION

A.CMOS technology

The current technology trend is CMOS technology which is referred as Complementary Symmetry Metal Oxide Semiconductor or COSMOS. From the words ' complementary symmetry ' , it is clear that , CMOS uses complementary as well as symmetrical pairs of p-type & n-type MOSFETS for logical function implementation.CMOS technology implements all the digital circuits with the main principle that , they use both p-type & n-type MOSFETs to create a path from input to output through voltage source (Vdd) or ground (Vss). (see fig.1).MOORE's law states that ,(see fig. 2) number of transistors per particular chip are going to get doubled at every two years approximately. As stated by MOORE , we are scaling the CMOS devices for further optimization & energy conservation . But now CMOS technology has reached its optimum limit & thus going to face the brick wall in around 2015 if we continue the same way . this is because , scaling down is limited due to certain constraints like power dissipation , degradation in switching performance etc. The main reasons are as stated below :

1. Difficulty in OFF current suppression .
2. Difficulty in increase in ON current .
3. Difficulty in decreasing the gate capacitance.
4. Increase in production & development cost.

B . Limitations of CMOS technology:

Basically for switching purpose we use BJTs or MOSFETs . These are the ideal characteristics (see fig. 3) if a CMOS switch which shows abrupt transition from one state to another state. (ON – OFF state). Practically the electronic devices so far do not exhibit such behavior. The term 'Figure of Merit ' is used to realize such behavior. This is the ratio of ON to OFF current . many factors are responsible to degrade the Figure of Merit including ' **Short Channel Effects '.**[2] These are listed below:

1. Sub threshold swing .
2. Drain induced barrier lowering (DIBL) .
3. Channel length modulation.
4. Velocity saturation.
5. Gate oxide leakage.
6. Gate induced drain leakage.
7. Hot carrier effect.
8. Statistical fluctuations of dopant atoms.

C. Remedies to limits of CMOS technology(ITRS roadmap)

At this moment, there are no candidates among the so-called „beyond CMOS" or „Post Si" new devices, which are believed to really replace CMOS transistors usable for the products of highly integrated circuits within 20 years. Still we need to continue CMOS based transistors with „More Moore" approach with combining that of „More than Moore." Then, „More Moore" approach is after we reach the downsizing limit or with no more decrease in gate length. Because the number of the transistors in a chip is limited by the power consumption, we could continue the „More Moore" law for certain period by replacing current CMOS transistors by nanowire or nanotube MOSFETs with which the suppression of off-leakage current and increase of on-current under low voltage could be realized because of its nature such as quasi-one-dimensional conduction.[3]

Beyond CMOS, several completely new approaches to information-processing and data-storage technologies and architectures are emerging to address the timeframe beyond the current roadmap. Rather than vying to "replace" CMOS, one or more of these embryonic paradigms, when combined with a CMOS platform, could extend microelectronics to new applications domains currently not accessible to CMOS. [5] (see fig.4)

2. THE TUNNEL FIELD EFFECT TRANSISTOR (TFET)

One of the device people are looking at, to overcome SCEs of MOSFET is the Tunnel Field Effect Transistor (TFET). In this section we try to briefly explain the working principle of the device. The basic principle of operation of the device is based on the band-to-band tunneling mechanism similar to the one explained in section 1.2.6. A version of lateral TFET is shown in Fig.8, is basically an SOI (Silicon on Insulator) having a P+ source and an N+ drain the region between these two is the channel which is kept intrinsic. However, various other structures are there in literature, we use the one shown in Fig.8 only for the sake of simplicity in explaining the basic operating principle.[4][5]

The p-i-n structure (see fig. 5) is usually reverse biased between source and drain terminals. Gate is the terminal which controls the source to drain current of the device. For n-channel operation, the gate is driven with positive voltage and inversion region is formed in the channel which consists of a n-type carriers. When sufficient amount of inversion region is formed, the source and the inverted channel form a P+N+ tunneling junction. Tunneling of carriers takes place between the valence band of the P+ source and conduction band of the inverted channel. The tunneling width and hence the amount of tunneling current is controlled by the gate . Since this is a reverse biased p-i-n structure, we see a very small amount of leakage current when no gate bias is applied. Since the device is based on tunneling mechanism and for silicon tunneling does not take place for widths greater than 10nm, the device can be scaled down to 10nm regime. (see fig. 6)

3.THE TERNARY LOGIC (MVL)

Ternary Logic is the subset of MVL & a most promising alternative to binary logic design. Using Ternary Logic, it is possible to accomplish simplicity & energy efficiency in modern digital design.Traditionally, digital computation is performed on two valued logic ; that is there are only two values possible : True & False. Ternary Logic has attracted considerable interests due to it's potential advantage over the binary. For example - 1). It is possible to achieve simplicity & energy efficiency since the logic reduces complexity & chip area. 2) Serial & parallel arithmetic operations can be carried fast if Ternary Logic is employed.[6][7]Ternary Logic functions are defined as functions having significance if third value is introduced to binary logic i.e. 0 , 1 , 2 which represent True , Undefined , False respectively. Basic gates & arithmetic circuits can be designed using TFETs.

The basic operations of ternary logic can be defined as follows.

Xi,Xj = {0, 1, 2}

Xi + Xj = max{Xi,Xj }

Xi - Xj = min{Xi,Xj }

Xi = 2−Xi

Here ' –' denotes the arithmetic subtraction , the operations '+' & '·' are referred to as the OR ,AND & NOT in ternary logic resp. The fundamental gates in the design of digital systems are the inverter , NOR gate & NAND gate. [8][9]

A.Ternary Inverter:

A general ternary inverter (see table 1) is an operator with one input x & three outputs y0 ,y1, y2 such that

$$y_0 = C_0(x) = \begin{cases} 2, & \text{if } x = 0 \\ 0, & \text{if } x \neq 0 \end{cases}$$

$$y_1 = C_1(x) = \overline{x} = 2 - x$$

$$y_2 = C_2(x) = \begin{cases} 2, & \text{if } x \neq 2 \\ 0, & \text{if } x = 2. \end{cases}$$

Thus the implementation requires three inverters i.e. negative ternary inverter (NTI) standard ternary Inverter (STI) & positive ternary inverter(PTI)(see table 2).

B.Ternary NAND & NOR gates:

The ternary NAND and NOR (see table 3) are two multiple entry operators used in ternary logic. The functions of the two-entry ternary NAND and NOR gates are defined by the following two equations, respectively .

YNAND = min{X1,X2}

YNOR = max{X1,X2}.

C. Basic Ternary Arithmetic Circuits:

The ternary gates can be used for designing ternary arithmetic circuits such as ternary adders and multipliers. As required for these circuits, a new design of the ternary decoder is presented (see fig 7) The ternary decoder is a one-input, three-output combinational circuit and generates unary functions for an input *x*. The response of the ternary decoder to the input *x* is given by

$$X_k = \begin{cases} 2, & \text{if } x = k \\ 0, & \text{if } x \neq k \end{cases}$$

where *k* can take logic values of 0, 1, or 2. The decoder consists of a PTI gate, two NTI gates, and a NOR gate, (see fig 7). One of the main advantages of ternary logic is that it

reduces the number of required computation steps. Since each signal can have three distinct values, the number of digits required in a ternary family is log3 2 times less than required in binary logic. Therefore, if we consider an *N*-bit binary adder, then the corresponding ternary adder has _log3 2*N*_ digits, where [x] represents the integer nearest to *x* and greater than *x* (i.e., the ceiling function).[8]

D. Ternary Half Adder:

A ternary half adder is shown below along with its truth table.(see table 4). HA can be derived from the Karnaugh map (see table5) as

Sum=*A*2*B*0+*A*1*B*1+*A*0*B*2+1 • (*A*1*B*0+*A*0*B*1+*A*2*B*2)

Carry = 1• (*A*2*B*1 + *A*2*B*2 + *A*1*B*2)

where *Ak* and *Bk* denote the output of the inputs *A* and *B* from the decoder shown in Fig. 7. The schematic diagram of the HA is shown in Fig. 8. Two decoders generate the unary output signals for inputs *A* and *B*, while the logic gates (such as ANDs and ORs) compute the functions given by above equations . The so-called *T* buffer of Fig. 8 represents a level shifter and its logic function is given by

$$\text{Out} = \begin{cases} 1, & \text{if in} = 1, 2 \\ 0, & \text{if in} = 0 \end{cases}$$

where 'in' is the input of the *T* gate and 'Out' is the output of the *T* gate.

4.CONCLUSION:

In this paper different scaling issues regarding CMOS technology are presented. The novel solution of Tunnel FET is presented along with its basic principle and operating characteristics. The MVL is another remedy across the limitations of conventional CMOS technology.

The basic design of Ternary invertors is given. Ternary decoder along with basic ternary logic gates are discussed . finally, the ternary arithmetic circuit i.e Half Adder is explained using truth tables , K-maps and respective equations in detail. Different simulation results can show the exact working principle and characteristics at respective instant.

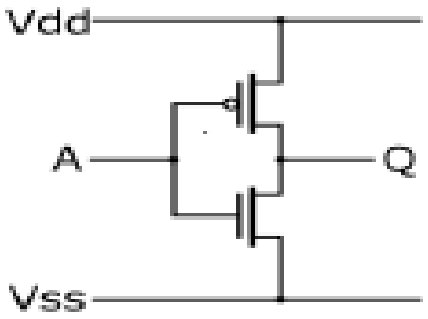

Fig 1 : CMOS Inverter

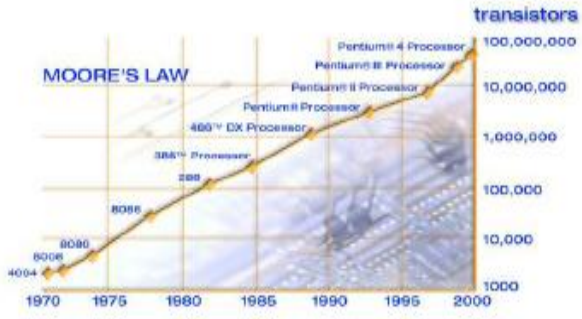

Fig 2 : Technology advancement

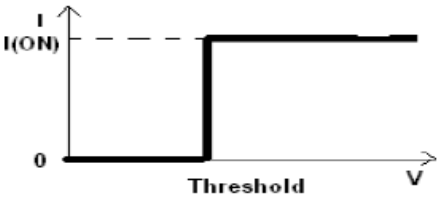

Fig 3 : Ideal characteristics of CMOS switch

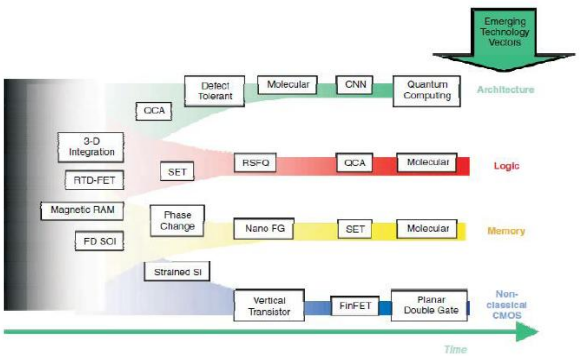

Fig 4 : ITRS roadmap for emerging technology sequence

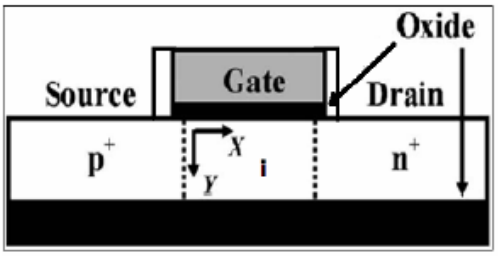

Fig. 5: A lateral TFET Structure

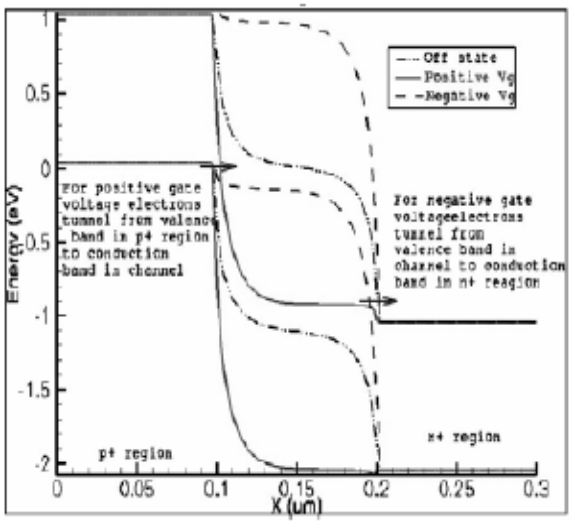

Fig. 6: Band diagram describing the n-channel and p-channel operation of TFET

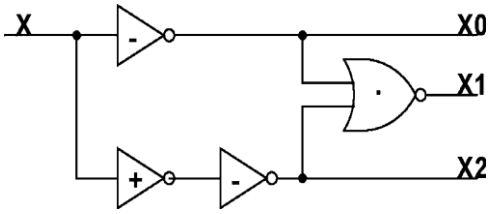

Fig 7 : Ternary decoder

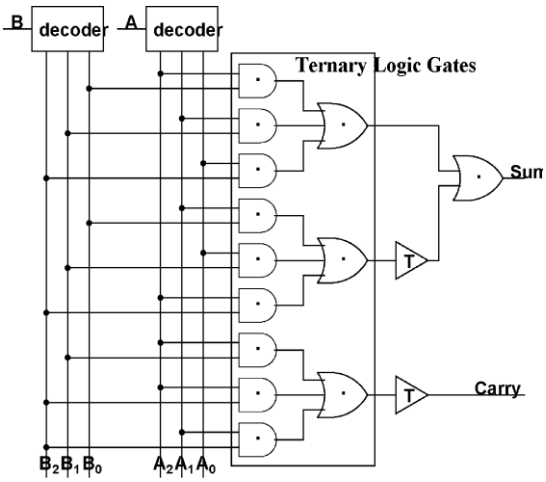

Fig 8 : Ternary Half Adder

Table 1 : Logic Symbols

Voltage Level	Logic Value
0	0
1/2 V_{dd}	1
V_{dd}	2

Table 2 : Truth tables of STI , PTI & NTI

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 3 :Truth table of Ternary NAND & Ternary NOR

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

Table 4 : Truth table of HA

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	1	2	0
1	2	0	1
2	2	1	1

Table 5 : Karnaugh map of HA

Sum

A/B	0	1	2
0		1	2
1	1	2	
2	2		1

Carry

A/B	0	1	2
0			
1			1
2		1	1

5.REFERENCES

[1] A. Lin, N. Patil, K. Ryu, A. Badmaev, L. G. De Arco,C. Zhou, S. Mitra, and H.-S. P. Wong, "Threshold voltage and on–off ratio tuning for multiple tube carbon nanotube FETs," IEEE Trans. Nanotechnol., vol. 8, no. 1, pp. 4–9, Jan. 2009.

[2] Daniel Rairigh, "Limits of CMOS Technology Scaling and Technologies Beyond-CMOS", IEEE, Nov. 21, 2009 .

[3] Robert R McCormick school of engineering and applied science, "Nanoscale cmos", Department of material science, Northwestern university, USA, 2009.

[4] Low power CMOS circuit design : by Kaushik Roy

[5] S. Thompson, P. Packan, and M. Bohr, "MOS Scaling: Transistor Challenges in the 21st Century," Source:Intel Technology Journal, v.Q3, p.1-19, 1998. http://developer.intel.com/technology/itj/q319-98/articles/art_3.htm

[6] R.S. Muller, T.I. Kamins and M. Chan, "Device Electronics for Integrated Circuits, Third Edition," John Wiley & Sons, Inc., 2003.

[7] CNTFET based design of Ternary Logic Gates & Arithmetic Circuits : by Sheng Lin, *Student Member, IEEE, Yong-Bin Kim, Senior Member, IEEE, and Fabrizio Lombardi, Fellow, IEEE.*

[8] Aspects of balance Ternary Arithmetics implemented using CMOS charged semiconducting Gate Devices: by Henning Gundersen , Institute of infermatics , University of Oslo.

[9] A Novel CNTFET-Based Ternary Logic Gate Design : by Sheng Lin, Yong-Bin Kim and Fabrizio Lombardi , Northeastern University Boston, MA, USA.