Implementation of MIMO Encoding & Decoding in a Wireless Receiver

Pravin W. Raut Research Scholar, Sr. Lecturer Shri Datta Meghe Polytechnic Nagpur Hingna Road, Nagpur S.L.Badjate Vice Principal & Professor S. B. Jain Institute of Technology, Management & Research,Nagpur

ABSTRACT

In this paper, we address the implementation of Multi-Input-Multi-Output (MIMO) Decoder embedded in a prototype of 3G / 4G Mobile receiver using FPGAs.

This MIMO decoder is part of a multi-carrier code division multiple-access (MC-CDMA) radio system, equipped with multiple antennas at both ends of the link that is able to handle up to 32 users and provides raw transmission bit-rates up to 125 Mbps.

The task of the MIMO decoder is to appropriately combine the signals simultaneously received on all antennas to construct an improved signal, free from interference, from which to estimate the transmitted symbols.

The main motto of this is to design & Implement the FPGA based MIMO Encoder and Decoder. The Data links for Two symbol period were established and found that the MIMO decoder outputs follows the MIMO Encoder input.

We report results using FPGA devices of the Xilinx family.

Keywords

FPGA, MIMO Encoder, MIMO Decoder ,Transmitter, Receiver , OFDM. antenna,

INTRODUCTION

The MIMO Decoder is a component of Mobile terminal (MT) Receiver linked with the MIMO Encoder of Mobile Base Station(BS) Transmitter. The wireless receiver is of 3G / 4G prototype. In order to investigate the real performance and feasibility of implementation of these technologies, a complete hardware demonstrator of a broadband mobile terminal (MT) has been designed and implemented. The demonstrator is focus on a MT with two antennas.

Multi-carrier CDMA, based on the serial combination of direct sequence CDMA and OFDM has been considered for the physical layer in the downlink.

The use of multiple antennas is another enabling technology for 3G / 4G systems, which helps to exploit spatial diversity, to increase capacity and to mitigate the effects of fading. In our system the space-time block code for two transmit antennas designed by Alamouti code scheme is employed.

This option has been favored over other MIMO technologies, such as beam-forming or layered space-time coding (BLAST), because it provides the maximum attainable diversity order for the number of antennas employed using a simple decoding algorithm.

To achieve good bit error rate (BER) performance, state-of the- art channel coding techniques, including duo-binary turbo codes for the uplink, and convolutional and low density parity check codes for the downlink are to be employed. The rest of the paper describes the design of the hardware module that performs MIMO decoding in the MT, and is organized as follows. In Section II a brief overview of the complete downlink system is given, where focus is on the receiver. Communication channel in MIMO system is reviewed in Section III. The basis of Alamouti code scheme is reviewed in Section IV. MIMO Encoder is reviewed in Section V. The MIMO decoding scheme and its architecture in Section VI. Tools and Implementation in section VII, and Finally the Conclusion in section VIII.

2. OVERVIEW OF THE DOWNLINK SYSTEM

2.1. Transmitting Base Station

A simplified diagram of the transmitting BS is shown in Fig. 1. Data bits to be transmitted to each active user are independently channel encoded and mapped onto symbols of the appropriate constellation (QPSK, 16-QAM or 64-QAM).

Each modulated symbol is multiplied by the spreading code of the corresponding user, and the spread symbols of the *Nu* active users are added together to be simultaneously transmitted over the same set of Sf = 32 sub carriers, which constitutes a MC-CDMA symbol. In our system the spreading factor in frequency is Sf = 32, and the number of users must be in the range $1 \le Nu \le Sf$

An OFDM symbol consists of Ns = 21 contiguous MCCDMA symbols, so that information is simultaneously transmitted over $Nd = Ns \ x \ Sf = 672$ subcarriers.

Data is prepared for multiantenna transmission by the MIMO encoding module. According to the Alamouti scheme, a pair of OFDM symbols $\{\mathbf{x}(n), \mathbf{x}(n + 1)\}$, also known as a space-time block, is transmitted employing two antennas over two consecutive symbol periods. During the first symbol period, $\mathbf{x}(n)$ is transmitted from the first antenna, and simultaneously $\mathbf{x}(n+1)$ is transmitted from the second one.

National Conference on Innovative Paradigms in Engineering & Technology (NCIPET-2012) Proceedings published by International Journal of Computer Applications® (IJCA)

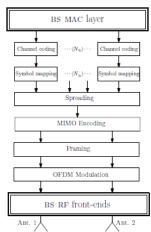


Fig. 1. Simplified diagram of the BS transmitter.

During the next symbol interval, the first antenna outputs $-\mathbf{x} \star (n$

+ 1), while the second one transmits $\mathbf{x} \star (n)$, with (.) \star standing for complex conjugate and *n* for the symbol epoch. Small bold letters denote vectors with *Nd* elements, corresponding to the number of data subcarriers in an OFDM symbol.

Before OFDM modulation, the framing module interleaves pilot symbols in the data stream, in order to aid channel estimation at the receiver. One IFFT operation per transmit antenna is required for OFDM modulation, to convert data to the time domain. The IFFT size is 1024, and the sampling rate 61.44 MHz.

Each stream of complex OFDM symbols is finally IQmodulated, power amplified by independent RF front-ends and radiated in the 5 GHz band.

2.2. Receiving Mobile Terminal

A simplified diagram of the MT receiver is depicted in

Fig. 2. Analog signals received by the two antennas of the

MT are down converted to base band by twin zero-IF RF front ends, and then sampled at 61.44 MHz. After automatic gain control (AGC) and correction of RF impairments caused by the zero-IF architecture of the front-ends, time and frequency synchronization must be performed in order to minimize misalignments with the

transmitting BS. One FFT operation per antenna branch is required to recover the symbols in the frequency domain (OFDM demodulation). Next, pilots are split from information symbols by the deframing module.

By interpolation of pilot symbols in time and frequency, the MIMO channel estimator provides the MIMO decoder with channel state information (CSI), which is combined with two contiguously received OFDM

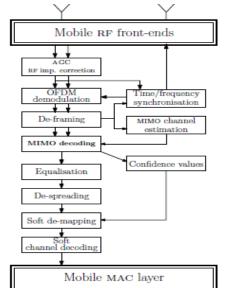


Fig. 2. Simplified diagram of the MT receiver.

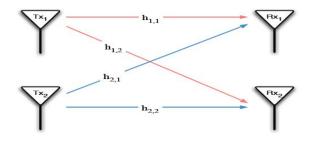
symbols to build the improved signal from which to estimate the modulated symbols. However, the output stream of the MIMO decoder further requires module equalization [6] and de-spreading (separation of users by correlation with their spreading codes) before detection of the desired user can take place. The output of the soft de-mapper is finally sent to the channel decoder to make decisions about the transmitted information bits.

3. COMMUNICATION CHANNEL IN MIMO SYSTEM

The MIMO refer to Multi-Input-Multi-Output (MIMO) antenna system. In this case we are using 2x2 MIMO system.

One possible way to improve the reliability of wireless communications is to employ diversity. Diversity is the technique of transmitting the same information across multiple channels to achieve higher reliability.

MIMO systems are able to achieve impressive improvements in reliability and capacity by exploiting the diversity offered by the multiple channels between the transmit and receive antennas. The following figure is 2×2 MIMO system, there is the potential for both transmit and receive diversity.



Receive diversity is when the same information is received by different antennas. For instance the information sent from Tx1 is transmitted across channels h1,1 and h1,2, and received by both Rx1 and Rx2. Transmit diversity is when the same information is sent from multiple transmit antennas. One possible way to achieve this is to code across multiple symbols periods. For instance, at time t antenna Tx1 could transmit the

symbol s then at time t+1 antenna Tx2 would transmit the same symbol s. The Alamouti scheme uses a method similar to this to obtain transmit diversity.

The channel capacity can be increased by increasing the bandwidth used in transmission, or to increase SNR.

Multi-Antenna systems use a rather novel approach to increase the overall capacity of a wireless communications system; use more channels. Each of the individual transmission channels is still limited according to Equation $C = B.log_2(1 + SNR)$ however the overall capacity of the system is now the sum of the capacities of the individual channels.

The transmission environment of this are the major drivers of wireless communication are mobile telephones and wireless LANs (e.g. IEEE 802.11b otherwise known as Wi-Fi), therefore it is prudent to examine the typical transmission environments in which these systems operate.

Under assumptions that the channel is "flat fading" channel, the complicated transmission environment can be mathematically represented by using complex numbers to represent the magnitude and phase change of the transmission channel.

The in-phase component is the real part of the complex representation, and the quadrature component is the imaginary part.

For a SISO system this model can reduce the entire transmission environment to a single complex number. The system can then be represented using Equation (1),

y = hx + e ------ (1)

where, h is the complex number representing the channel, x is the input signal, e is a complex number modeling the thermal noise at the receiver.

Similarly MIMO systems can be modeled with Equation (2). The variables have the same meaning as for the SISO case, however instead of the scalar complex numbers in Equation (1), the variables are matrices of complex numbers.

Y = HX + E ----- (2)

4. THE ALAMOUTI CODE

The coding scheme used for MIMO is an Alamouti code. Alamouti Code is belong to a class of Space-Time Block Codes (STBC). The Space-Time refers to coding across space and time. Coding across space by using multiple transmit and receive antennas, and across time by using multiple symbol periods. Like normal block codes, the Alamouti code operates on blocks of input bits, however rather than having 1 dimensional code vectors it has 2 dimensional code matrices.

STBCs can be described by a code matrix, which defines what is to be sent from the transmit antennas during transmission of a block. The code matrix is of dimension $Nt \times tb$, where Nt is the number of transmit antennas and tb is the number of symbol periods used to transmit a block. So the rows of the matrix represent the transmit antennas, and the columns are the time (symbol) periods. The code matrix for the Alamouti code is given in Equation (1).

The code belongs to a special subclass of STBCs known as Orthogonal Space Time Block Codes (OSTBC). The code matrices of OSTBCs satisfy the following constraint.

$$XX^{H} = \sum_{n=1}^{n_{s}} |s_{n}|^{2} \cdot (\alpha I) \quad ----(2)$$

where ns is the number of symbols, sn is the nth complex symbol, α is an arbitrary constant and (.)^H denotes the Hermitian conjugate given as $X^{H} = (X^{*})^{T}$.

There are a number of properties that make OSTBCs particularly interesting. Foremost is that Maximum Likelihood (ML) detection of different symbols is decoupled. In the case of the Alamouti code this means that the two symbols which are coded together can be detected independently at the receiver. In other words the same techniques used to detect symbols one at a time in a SISO scheme can be used in the Alamouti scheme as well. Using above Equations ,the received matrix in a 2x2 system can be written as

 $Y = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} s_1 & -s_2^* \\ s_2 & s_1^* \end{bmatrix} + \begin{bmatrix} e_{11} & e_{12} \\ e_{21} & e_{22} \end{bmatrix}$ -----(3) Now let

These are the signals that are received by each of the antennas at the receiver across the two time periods. The above expressions can be obtained by expanding Equation (3). The first digit of the subscript denotes the receive antenna, and the second digit is the time period when the signal is received. Equation (3) can now be re-written as

$$Y = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix}$$
(8)

Alamouti states that the transmitted symbols sland s2 can be estimated in a maximum likelihood fashion by first combining the received signals according to the following equations

$$\tilde{s_1} = h_{11}^* r_{11} + h_{12} r_{12}^* + h_{21}^* r_{21} + h_{22} r_{22}^* \qquad \dots \dots (9)$$

and then using a standard Maximum Likelihood detector to attempt to recover s1 and s2 from s1 and s2. This is the decoupled ML detection that is common to all OSTBCs. The validity of Alamouti's proposed system can been seen by substituting the values of r11, r12, r21 and r22 from Equations 4,5,6,7 into above Equations to obtain the following.

$$\begin{split} \vec{s_1} &= h_{11}^* (h_{11}s_1 + h_{12}s_2 + e_{11}) \\ &+ h_{12}(-h_{11}^*s_2 + h_{12}^*s_1 + e_{12}^*) \\ &+ h_{21}^* (h_{21}s_1 + h_{22}s_2 + e_{21}) \\ &+ h_{22}^* (-h_{21}^*s_2 + h_{22}^*s_1 + e_{22}^*) \\ &= s_1(|h_{11}| + |h_{12}| + |h_{22}| + |h_{22}|) \\ &+ h_{11}^*e_{11} + s_2 = s_2(|h_{11}| + |h_{12}| + |h_{21}| + |h_{22}|) \\ &- h_{11}e_{12}^* + h_{12}^*e_{11} - h_{21}e_{22}^* + h_{22}^*e_{21} \quad -----(12) \end{split}$$

Similarly

National Conference on Innovative Paradigms in Engineering & Technology (NCIPET-2012) Proceedings published by International Journal of Computer Applications® (IJCA)

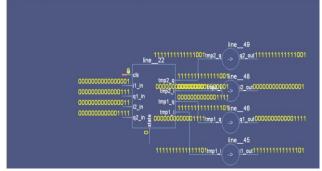
Equations 11 and 12 show that when the received signals are combined according to Equations 9 and 10, the transmitted symbols are combined coherently and weighted by a positive factor, i.e. |h11|+|h12|+|h22|. The noise samples however, get combined in an incoherent manner. This is how the Alamouti scheme is able to achieve an improvement in performance over SISO systems.

5. ALAMOUTI MIMO ENCODER-Hardware Design

The Alamouti encoder contains sequential logic and thus requires some control logic, and a clock signal. The encoder has four 16 bit inputs for the real and imaginary parts of the 2 symbols being encoded. The inputs are not registered, and are assumed to be held constant for the duration of the encoding process (2 clock cycles). There are also four 16 bit outputs for the real and imaginary parts of the encoded symbols. In line with Equation (1) of code matrix of Alamouti code, the symbols are first copied straight through to the output arrays unmodified. Then the symbols are swapped over to the opposite transmit antenna and complex conjugated, also one symbol is negated. Complex conjugation is achieved by simply negating the imaginary part Of the input before placing it into the output. Also the complex conjugation, and extra negation operations are combined into a single step for the relevant symbol by negating the real part instead of the imaginary. It is designed to operate at the same clock speed as the data rate of the system, so one clock cycle is assumed to be one symbol period.

Since it takes 2 clock cycles to encode 2 symbols the modulator must maintain a state to indicate if it is currently the first or second time period. This state is implemented as a single bit signal that is toggled each clock cycle. These outputs are feed to the OFDM and then to the RF module of 2.4GHz transceiver (Maxim MAX2822).. These chips are compatible with the physical

layer of the IEEE 802.11b standard for wireless networking. Alamouti Encoder –Result-Data Flow Result



6. ALAMOUTI MIMO DECODER-Hardware Design

The actual algorithm implemented by the combiner is fairly straight forward, however for the low-level implementation the mathematical expressions for each symbol estimate were expanded and simplified to remove the complex numbers and operations. The resulting expressions are shown in Equations (1) to (4)

	° 1 11	
	$Re\{h_{0,0}\}\times Re\{y_{0,0}\}+Im\{h_{0,0}\}\times Im\{y_{0,0}\}$	$s0_{re} =$
	$+Re\{h_{0,1}\}\times Re\{y_{0,1}\}+Im\{h_{0,1}\}\times Im\{y_{0,1}\}$	
	$+Re\{h_{1,0}\}\times Re\{y_{1,0}\}+Im\{h_{1,0}\}\times Im\{y_{1,0}\}$	
(1)	$+Re\{h_{1,1}\}\times Re\{y_{1,1}\}+Im\{h_{1,1}\}\times Im\{y_{1,1}\}$	
	$Re\{h_{0,0}\}\times Im\{y_{0,0}\}-Im\{h_{0,0}\}\times Re\{y_{0,0}\}$	$s0_{im} =$
	$-Re\{h_{0,1}\}\times Im\{y_{0,1}\}+Im\{h_{0,1}\}\times Re\{y_{0,1}\}$	
	$+Re\{h_{1,0}\}\times Im\{y_{1,0}\}-Im\{h_{1,0}\}\times Re\{y_{1,0}\}$	
(2)	$-Re\{h_{1,1}\}\times Im\{y_{1,1}\}+Im\{h_{1,1}\}\times Re\{y_{1,1}\}$	
	$Re\{h_{0,1}\}\times Re\{y_{0,0}\}+Im\{h_{0,1}\}\times Im\{y_{0,0}\}$	$s1_{re} =$
	$-Re\{h_{0,0}\}\times Re\{y_{0,1}\}-Im\{h_{0,0}\}\times Im\{y_{0,1}\}$	
	$+Re\{h_{1,1}\}\times Re\{y_{1,0}\}+Im\{h_{1,1}\}\times Im\{y_{1,0}\}$	
(3)	$-Re\{h_{1,0}\}\times Re\{y_{1,1}\}-Im\{h_{1,0}\}\times Im\{y_{1,1}\}$	
	$Re\{h_{0,1}\}\times Im\{y_{0,0}\}-Im\{h_{0,1}\}\times Re\{y_{0,0}\}$	$s1_{im} =$
	$+Re\{h_{0,0}\}\times Im\{y_{0,1}\}-Im\{h_{0,0}\}\times Re\{y_{0,1}\}$	
	$+Re\{h_{1,1}\}\times Im\{y_{1,0}\}-Im\{h_{1,1}\}\times Re\{y_{1,0}\}$	
(4)	$+Re\{h_{1,0}\}\times Im\{y_{1,1}\}-Im\{h_{1,0}\}\times Re\{y_{1,1}\}$	

So, after expansion and simplification, the expression for each component is essentially a sum of products.

The combiner inputs are four 2×2 arrays, two for the real and imaginary parts of the channel estimate, and two for the real and imaginary parts of the received samples. The outputs are two 2×1 arrays, representing the real and imaginary parts of the two symbol estimates.

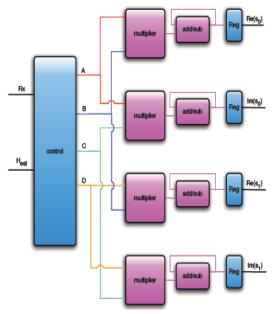
Like in the low-level simulation the hardware implementation of the Alamouti decoder is based on Equations (1)–(4).However, unlike the low-level simulation they are not simply converted into the programming language in use. When converted in this manner the single equation used over half the resources available on the FPGA chip. on the testbed. Obviously this in unacceptable as not only are there 3 other equations, but there are also other components that need to fit on the FPGA as well. So a new design is developed as given below.

MIMO Decoder Process.

Figure (3) shows a block diagram of this revised design. The design consists of four multiplier functional units, and four associated add/subtract units with registers to accumulate the totals. There is also control logic, implemented as a state machine, to multiplex inputs through to the various functional units, and also control whether the add/subtract units add or subtract (these control lines are not shown in the diagram).

The meaning of the A, B, C, and D signals is not immediately obvious, however it is explained below how these signals are related to the input signals.

National Conference on Innovative Paradigms in Engineering & Technology (NCIPET-2012) Proceedings published by International Journal of Computer Applications® (IJCA)



Block Diagram of Hardware Implementation of Alamouti Decoder

From Figure it can be seen that the design calculates all the equations for the symbol estimates in parallel. There is one multiplier and one add/subtract unit for each equation being implemented. The design is a multi-cycle implementation, it takes multiple clock cycles to compute the results. The multipliers take one clock cycle to calculate a product and the add/subtract units also take one clock cycle. Therefore two symbol estimates (real and imaginary parts) are produced every 8 clock cycles. When synthesised for the testbed the decoder can run at a maximum clock frequency of 62.135 MHz.The meaning of the A, B, C and D signal can be found by careful examination of Equations (1) -(4). In particular, note that there are four distinct sets of operands for the multiplication operations. These four sets, which have been labeled A,B,C and D, are shown in Table (1)

Pair	First Usage	Second Usage
Α	$s0_{re}$ oper and 1	$s0_{im}$ oper and 1
В	$s0_{re}$ operand 2	$s1_{re}$ operand 2
С	$s0_{im}$ oper and 2	$s1_{im}$ operand 2
D	$s1_{re}$ operand 1	$s1_{im}$ operand 1

Pairs of Operands Output by the Control Logic in Alamouti Decoder.

To further explain the meaning of Table (1) take pair A as an example. The first usage of A is listed as "s0re operand 1" and the second is "s0im operand 1". Now examine Equations (1) and (2), the equations for s0re and s0im, reproduced in part below as Equations (5) and (6).

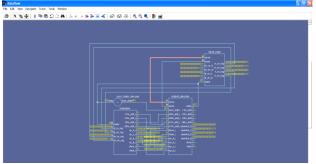
$$s_{0re} = Re\{h_{0,0}\} \times Re\{y_{0,0}\} + Im\{h_{0,0}\} \times Im\{y_{0,0}\} + Re\{h_{0,1}\} \times Re\{y_{0,1}\} + Im\{h_{0,1}\} \times Im\{y_{0,1}\} \dots$$

$$s_{0im} = Re\{h_{0,0}\} \times Im\{y_{0,0}\} - Im\{h_{0,0}\} \times Re\{y_{0,0}\} - Re\{h_{0,1}\} \times Im\{y_{0,1}\} + Im\{h_{0,1}\} \times Re\{y_{0,1}\} \dots$$
(6)

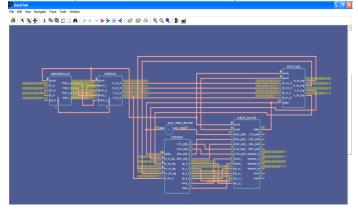
Note, in particular, that the first (left hand) operand of any multiplication in Equation (1) is the same as the first operand of the corresponding multiplication in Equation (2). Because these operands are always the same they are grouped together as pair A. Table(1).similarly specifies the members of the other pairs. These grouping can be

verified by checking them against Equations (1) - (4)By exploiting these pairings the control logic is able to multiplex the required inputs through to all of the multiplier functional units using only four multiplexers instead of the eight that would otherwise be required.

Alamouti Deccoder –Result-Data Flow Result



MIMO-All (Encoder +OFDM +Decoder) –Dataflow Result



7. TOOLS & IMPLEMENTATION

The Following tools were used during design are MODEL SIM-XE II 5.7c and Quartus II 5.1 c For establishing 3G/4G Wireless link, Suggested RF module is of 2.4GHz transceiver (MaximMAX2822). These chips are compatible with the physical layer of the IEEE 802.11b standard for wireless networking.

8. CONCLUSIONS

We have presented the design methodology used in the implementation of a MIMO decoder within a 3G/4G radio system. The architecture of the system has been optimized to comply with the throughput requirements while reducing implementation area.

For Demonstrating the MIMO DECODER, First the MIMO Encoder with OFDM Modulation and then MIMO Decoder with OFDM Demodulation is developed.

For transmitting TWO Symbols, Four 16 bit Inputs are applied as Input to 2X2 MIMO Encoder and OFDM whose Outputs are coupled to the Receiver section-OFDM Demodulation and MIMO Decoder.

The Data Output produce by the MIMO Decoder is same as the Data Input applied to MIMO Encoder. Hence the MIMO Decoder follows the MIMO Encoder Inputs.

Two FPGA Based Modules are implemented. One For Transmitter Part includes MIMO Encoder and OFDM. Second For Receiver Part included OFDM and MIMO DECODER.

9. REFERENCES

- VLSI Design Volume 2008, Article ID 312614. This work has been supported by European FP6 IST 2002 507039 Project 4 MORE and by the Spanish Ministry of Science and Technology under Project TEC2006-13067-C03-03 from IEEE site
- [2] 4MORE IST project website. [Online]. Available: http://ist-4more.org
- [3] S. M. Alamouti, "A simple transmit diversity technique for wireless communications," *IEEE J. Select. Areas Commun.*, vol. 16, no. 8, pp. 1451–1458, Oct. 1998.
- [4] A. Fern'andez-Herrero, A. Jim'enez-Pacheco, G. Caffarena, and J. Casaj'us- Quir'os, "Design and implementation of a hardware module for equalisation
- in a 4G MIMO receiver," in *Proc. IEEE Int. Conf. on Field Programmable Logic and Applications (FPL'2006)*, Madrid, Spain, Aug.2006.
- [5] (2006, Mar.) Virtex-4 user guide. [Online]. Available: <u>http://www.xilinx</u>. com/bvdocs/userguides/ug070.pdf.