Design Methods for Low-Power Implementation

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ABSTRACT
Implementation of low power techniques in the design is increasing because of the increasing clock frequency and a continuous increase in the number of transistors on chip. These low power techniques are being implemented across all levels of abstraction - system level to device level. Here, approaches related to front-end HDL based design styles, which can reduce power consumption, have been mentioned. As is known, power dissipation has a direct relation with the clock frequency and dynamic power also depends upon the rate at which the data toggles for a given circuit. The design styles mentioned here, focus on several areas of designing using HDL, which are at times not considered significant, as they do not affect the functionality. The techniques mentioned here are quite simple to implement and mostly clear of confusion techniques that are considered quite insignificant, yet have a significant impact on the overall power-consumption.

Keywords
RTL, One- hot encoding, Gray encoding, Bus invert coding, synthesis, FSM

1.INTRODUCTION
Power dissipation in a CMOS transistor depends on the capacitance, supply voltage and the rate at which the data toggles.

$$P = f * C_{load} * V_{DD}^2$$

Where,
C_{load} is the load capacitance of the CMOS transistor
V_{DD} is the supply voltage
f is the frequency at which the data transition takes place.
If P_{dt} describes the probability of data transition then

$$f = P_{dt} * f_{clk}$$

Example: For a random data P_{dt} = 0.5 so for a clock frequency of 50MHz, the value of f would be 0.5 * 50 MHz = 25 MHz. An efficient and high quality HDL code can reduce unwanted transitions and can save substantial amount of power in the design. Also logic optimization techniques like removing redundant logic and properly sharing the resource in design also helps in power reduction.

1. MINIMIZING DATA TRANSITIONS ON BUS
In many cases the data on the bus keeps on transitioning from one value to another because there is no default state for assigning a constant value. This may not affect the design functionally as there may be some handshaking signal which indicates that the data is valid. But the transitions on data bus consume power.

// Code that resets the Bus to default status after valid gets de-asserted.

```
always@(posedge clk or negedge reset)
begin
        if(!reset)
            data_bus = 16'b0;
        else if(data_bus_valid)
            data_bus = data_o;
        else
            data_bus = 16'b0;
end
```

// Code that holds the Bus to its previous value after valid gets de-asserted.

```
always@(posedge clk or negedge reset)
begin
        if(!reset)
            data_bus = 16'b0;
        else if(data_bus_valid)
            data_bus = data_o;
end
```

AVOIDING UNNECESSARY TRANSITION OF SIGNAL
It is seen in many designs that certain signals transit when they are not required to, but they are not detected in functional verification, as they satisfy the logical requirements. Such signals, if checked properly and if the logic is tweaked to suppress those unwanted transitions, can also help avoid utilization of power.

RESOURCE SHARING
The RTL coding should be carried out in a manner that there are no unwanted or redundant logic elements. Any logic element will contribute to power consumption as it has a capacitance attached to it and transitioning of data through that logic will lead to power dissipation.

```
// Example where resource sharing is not possible
always@(in1 or in2 or sel)
        if(sel)
            out1 = in1 + in2;
        else
            out1 = 4'b0;
always@(in3 or in4 or sel)
        if(!sel)
            out2 = in3 +in4;
        else
            out = 4'b0;
// Example where resource sharing is  possible
always@(in1 or in2 or in3 or in4 or sel)
    if(sel)
        begin
          out1 = in1 + in2;
          out2 = 4'b0;
        end
```

```
else
        begin
          out1 = 4'b0;
          out2 = in3 + in4;
        end
```

4. CONTROL OVER COUNTERS

Counters are normally designed so that they can start and stop as per requirement. Certain times, due to improper coding, all the start and stop conditions are not taken care of and the counter may unnecessarily keep on counting.

```
// Example of unnecessary counter transitions.
always@(posedge clk or negedge reset)
begin
        if(!reset)
              cnt  = 4'b0;
        else if( (cnt == 4'b0111) | cntr_reset)
              cnt = 4'b0;
        else
              cnt = cnt + 1'b1;
end

// Example that removes unnecessary counter transitions.
always@(posedge clk or negedge reset)
begin
        if(!reset)
              cnt  = 4'b0;
        else if ( cntr_reset)
              cnt = 4'b0;
        else if(cnt < 4'b0111)
              cnt = cnt + 1'b1;
end
```

For example, for a random probability data (P = 0.5) and clock frequency of 100 MHz, the transition frequency would be around 50 MHz. For a bus capacitance of 25 pF and supply voltage of 1.2 V, this would result in 1.8 mW power consumption.

5. STATE MACHINE ENCODING(FSM)

It is a well known fact that one-hot and Gray encoding consume lesser power as compared to binary encoding. This is because one-hot and gray encodings have only a single bit change while going from one state to another.

6.ALLOW SYNTHESIS OPTIMIZATION

Certain constraints and coding styles can be followed which reduce the area utilization or logic optimization. This is because extra logic will add extra capacitance and in turn will consume more power. Also, one way of checking redundant hardware generation is by tactfully analyzing the code coverage reports.

REGISTER RETIMING

Register timing is a concept mostly used in improving timing by reordering the combinational and sequential logic in a given data path. However in certain cases, there is a saving of logic and thus can help improve upon power consumption. Of course, this is possible only if the design can support the additional timing overhead.

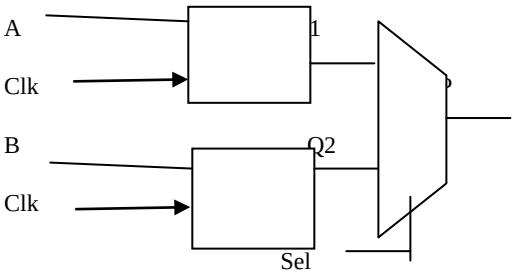

Fig1. Without Retiming

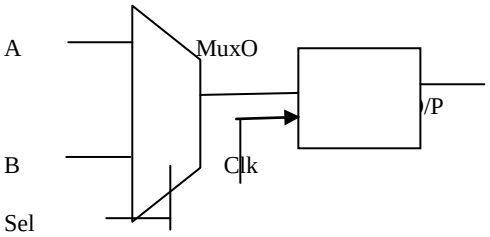

Fig2. With Retiming

USING GRAY CODING FOR ADDRESSING MEMORIES

It is seen that addressing memories via gray coding significantly reduces the power as there are lesser number of transitions that the address counter performs. A detailed explanation and trade-offs of the same is mentioned [3].

USING BUS INVERT CODING FOR I/Os OR LONG DATA PATHS

Bus invert coding [2] is a technique in which if the hamming distance between the current data and the next data is more that N/2 (where N is the bus width), then one can invert the bits and send it, so as to minimize the number of transitions on the bus. In that case a control bit goes along with the data to indicate the receiving end, whether the data is inverted or not. The following are the results of a simulation carried out to understand the reduction in the number of transitions due to bus invert coding.

Bus Width	Total random data input	Number of Transitions without coding (A)	Number of transition with bus invert coding (B)	Percentage improvement in bus invert coding against non-coded data (B) / (A) * 100
32-bit	**5000000**	**8005314**	**6879054**	14.06 %
64-bit	1000000	32000980	28513273	**10.89**

USING SYSTOLIC OR PIPELINED DESIGN FOR DSP IMPLEMENTATION

A detailed understanding of systolic architecture and pipelined architecture for implementing a DSP block are mentioned in [1]. Pipelining reduces power by registering the inputs at regular intervals and thereby reduces the overall net-lengths and minimizes glitches. Systolic architectures have high modularity and help reduce long interconnect path delays. Depending on the requirements of latency and hardware, one can choose one of these approaches

CONCLUSION

A significant reduction in the power dissipation was observed by following the techniques described in this paper. A good practice would be to not only verify the design for its functional adherence, but also verify it from the low power perspective, by employing methods and strategies that target detection of unwanted transitions and logic redundancy.

REFRENCES

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