Review of Junctionless transistor using CMOS technology and MOSFETs

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ABSTRACT
Transistors are the fundamental building blocks of modern electronic devices and all existing transistors contain semiconductor junctions. Junctionless transistor is a uniformly doped nanowire without junctions with a wrap-around gate. As the distance between junctions in modern devices drops below 10nm, extraordinarily high doping concentration gradients become necessary. Junctionless transistors could therefore help chipmakers continue to make smaller devices. Here, in this paper presented a new type of transistor in which there are no junctions and no doping concentration gradients. They have near-ideal sun threshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistors.

General Terms
Structure and operating modes of Junctionless transistor, Fabrication techniques, Comparison between conventional MOSFETs and Junctionless transistor.

Keywords
Gated resistor, Junctionless transistor, Silicon nanowire FET, E-beam lithography and AFM.

1. INTRODUCTION
The transistor principle was filed in Canada by Austrian-Hungarian physicist Julius Edgar Lilienfield. Continuous device miniaturization, such as scaling physical channel length and gate dielectric thickness, is becoming increasingly difficult in semiconductor technology. In addition due to challenging doping profile control in order to control short-channel effects of bulk silicon channel, novel non–planar structures are being sought. Among emerging devices, nanowire transistors, which could be done with the undoped or doped body, have drawn much attention for good scaling capability and technology compatibility [1]. Recently, the junctionless MOSFET with a same type of semiconductor throughout the whole silicon (from source to drain), which behaves like a resistor, was proposed. The Lilienfield device is a simple resistor and the application of a gate voltage allows the semiconductor film of carriers to be depleted thereby modulating its conductivity. Ideally, it should be possible to completely deplete the semiconductor film of carriers. All existing transistors are based on the formation of junctions. Junctions are capable of both blocking current and allowing it to flow, depending on an applied bias, they are typically formed by placing two semiconductor regions with opposite polarities into contact with one another. The most common junction is the p-n junction. Other types of junctions include the metal-silicon 'Schottky' junction and the heterojunction. The bipolar junction transistor contains two p-n junctions, and so does the MOSFET. The JFET has only one p-n junction and the MESFET (metal-semiconductor field effect transistor) contains Schottky junction. The Lilienfield transistor, unlike all other types of transistors, does not contain any junction. Although the idea of a transistor without junctions may seem quite unorthodox, the word 'transistor' does not imply the presence of junction. A transistor is a solid state device that controls current flow, and the word 'transistor' is a contraction of 'trans-resistor'. Technically, the Lilienfield transistor is a gated trans-resistor; that is, it is a resistor with a gate that controls the carrier density, and hence the current flow [2].

2. DEVICE STRUCTURE AND OPERATING MODES

2.1 Structure

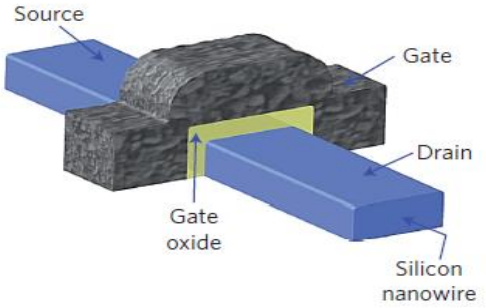

Fig 1: Structure of junctionless transistor

The Lilienfield transistor is a field effect device, much like modern metal-oxide-semiconductor (MOS) devices. It consists of a thin semiconductor film deposited on a thin insulator layer, itself deposited on a metal electrode. The latter metal electrode serves as the gate of the device. In operation, the current flows in the resistor between two contact electrodes, in much the same way that drain current flows in the resistor between the source and drain in modern MOSFET.

2.2 Operating modes
The channel region in a gated resistor is neutral in the centre of the nanowire and, because the carriers are located in neutral silicon, they see a zero electric field in the directions perpendicular to the current flow. When the device is fully turned on, assuming a low drain voltage for simplicity, the entire channel region is neutral and in flatband conditions. The channel then effectively behaves as a resistor with conductivity $\sigma = q\mu N_D$, and the mobility is that of carriers traveling through bulk silicon. The mobility of electrons in heavily doped n-type silicon is ~100cm² $V^{-1}s^{-1}$; it varies very little for doping concentrations ranging from $1x10^{19}$ to $1x10^{20}$ cm^{-3}. In a similar way, hole mobility hovers around $40cm^2 V^{-1}s^{-1}$ in p-type silicon for the same doping concentrations. These mobility values may seem rather low, but they are to be placed in the context of modern short-channel MOSFETs. In unstrained silicon, the effective channel mobility of bulk MOSFETs drops from 400 $cm^2 V^{-1} s^{-1}$ at the 0.8 μm node to 100 $cm^2 V^{-1} s^{-1}$ at the 0.13 μm node.

Similarly, a drop of peak mobility from 300 to 140 $cm^2 V^{-1} s^{-1}$ is reported in FinFETs when the gate length is reduced from 0.9 to 0.11 μm. If it was not for straining techniques, the electron mobility at the 45 nm node would be well below 100 $cm^2 V^{-1} s^{-1}$. These straining techniques can, of course, be applied to gated resistors as well inversion-mode transistors. In a MOSFET, carriers are confined in an inversion channel in which scattering events rapidly increase in frequency with gate voltage, thereby decreasing trans conductance and current drive. In the heavily doped gated resistor, the drain current essentially flows through the entire section of the nanoribbon, instead of being confined in a surface channel. Figure 2 shows the electron concentration in an n-type junctionless gated resistor for different values of gate voltage ranging from device pinch-off (Fig. 2a)to flatband conditions (Fig. 2d). The conduction path is clearly located near the centre of the nanowire, and not at the silicon–SiO2 interfaces. This allows for the electrons to move through the silicon with bulk mobility, which is influenced much less by scattering than the surface mobility experienced by regular transistors. It is, however, possible to create surface accumulation channels by increasing the gate voltage beyond the flatband voltage, if a resistor sees its transconductance degrade much more slowly when gate voltage is increased. As a result, higher current and, therefore, higher-speed performance, can be expected from the gated resistor. The variation of the threshold voltage of a gated resistor with temperature is similar to that of a bulk MOSFET, with values of approximately -1.5 mV^oC^{-1} measured in our devices. Interestingly, the decrease of mobility with temperature is much smaller in the gated resistors than in trigate FETs. In a lightly doped FET, the mobility is little affected by impurity scattering and tends to be phonon limited, so it shows a strong temperature dependence. In the highly doped gated resistor, on the other hand, mobility is limited by impurity scattering rather by phonon scattering, and its variation with temperature is much smaller. For instance, the electron mobility measured at room temperature in trigate FETs and gated resistors are 300 and 100 $cm^2 V^{-1} s^{-1}$, respectively. When heated to 200ºC, the trigate FETs show a 36% loss of mobility, whereas the gated resistor has a reduction in mobility of only 6%.further increase of drain current is desired. Because it operates under bulk conduction rather than channel conduction, the gated resistor sees its transconductance degrade much more slowly when gate voltage is increased. As a result, higher current and, therefore, higher-speed performance, can be expected from the gated resistor [2].

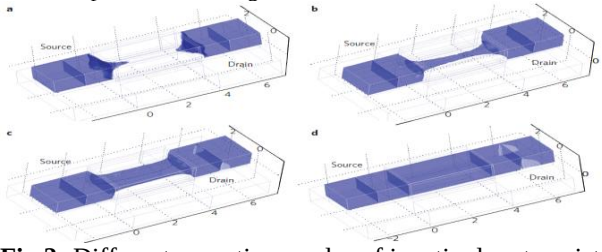

Fig 2: Different operating modes of junctionless transistor

Plots result from simulations carried out for a drain voltage of 50 mV and for different gate voltage (V_G) values: below threshold ($V_G<V_{TH}$) the channel region is depleted of electrons (a); at threshold ($V_G=V_{TH}$) a string-shaped channel of neutral n-type silicon connects source and drain (b); above threshold ($V_G>V_{TH}$) the channel neutral n-type silicon expands in width and thickness (c); when a flat energy bands situation is reached ($V_G=V_{FB}>>V_{TH}$) the channel region has become a simple resistor (d). The device has a channel width, height and length of 20, 10 and 40 nm, respectively. The n-type doping concentration is 1 x 10^{19} cm^{-3}

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3. DEVICE FABRICATION TECHNIQUES

The key to fabricating a junctionless gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations.

The devices were made on standard SOI. The SOI layer was thinned down to 10-15nm and patterned into nanoribbons using ebeam lithography. Gate oxidation was performed and ion implantation was used to dope the devices uniformly N+ or P+ with a concentration of 1-2×10^{19} cm^{-3}, which is a typical LDD doping concentration, to realize N-channel and P channel devices, respectively. The gate was formed by deposition of a 50-nm-thick layer of amorphous silicon at a temperature of 550 ºC in a low-pressure chemical vapour deposition (LPCVD) reactor. The N-channel gated resistors have a P+ polysilicon gate and the P-channel devices have an N+ poly gate, which eliminates poly depletion effects and yields suitable threshold voltage values. No additional S&D implant was used. Oxide was deposited and etched to form contact holes, and TiW + Al metallization completed the process. Nanoribbons were fabricated with thickness ranging from 5 to 10nm and width ranging from 20 to 40nm. The gate oxide thickness is 10nm [3].

The Junctionless side gate silicon Nano-wire transistor has been fabricated by Atomic Force Microscopy (AFM) and wet etching on p-type Silicon On Insulator (SOI) wafer. The nanometer-scaled electronic design pattern was fabricated on

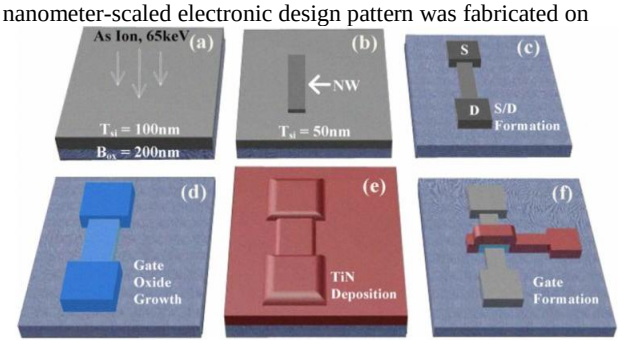

Fig 3: Fabrication process by E-beam lithography [4]

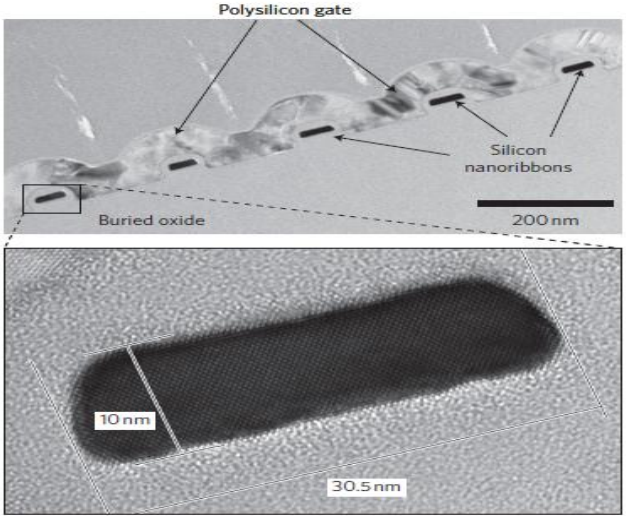

Fig 4: TEM image of one of the parallel junctionless transistors [2]

(100) silicon on insulator wafer by using Scanning Probe Microscopy (SPM) via Atomic Force Microscope (AFM) nanolithography process. In this work we make a nano-electronic device fabrication process based on KOH etch applied to structures defined by AFM nanolithography. The samples with a surface area 1-1.5 cm^2 were cut from p-type Silicon On Insulator (SOI) <111> wafers phosphorus doped, resistivity 5-10 µm, diameter 100±0.5mm, thickness 525 ± 25 µm. The SOI were used was as-grown and not subjected to any heat treatment. The samples were cleaned by using NH_4OH CMOS grad and H_2O_2 heated at 80^oC for 15 minutes to remove the organic contaminants, followed by rinsing with De Ionized Water (DIW). Solution from HCl and H_2O_2 were used to clean the ion metal on surface and heated at 80oC for 15 minutes, followed by DIW. Diluted HF, ratio 1:20 were use to remove the native oxide layer on SOI. All samples were cleaned with HF to give all samples the same starting conditions. After cleaning, the sample were place in the beaker, containing the aqueous KOH varies in concentrations from 10% wt. to 40% wt. All the samples were etched in that solution for 12 sec in 60°C with and accuracy ±5°C. The nanometer-scaled electronic structure of the transistor is prepared by using of the- AFM nanolithography, which set up with constantly AFM mood in all necessary parameters. The pattern is formed on Silicon-On-Insulator (SOI) <100>. Before growth oxide as a mask (desired pattern), the SOI (substrate) were followed cleaning procedure as above mentioned [5].

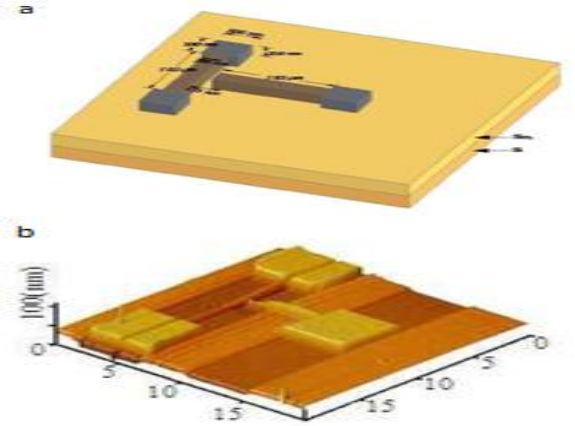

Fig 5(a) and (b): Fabrication process by Atomic Force Microscopy

4. COMPARISON

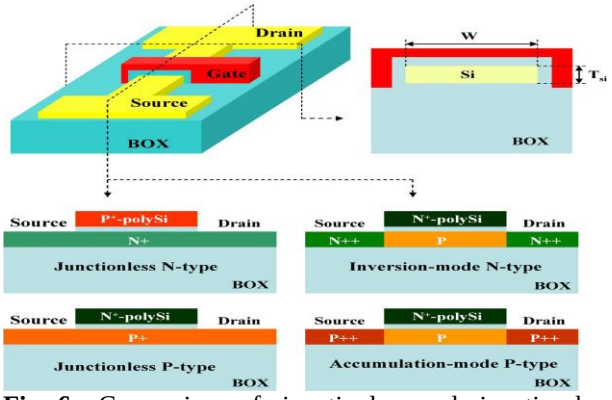

Fig. 6. Comparison of junctionless and junction-based transistors [6]

MOSFETs (including FinFETs and trigate FETs) are normally-off devices, as the drain junction is reverse biased and blocks any current flow if no channel is created between source and drain. To turn the device on, the gate voltage is increased to create an inversion channel. The drain current in such a device is classically given by

$$I_D \approx \mu C_{ox} \left(\frac{W_{si}}{L}\right)(V_{DD} - V_{TH})^2$$

where Wsi is the width of the device, L the gate length, VDD the supply voltage and Cox the gate oxide capacitance. The gated resistor, on the other hand, is basically a normally-on device in which the workfunction difference between the gate electrode and the silicon nanowire shifts the flatband voltage and the threshold voltage to positive values. When the device is turned on and in flatband conditions, it essentially behaves as a resistor and the drain current is given by

$$I_D \approx q\,\mu N_D \left(\frac{T_{si}W_{si}}{L}\right)V_{DD}$$

where Tsi is the thickness of the silicon and ND the doping concentration. Note that the current is independent of the gate oxide capacitance. Current can be increased simply by increasing the doping concentration of the device. The variability of the threshold voltage is larger in gated resistors than in traditional ultrathin-film, inversion-mode SOI transistors. The carrier mobility of gated resistors is lower than the nanowire FETs at high VGS i.e, high ON state, but in the 'weak inversion' i.e, subthreshold region it shows similar carrier mobility that of the conventional nanowires. The junctionless transistor has better SS (subthreshold) slope and DIBL (drain induced barrier lowering) characteristics than the conventional mosfets in ultra low power logic. The short-channel effects have been improved in junctionless devices.

Table 1: Comparison of conduction modes

State	Inversion mode NWT	Accumulation mode NWT	Junctionless transistor
ON	Main current in surface inversion channels	-Surface accumulation channels -small body current	-Surface accumulation channels are unnecessary -large body current
OFF	Surface subthreshold current	Body subthreshold current	Body subthreshold current

Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold, but above threshold the field drops to zero. This is the opposite of inversion-mode (IM) or even accumulation mode (AM) devices where the field is highest when the device is turned on [7].

5. TYPES OF JUNCTIONLESS TRANSISTOR

5.1 Junctionless MuGFET

This device has no junctions, a simpler fabrication process, less variability and better electrical property than classical inversion mode.

5.2 Bulk Planar Junctionless Transistor (BPJLT)

The bulk planar junctionless transistor (BPJLT) is highly scalable source–drain junction- free field-effect transistor. It is thus junctionless in the source–channel–drain path but needs a junction in the vertical direction for isolation purposes.

5.3 Junctionless Vertical MOSFET (JLVMOS)

The junctionless VMOS is based on bulk-Si wafer. The vertical channel of a VMOS is defined by the gate spacer thus the fabrication cost can be reduced drastically. The double-gate scheme of a VMOS helps to increase the gate controllability over the channel region [8].

6. CONCLUSION

In this paper, structure of junctionless transistor has been studied with different fabrication techniques such as E-beam lithography using LPCVD reactor and Atomic Force Microscopy using scanning probe microscopy. Different operating modes of the transistor have been studied based on the values of V_{GS} and V_{TH}. Also, the comparison between the conventional MOSFETs and the junctionless transistor has been studied. The gated resistor requires much less complicated fabrication steps and hence simpler chip making. It also shows better electrical properties than the conventional MOSFETs in the ultra low power logic.

7. REFERENCES

[1] Chun-Yu Chen1, Jyi-Tsong Lin1, Meng-Hsueh Chiang2, and Keunwoo Kim3 “High-Performance Ultra-Low Power Junctionless Nanowire FET on SOI Substrate in Subthreshold Logic Application” 1National Sun Yat-Sen University., Kaohsiung 804, Taiwan ROC, 2National Ilan University., I-Lan 260, Taiwan ROC, 3IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA

[2] Jean-Pierre Colinge, Chi-Woo Lee, Aryan Afzalian, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, Pedram Razavi, Brendan O’Neill, Alan Blake, Mary White, Anne-Marie Kelleher, Brendan McCarthy and Richard Murphy: “Nanowire transistors without junctions”, Nature nanotechnology.

[3] J.P. Colinge, C.W. Lee, A. Afzalian, N. Dehdashti, R. Yan, I. Ferain, P. Razavi, B. O’Neill, A. Blake, M. White, A.M. Kelleher, B. McCarthy and R. Murphy “SOI Gated Resistor: CMOS without junctions” Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Republic of Ireland.

[4] Chan-Hoon Park, Myung-Dong Ko, Ki-Hyun Kim, Chang-Woo Sohn, Chang Ki Baek, Yoon-Ha Jeong and Jeong-Soo Lee “Comparative Study of Fabricated Junctionless and Inversion-mode N anowire FE Ts”. POSTECH, Pohang, Gyeongbuk, 790-784, Korea.

[5] Arash Dehzangi, Farhad Larki, E.B. Saion, Sabar D. Hatagalung, Makarimi Abdullah, M.N. Hamidon and Jumiah Hassan “Study the Characteristic of P-Type Junction-Less Side Gate Silicon Nanowire Transistor Fabricated by Atomic Force Microscopy Lithography” American Journal of Applied Sciences 8 (9): 872-877, 2011 ISSN 1546-9239 © 2011 Science Publications

[6] Chi-Woo Lee, Adrien Borne, Isabelle Ferain, Aryan Afzalian, Member, IEEE, Ran Yan, Nima Dehdashti Akhavan, Pedram Razavi, and Jean-Pierre Colinge, Fellow, IEEE, “High-Temperature Performance of Silicon Junctionless MOSFETs” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 57, NO. 3, MARCH 2010.

[7] Twinkal Solankia, Nilesh Parmar “ A Review paper: A Comprehensive study of Junctionless transistor”, National Conference on Recent Trends in Engineering & Technology.

[8] Chih-Hsuan Tai, Jyi-Tsong Lin, Yi-Chuen Eng, and Po-Hsieh Lin “A Novel High-Performance Junctionless Vertical MOSFET Produced on Bulk-Si Wafer” Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan R.O.C.