# Current Starved Voltage Controlled Oscillator for PLL Using 0.18µm CMOS Process

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## ABSTRACT

A five stage current starved Voltage Controlled Oscillator (CMOS VCO) is designed in this paper. The design is implemented in Tanner environment with high oscillation frequency and low power consumption. Oscillation frequency of the designed VCO ranges from 25.70 MHz to 222.53 MHz. The circuit is simulated using 180nm SCN018 Technology. Simulation results reported that the power consumption is 58.47uA @ 1.8V VDD. Design procedures and simulation results are illustrated. This design is suitable for PLL as a frequency multiplier.

## Keywords

Tanner, Low power, current starved VCO

## 1. INTRODUCTION

A PLL is essentially a feedback loop that locks the on-chip clock phase to that of an input clock or signal. High-performance PLLs and clock buffers are widely used within a digital system for two purposes: clock generation, and timing recovery. For clock generation, since off-chip reference frequencies are limited by the maximum frequency of a crystal frequency reference, (Typically in the range of 10 MHz) a PLL receives the reference clock and multiplies the frequency to the multi-gigahertz operating frequency. The high-frequency clock is then driven to all parts of the chip. Timing recovery pertains to the data communication between chips. As data rates increase to satisfy the increase in on-chip processing rate, the phase relationship between the input data and the on-chip clock is not fixed. To reliably receive the high-speed data, a PLL locks the clock phase that samples the data to the phase of the input data. Phase locked loop is closed loop control system that compares the output phase with the input phase. High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Within the digital systems, well-timed clocks are generated with phase-locked loops (PLLs). The rapid increase of the system's clock frequency possesses challenges in generating and distributing the clock with low uncertainty [1].

### 1.1 System Overview

Phase-locked loops (PLLs) generate well-timed on-chip clocks for various applications such as clock-and-data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent.

This section briefly discusses the basic concept of phase locking. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL.

A PLL also multiplies a low-frequency reference clock , to produce a high-frequency clock . A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals. The overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

A basic form of a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
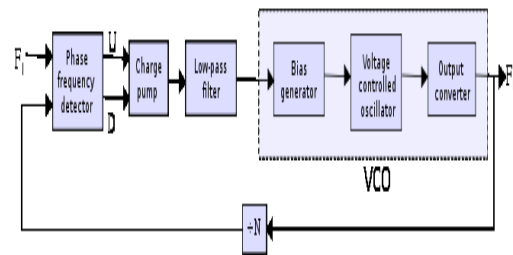5. Divide by N Counter



**Figure 1 Block Diagram of PLL**

The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an up signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage control $V$. On the contrary, if the error signal from the PFD is a down signal, the charge pump removes charge from the LPF capacitor, which decreases control $V$ . control $V$ is the input to the VCO. Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an up signal, the VCO speeds up. On the contrary, if a down signal is generated, the VCO slows down. The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock. Because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference clock [2].

## 1.2 Other applications

- Demodulation of both FM and AM signals
- Recovery of small signals that otherwise would be lost in noise (lock-in amplifier)
- Recovery of clock timing information from a data stream such as from a disk drive
- Clock multipliers in microprocessors that allow internal processor elements to run faster than external connections, while maintaining precise timing relationships
- DTMF decoders, modems, and other tone decoders, for remote control and telecommunications

## 2. WORKING OF CURRENT STARVED VCO

The operation of current starved VCO is similar to the ring oscillator. Middle PMOSM1 and NMOSM2 operate as inverter, while upper PMOSM13 and lower NMOSM14 operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. PMOSM11 and NMOSM11 drain currents are the same and are set by the input control voltage [3].

## 3. VCO DESIGN

The Designed current-starved VCO is shown in Fig 2.The VCO is composed of 5 cascaded inverters the inverter schematic is given in Fig 4. The inverter sizes PMOS1 and NMOS1, of Fig.2, are calculated [4]. The total capacitance Ctot is given by,

$$Ctot = \frac{5 * Cox(WpLp + WnLn)}{2}$$

where Cox is the oxide capacitance.

The number of stages of the oscillator is selected; there are 5 stages. The centre drain current is calculated as:

$$IDcentre = N * VDD * Ctot * Fcen$$

where N is the number of stages of inverter.

The sizes of PMOS11 and NMOS12 are determined as:

$$IDcentre = \frac{\beta(Vgs - Vthn)2}{2}$$
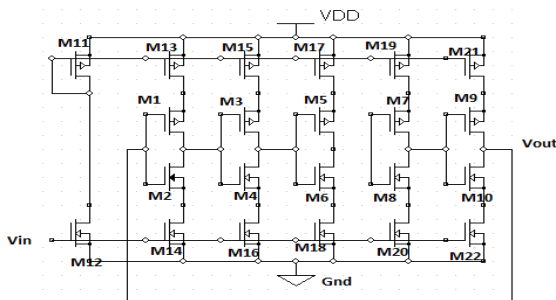
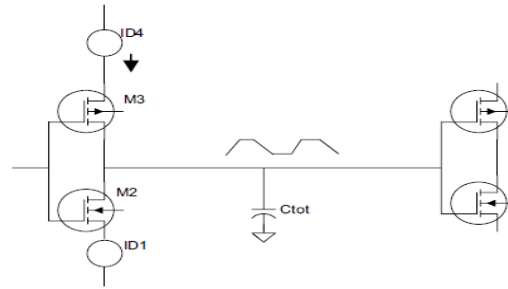Where, $\beta = \frac{Kp \cdot W}{L}$



**Figure 2.Current-Starved VCO**



**Figure 3 Inverter Schematic**

It can be shown that the oscillation frequency is:

$$Fosc = 1/N * Td$$

$$= \frac{ID}{N \cdot Ctot \cdot VDD}$$

$$= Fcen@VinVCO$$

$$= \frac{VDD}{2}$$

where Td is the time delay.

Above equation gives the centre frequency of the VCO when ID=IDcentre.

The VCO stops oscillating, neglecting subthreshold currents, when ,VinVCO<Vthn.

Thus, Vmin=Vthn and Fmin=0

The max VCO oscillation frequency Fmax is determined by finding ID when

VinVCO=VDD.

At the max frequency then, Vmax=VDD.

## 4. SIMULATION RESULTS

In PLL, when output of charge pump is applied as a control voltage to the VCO, the respective output voltage waveform of VCO is shown in fig .4.Thus it can be seen that at the control voltage of 1.8V, the respective output frequency is 222.53MHz.
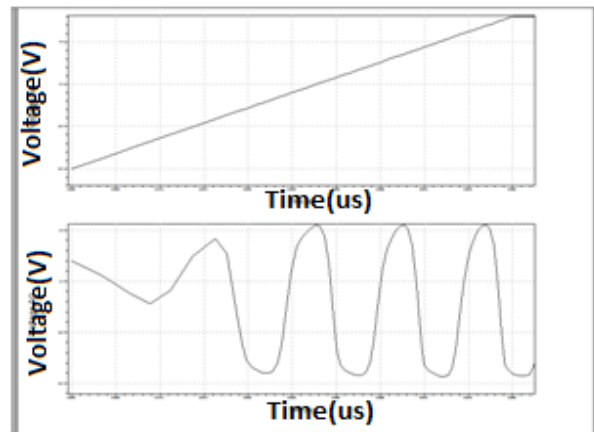


**gure. 4**

Thus it s noted that at a constant control voltage of 1.8V the output frequency of current starved VCO is 222.53 MHz and respective output waveform of VCO is shown in Fig.5. Simulation results reported that the power consumption is 58.47uA @ 1.8 VDD.
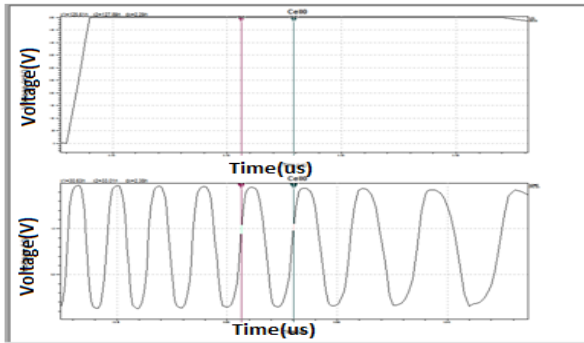
**Figure 5.Output Waveforms of current starved VCO**

When the control voltage is varied from 0V to 1.8V, the. Oscillation frequency of the designed VCO ranges from 25.70 MHz to 222.53 MHz. Table 1 gives the characteristics of the current starved VCO i.e. control voltage(V) Vs frequency (MHz).

**Table 1 Control Voltage Vs Frequency of Current Starved VCO**

| Control Voltage(V) | Frequency(MHz) |
|---|---|
| 0.1 | 25.70 |
| 0.2 | 44.64 |
| 0.3 | 57.14 |
| 0.4 | 101.52 |
| 0.5 | 129.03 |
| 0.6 | 147.05 |
| 0.7 | 161.29 |
| 0.8 | 178.57 |
| 0.9 | 188.67 |
| 1.0 | 192.30 |
| 1.1 | 198.01 |
| 1.2 | 203.99 |
| 1.3 | 208.62 |
| 1.4 | 212.24 |
| 1.5 | 212.77 |
| 1.6 | 216.00 |
| 1.7 | 216.37 |
| 1.8 | 222.53 |

The graph shown in Fig.6 shows that the relationship between frequency (MHz) Vs control voltage (V) is linear.
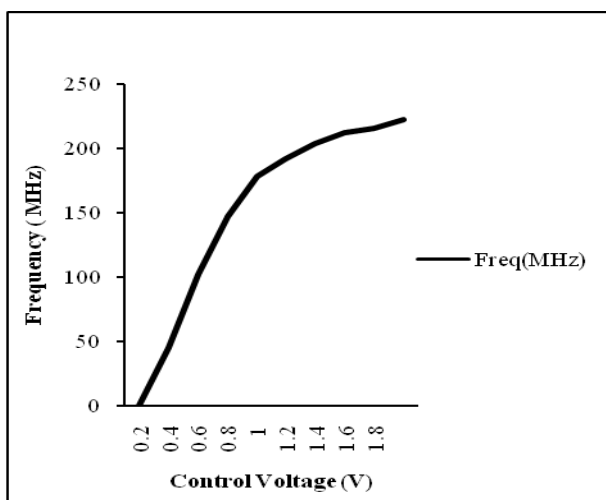


**Figure 6.Frequency (MHz) Vs Control Voltage (V)**

## 5. CONCLUSION

This paper presents a design of a low power, 222.53 MHz CMOS VCO using SCN018 Technology. The simulation results of this design shows that the proposed VCO could achieve high oscillation frequency with low power consumption. This design is suitable for PLL as a frequency multiplier. The design goal of a wide range, low power Consumption VCO is successfully achieved. Therefore, a robust VCO can be designed for reliable operation.The techniques proposed in this paper can also be applied to other low voltage analog and RF circuits to improve their performance.

## 6. REFERENCES

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