Carrier Pulse width Modulation for Three Phase Multilevel Inverter to Minimise THD and enhance the Performance of Induction motor

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Abstract
This paper presents the simulation of multilevel inverter fed induction motor drive. The poor quality of voltage and current of a conventional inverter fed induction machine is due to the presence of harmonics and hence there is significant level of energy losses. To obtain high quality sinusoidal output voltage with reduced harmonics, SPWM control scheme is proposed for diode clamped multilevel inverter. An open loop speed control can be achieved by using V/f method. The proposed system is an effective replacement for the conventional method which produces high switching losses, results in poor drive performance. The simulation results reveal that the proposed circuit effectively controls the motor speed and enhances the drive performance through reduction in total harmonic distortion (THD). The effectiveness of the system is verified through simulation using MATLAB.

Keyword-: Diode clamped multilevel inverter, Induction motor, Multicarrier PWM technique, THD,

1. INTRODUCTION
Power Electronics is playing an important role in the torque and speed control of motor drive. Variable speed AC induction motor drives are replacing the conventional DC Drives in industrial drive environment.
DC motors have been used in the past in the industries for variable speed control applications, because its flux and torque can be controlled easily by changing the field and armature currents respectively. Furthermore, four quadrant operations of induction motors was also achieved. Induction motor is popularly used in industries as they are mechanically rugged and robust. They were mainly used for essentially constant speed applications because of the unavailability of the variable frequency supply voltage. The advancement of Power Electronics has made it possible to vary the frequency of the voltage. Thus, it has extended the use of induction motor in variable speed drive applications.

The concept of multilevel inverter control has opened a new possibility that induction motors can be controlled to achieve dynamic performance equally as that of DC motors. . The recent advancement in Power Electronics has been initiated to improve the level of inverter rather than increasing the filter size. Using multilevel inverter, it is better to reduce the harmonics. In this research, sinusoidal pulse-width modulation technique will be used for multilevel inverter system to reduce the harmonics. Even updated pulse-width modulation (PWM) techniques used to control modern static converters such as machine drives, power factor compensators do not produce perfect waveforms, which strongly depend on the semiconductors switching frequency. Also, the distorted voltages and current waveforms produce harmonic contamination, additional power losses and high frequency noise that can affect not only the power load but also the associated controllers. All these unwanted operating characteristics associated with PWM converters could be overcome with multilevel converters, in addition to the fact that higher voltage levels can be achieved Very popular application is the classic carrier based sinusoidal PWM (SPWM) that uses the phase shifting technique to reduce the harmonics in the load voltage. In this paper, a three-phase diode clamped multilevel inverter fed induction motor is described. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. The voltage across the switches has only half of the dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device. Here the speed of an induction motor is precisely controlled by using three level diode clamped multilevel inverter.

2. VOLTAGE SOURCE INVERTERS
Voltage source inverters will provide significant advantages: it can control the output frequency and voltage from energy sources and it can also control the active and reactive power flow from a utility connected to power source. This offer many benefits for power applications. In particular, uninterruptible power supplies (UPSs), static *VAR* compensation, harmonic compensation and active filters.

2.1. Two-Level Three-Phase Inverter
The voltage source inverter produces an output voltage or a current with levels either zero or +/- Vdc. They are known as two level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width modulation strategies. In high-power and high-voltage applications, these two-level inverters have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. The dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maxi mum allowable switching frequency has to be more lowered; hence the harmonic reduction becomes more difficult. In addition, the two level inverters generate high frequency common-mode voltage within the motor windings which may result in motor and drive application problems. The inverter is limited by voltage ratings of switching devices; the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maxi mum allowable switching frequency has to be more lowered; hence the harmonic reduction becomes more difficult. In addition, the two level inverters generate high frequency common-mode voltage within the motor windings which may result in motor and drive application problems. From the aspect of harmonic reduction and high dc-link voltage level, three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage. A three level inverter will not generate common-mode

voltages when the inverter output voltages are limited within certain of the available switching states. So the three-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems.

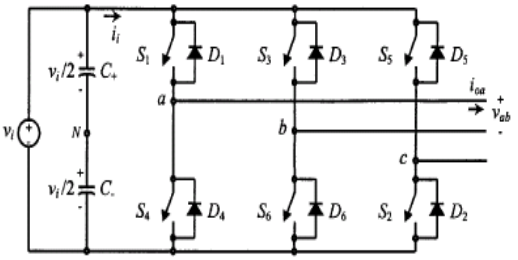

Fig.1. two level voltage source converter

2.2. Diode-Clamped Multi-Level Inverter

The most common used of multilevel inverters is the diode-clamped multilevel inverter. It provides a significant advantage it can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode clamped inverter implementation has been mostly limited to the three-level .In general in *n-level* diode-clamped inverter there are (n − 1) adjacent transistors gated on for producing each switching state.

2.3. Three-Level Diode-Clamped Inverter

This topology has twice as many transistors as well as added diode compared to the two-level inverter as it shown in Fig.1, each of the switches must block only one half of the DC link voltage although the structure is more complex and the switching is straightforward.

Three level inverters are capable in producing three different levels of output voltage (+Vi/2, 0, -Vi/2).There are a total of 27 (*n*3 = 33 where n is the number of levels) possible switching combinations (vectors),Table.15.7 presents the switching possibilities for phase-a.

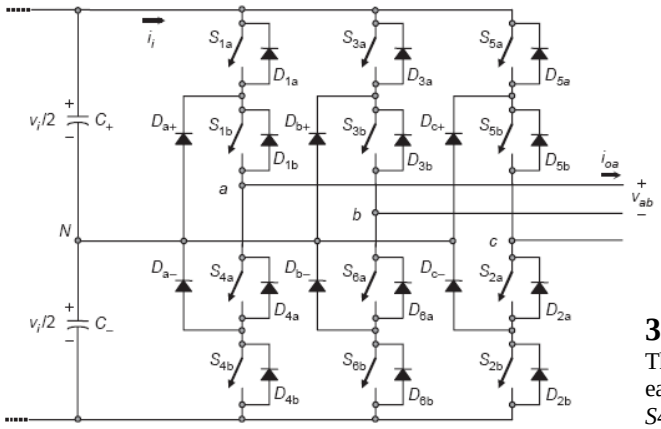

Fig.2. Three level voltage source Inverter

s_{1a}	s_{1b}	s_{4a}	s_{4b}	v_o	Components conducting	
1	1	0	0	$v_i/2$	S_{1a}, S_{1b}	if $i_{oa} > 0$
					D_{1a}, D_{1b}	if $i_{oa} < 0$
0	1	1	0	0	S_{1b}, D_{a+}	if $i_{oa} > 0$
					S_{4a}, D_{a-}	if $i_{oa} < 0$
0	0	1	1	$-v_i/2$	D_{4a}, D_{4b}	if $i_{oa} > 0$
					S_{4a}, S_{4b}	if $i_{oa} < 0$

Fig.3. Valid Switch states for a three level VSI, phase a

3. MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

AC input is rectified using a diode rectifier. It is filtered using a capacitor filter. DC is applied to the multilevel inverter. The output of the inverter is fed to the Induction motor. This system will be simulated using Matlab simulink. The simulink Model for multilevel inverter fed system is depicted in Fig. Input pulses to the IGBT are generated by the SPWM Modulation technique circuit generates the gating pulses required by the inverter. The phase voltages and line to line voltages are measured by the scopes connected at the output. The scope is connected to measure parameters like voltage rotor speed and torque. The pulses are generated using SPWM method. This is accomplished by comparing the modulating sine wave with only one triangular carrier wave for the generation of PWM signals in the lower output voltage range and with two triangular carrier waves in the higher output voltage range .The number of switching's per modulation cycle at each level of the inverter is dependent on the carrier frequency for that level and the duration of time that the reference waveform dwells within the level's corresponding time band. If the carrier frequency for all of the levels is identical, the top and the bottom levels will have many more switching's than the intermediate levels

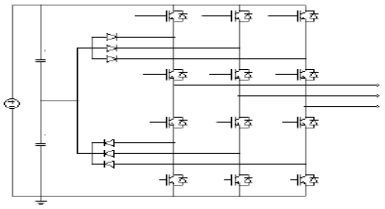

Fig. 4: The power circuit of the multilevel inverter

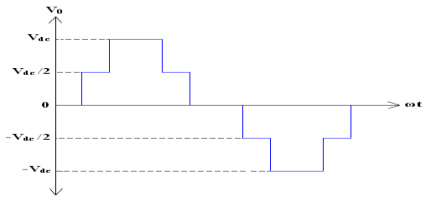

Fig: 3- Level output voltage

3.1. Principal operation of 3-Level inverter

The easiest way of obtaining the valid switch states is to analyse each phase separately. Phase *a* contains the switches *S*1*a*, *S*1*b*, *S*4*a*, and *S*4*b*, which cannot be on simultaneously because a short circuit across the dc bus would be produced, and cannot be off simultaneously because an undefined phase voltage *vaN* would be produced. Switch *S*1*a* state is always the opposite to switch *S*4*a* state, and that switch *S*1*b* state is always the opposite to switch *S*4*b* state Any other switch-state combination would result in an undefined inverter phase *a* voltage because it will depend

upon the load-phase current *ioa* polarity. The switch states for phases *b* and *c* are identical to that of phase *a*; moreover because they are paralleled, they can operate in an independent manner.

4. PULSE WIDTH MODULATION TECHNIQUES

The objective to achieve a variety of aims such as: wide linear modulation range; less switching loss; less total harmonic distortion (THD) in the spectrum of switching waveform, and easy implementation and less computation time were the motivation for developing different modulation strategies with different concept and performance.

Carrier Based Pulse width modulation (CBPWM) technique has been extensively used, because it improves the harmonic spectrum of the inverter by moving the voltage harmonic components to higher frequencies. With the development of microprocessors, space-vector modulation was introduced in the mid of 1980s as an alternative method for determining the switched pulse widths. It becomes the most important PWM methods for three-phase converters due to its ability to reduce commutation losses and the harmonic contents of output voltage, as well as obtaining higher amplitude modulation indexes.

4.1. Carrier-Based Pulse Width Modulation

Carrier-based PWM (CBPWM) methods compare a reference waveform with a triangular or saw-tooth carrier at a higher frequency in order to generate the gating signals to switch on or off the switching device. The operation of PWM can be divided into two modes:

1) Linear Mode: in the linear mode, the peak of a modulation signal is less than or equal to the peak of the carrier signal. The maximum boundary for this mode when the value of the modulation index (m) reaches 1, (m=1), which gives the maximum peak amplitude of the fundamental output voltage as Vo(max)= Vs.

2) Nonlinear Mode: this operation is called *over modulation*, where the modulation index is greater than 1, (m>1), leads to get a square-wave operation and adds more harmonics as compared to operation in the linear Mode. This operation is normally avoided in applications requiring low distortion for example in (UPSs) applications. In general Carrier Based Modulation has high Harmonic distortion at a high modulation index and when the switching frequency for the switching devices is low, which is almost inevitable for high power applications.

4.2. Multi-Level Carrier Based Pulse Width Modulation

For a n-level inverter, n-1 carrier signals with the same frequency and same peak to peak amplitude are disposed such that the bands they occupy are contiguous, see Fig. As mentioned earlier, one of the important advantages of the proposed 3-level inverter is that it can be operated as a 2-level inverter in the lower output.

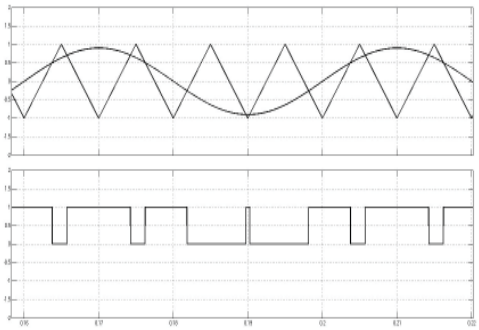

Fig.5 Carrier based pulsed width modulation

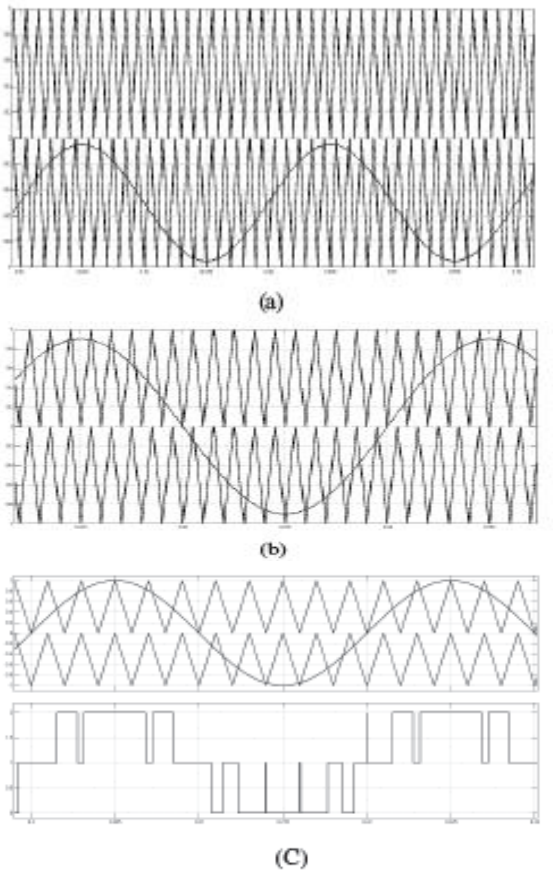

Fig.6. Three-level carrier based PWM, (a) Inverter runs at the two-Level Mode, (b) Inverter runs in the Three-Level Mode, (c) Three-level PWM signals generation.

5. CONTROL STRATEGY

Fig. shows the relation between the voltage and torque versus frequency. The voltage and frequency being increased up to the base speed. At base speed, the voltage and frequency reach the rated values. We can drive the motor beyond base speed by increasing the frequency further. But the voltage applied cannot be increased beyond the rated voltage. Therefore, only the frequency can be increased, which results in the field weakening and the torque available being reduced. Above base speed, the factors governing torque become complex, since friction and windage losses increase significantly at higher speeds. Hence, the torque curve becomes nonlinear with respect to speed or frequency.

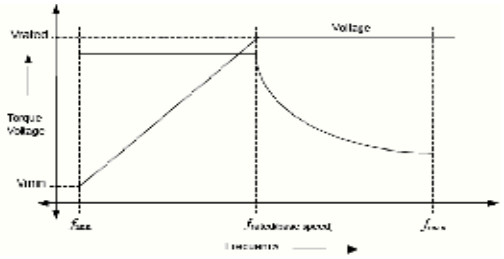

Fig.7.Speed-Torque characteristics with V/f control.

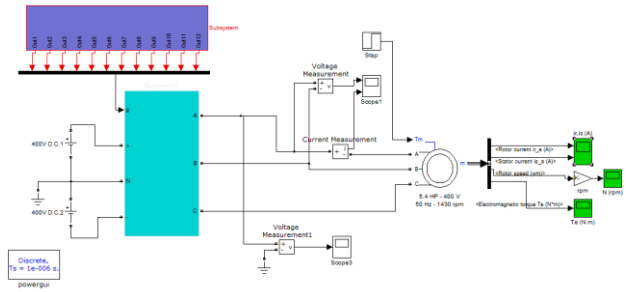

Fig.10. Simulated circuit for three level voltage source inverter

6. SIMULATED CIRCUITS AND WAVEFORMS

Fig. shows the PWM circuit to generate the gating signals for the multilevel inverter switches. To control a three phase multilevel inverter with an output voltage of three levels; two carriers are generated and compared at each time to a set of three sinusoidal reference waveforms. One carrier wave above the zero reference and one carrier wave below the reference. These carriers are same in frequency, amplitude and phases; but they are just different in dc offset to occupy contiguous bands. Phase disposition technique has less harmonic distortion on line voltages. Fig.9. shows the waveform of sine-triangle intersection. Two carriers together with modulation signal have been used to obtain SPWM control.

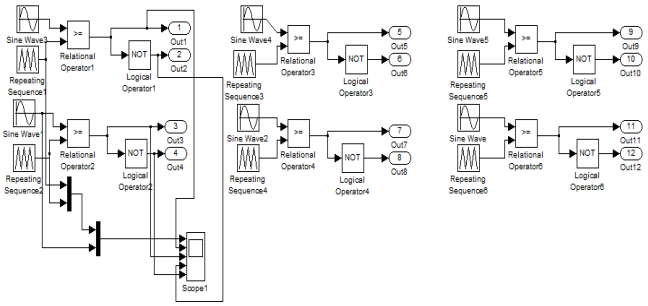

Fig .8. PWM simulated circuit

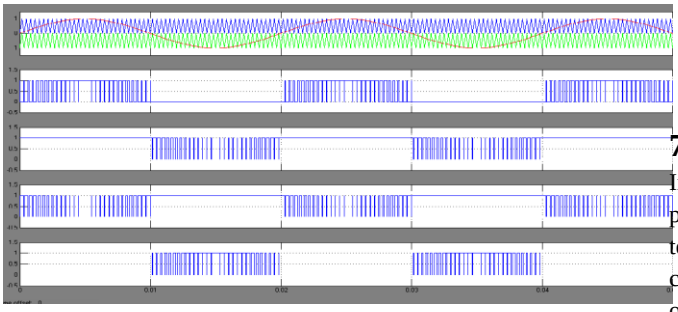

Fig. 9.PWM simulated result

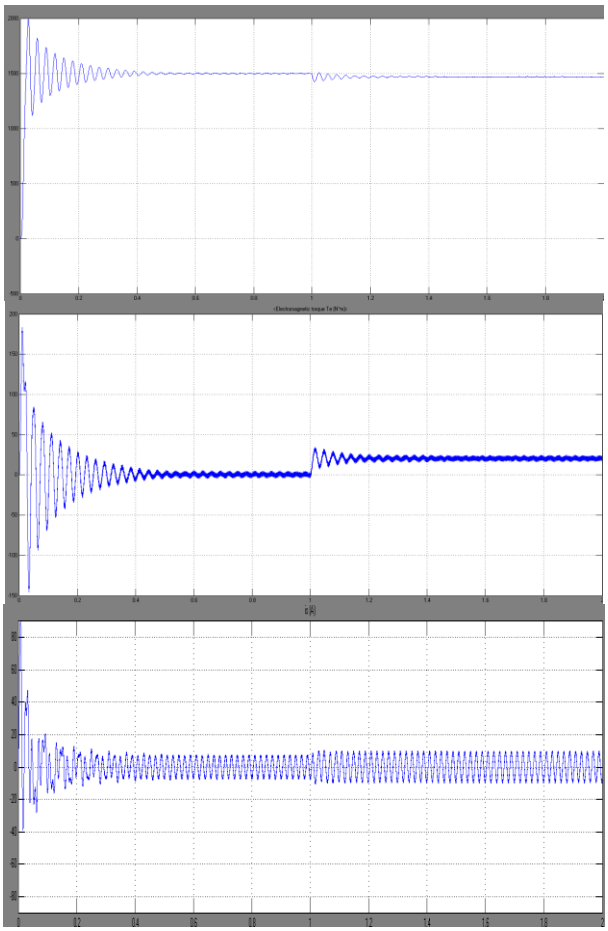

Fig. 11. Simulated result of speed, torque and current.

7. CONCLUSION

In this paper a diode clamped multilevel inverter has been presented for drive applications. The multicarrier PWM technique can be implemented for producing low harmonic contents in the output; hence the high quality output voltage was obtained. The open loop speed control was achieved by maintaining V/f ratio at constant value. The simulation results show that the proposed system effectively controls the motor speed and enhances the drive performance through reduction in total harmonic distortion (THD). This drive system can be used for variable speed applications like conveyors, rolling mills, printing machines etc.

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