Design of Multiplier based Low Power PID Controllers

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ABSTRACT
The increasing industrial growth needs its system to be fully controllable. Such control systems are almost composed of VLSI components such as adders, multipliers and accumulators. This paper analyzes two MAC units with array, booth algorithms and those blocks are incorporated in PID controller architecture. Comparisons are made with power consumption of each architecture. The simulations are done in Modelsim and power results are synthesized using Xilinx ISE. The results suggest that the PID controller with booth based MAC unit and PID architecture consumes less power when compared to array based architectures.

General Terms
VLSI, Multiplication algorithms and Power consumption.

Keywords
Multiply-Accumulate (MAC), Array Multiplier, Booth Multiplier, Proportional-Integral-Derivative controllers (PID)

1. INTRODUCTION
With the development of industrial equipments, engineers are in search of efficient control structures. But still Proportional-Integral-Derivative (PID) controller strongly holds its place in industries such as robotics, automation systems, aerospace and process control because of its simple control structure, remarkable efficiency, robust performance and low power consumption. A PID will make the output plant to behave in a desired manner, causing the output to follow a reference input signal. For proper tracking of output to its reference, controllers are in need of delay-less (i.e., quick computation of inner arithmetic operations) architectures. The various modules in controllers are designed with the help of state machines [1]. The looping of multipliers from controllers are shown in [2]. Seven adders based PID controllers are simulated and the results are compared in [3]. Controllers with Vedic multipliers are designed in [4]. The MAC flow diagram for simulation is taken from [5]. This paper outlines significant Multiplier-Accumulator (MAC) architectures of PID which might highlights on high speed, low power consumption. Comparisons are made between power, delay and power-delay product.

The controller's output is the summation of proportional, integral and derivative gains which is given by,

$$u(k) = P(k) + I(k) + D(k) \quad (1)$$

The output equation is abbreviated with the error signal as

$$u(t) = K_p\left(e(t) + \frac{1}{Ti}\int_0^t e(t)\,dt + T_d\frac{de(t)}{dt}\right) \quad (2)$$

Where, K_p is the proportional gain, T_i is the integral time constant and T_d is the derivative time constant.

The block diagram of PID is depicted in Figure 1.

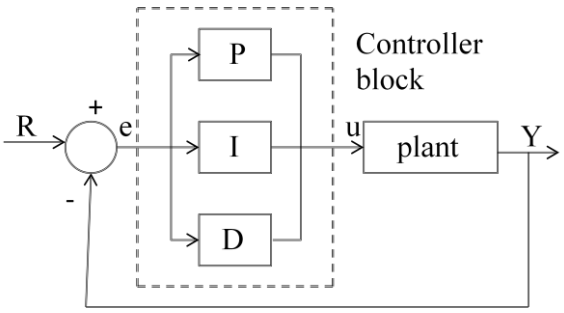

Fig 1: PID general architecture

Where, R, e and u represents the reference input, error signal and output of the controller.

There are many tuning schemes are proposed for the efficient operation of PID controller. This paper gives a special attention to the inner architecture especially on multiplier, adder and accumulator which decides the entire controller performance.

2. MULTIPLY-ACCUMULATE BLOCK
The error signal which is calculated by subtracting the reference signal and the output is given as input to the multiplier. The adder receives input from the multiplier and the previously accumulated value from the shift register as shown in Figure 2. The choice of the multiplier depends on the application. Array multipliers usually have regular structures and are easy to expand. The partial products are generated by multiplying the multiplicand with their respective multiplier bits. The generated partial products are shifted according to their bit orders and then added as in Figure.3. Array multiplication needs to add as many partial products as there are in multiplier bits. The generation of A partial products requires A×B two-bit AND gates.

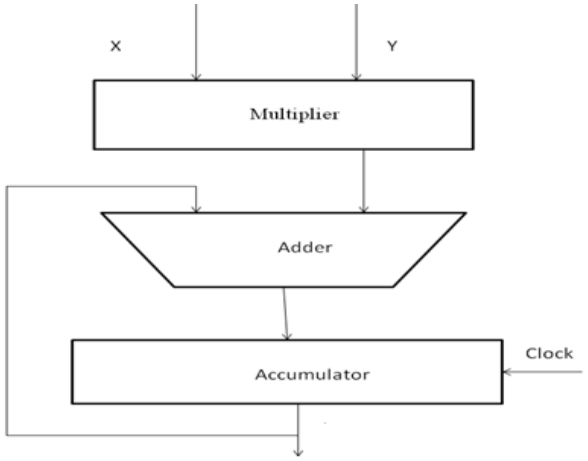

Fig 2: MAC unit

A booth multiplier consists of a booth encoder, carry save adder tree to add partial products and a final adder for the result. This approach utilizes fewer additions and subtractions than straight forward algorithms. The partial products generated using booth encoder is given as input to the carry save adder so that sum and carry outputs are obtained. The number of partial products generated in booth algorithm is halved when compared with array multiplier.

Table 1. Booth Algorithm

a_i	a_{i-1}	Operation
0	0	No operation
0	1	Add b
1	0	Subtract b
1	1	No operation

The output from the multipliers is added with the previously accumulated value. The adder used here is the Ripple carry adder. A ripple carry adder is simply several full adders connected in series such that the carry can propagate through full adder before the addition. The carry propagation chain will determine the latency of the entire ripple carry adder circuit.

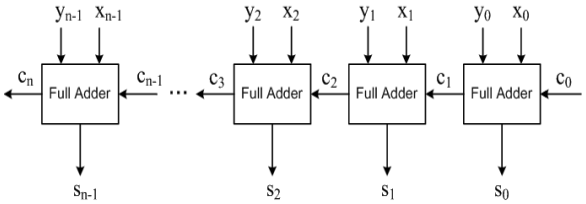

Fig 3: n-bit Ripple Carry Adder

A register is a group of binary storage cells (such as flip flops) capable of holding binary information. It also has combinational part for data processing tasks. There are a group of flip-flops connected in a chain so that the output from one becomes the input of the next which is depicted in Figure 4. All the flip flops are driven by a common clock, and all are set or reset simultaneously. When there is a clock signal, the inputs D0,D1….D7 are loaded parallel into the register and the outputs Q0,Q1,….Q7 are also available in parallel at the output. All the data gets shifted simultaneously during a single clock cycle. Parallel shifting is much faster than serial shifting.

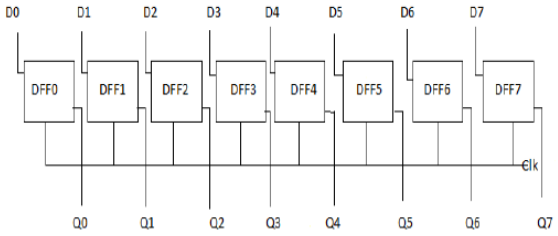

Fig 4: PIPO Shift Register

3. PID WITH PROPOSED MAC UNIT

PID Controller is used in higher order dynamics. The two standard versions of PID are incremental form and commercial form. The incremental form has the series drawback that it cannot be used for P and PD controllers. In commercial form the transfer functions are approximated by limiting the derivative gain and setpoint weight. The designed MAC unit is embedded in the PID architecture. Due to quick computation of arithmetic operations, the controller is able to calculate its error value for next cycle. The error signal is measured by calculating difference between the reference value and the previous value stored in the register. When there is four inputs, DMAC (Double MAC) instead of MAC, is used to reduce the complexity. The coefficients of PID are utilized in architecture as per the equations. The designed PID can be used for various closed loop performance. $U_c(k)$ is the reference signal and Y(k) is the feedback stored in the register. The subtractor subtracts the two values and stored in a register for future operations as in Figure 5. The commercial PID overcomes the drawbacks of incremental PID and can be used for all individual and combinations of controllers.

The designed MAC unit with array multiplier and booth multiplier is embedded in the PID architecture to compare the performance. Since the booth multiplier reduces the partial products row, delay is reduced. Power consumption is also less due to less usage of logic gates when compared to array multiplier. The registers in the PID architecture are used to temporarily store the results of previous blocks. The commercial PID with their coefficients as the input to MAC and DMAC is shown in Figure 5. The coefficient values depends on the time constants of proportional, integral and derivative controllers.

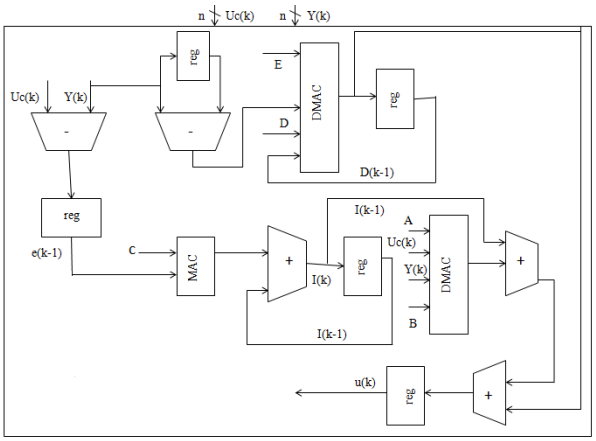

Fig 5: Commercial PID architecture

4. RESULTS AND DISCUSSIONS

The array based and booth based MAC units are simulated. The booth multiplier gives the output by reducing the partial product row. The ripple carry adder for 16 bit consists of series 16 full adder and the results shown in Figure 6. The adder gets its first input from the multiplier and the second one from the register which is previously accumulated.

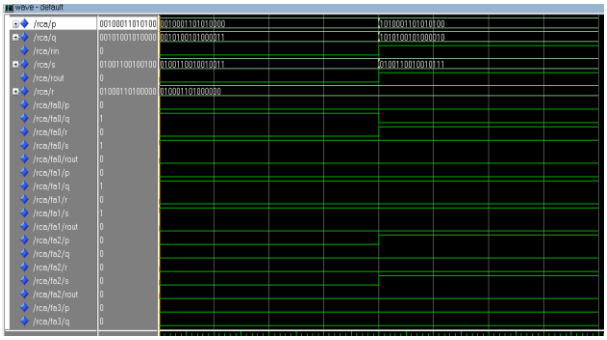

Fig 6: Ripple Carry Adder Output

The parallel in parallel out shift register receives its input from the adder and gives the output after a delay depicts in Figure 7. Each D-flip flop receives its respective bit from the ripple carry adder output and is accumulated for a certain time delay and delivers the output.

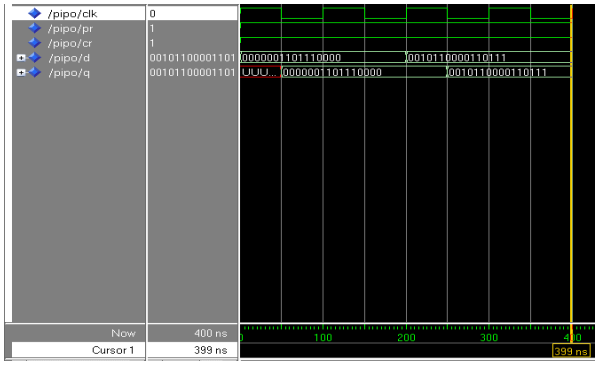

Fig 7: PIPO shift register Output

The array multiplier utilizes 64 AND gates and 56 Full Adders. Each AND gate and Full Adder output is simulated such that the overall output is shown in Figure 7.The booth multipliers uses booth encoder and carry save adder for the multiplication. The encoder encodes the multiplier and does the respective operation with the multiplicand. The encoder, the adder and the overall booth multiplication is shown in Figure 8.

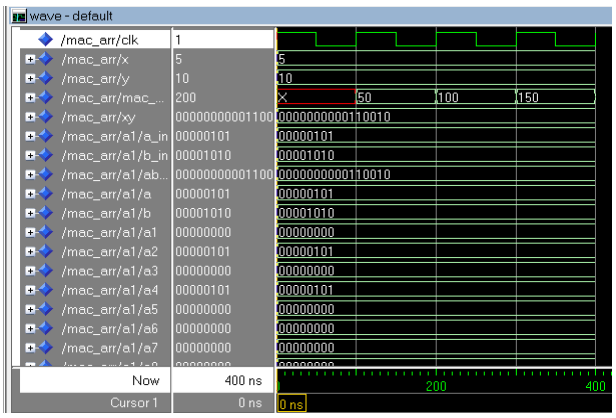

Fig 8: Waveform of array based MAC

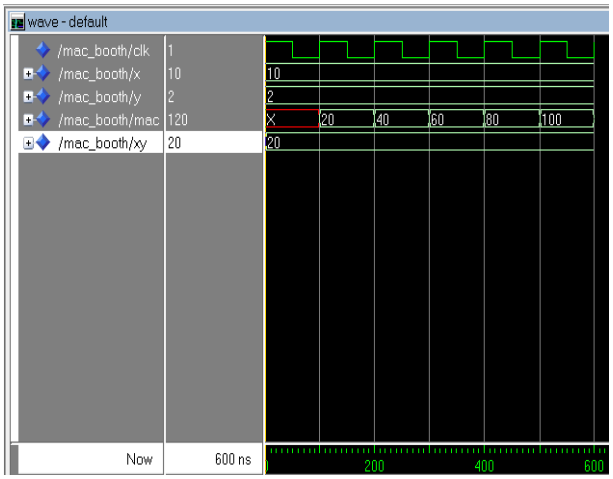

Fig 9: Waveform of booth based MAC

The power results for these MAC units are measured in XILINX ISE and the values are tabulated as follows.

Table.2 Power Comparison

MAC model	Power(mW)
Array	168
Booth	146

The synthesis results depicts that the booth based MAC unit consumes less power when compared to array based MAC. The array MAC utilizes more power.

5. CONCLUSION

Different multiplier based MAC unit has been designed and the power results are compared for better performance of PID controller. The wallace tree MAC architecture consumes less power when compared to array based MAC and booth based MAC architectures. The future consideration of this paper is to embed the above three MAC unit in PID architecture. The PID with better performance in terms of power will be implemented using FPGA.

6. REFERENCES

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